



1990 New Releases Data Book

**A/D Converters
D/A Converters
Analog Switches
Analog Multiplexers
Active Filters
Power Supply Circuits**

**Video Products
RS-232/Interface Circuits
Op Amps/Buffers
Voltage References
Display Drivers
Timers/Counters**



1990 NEW RELEASES DATA BOOK

A/D Converters

D/A Converters

Voltage References

Op Amps/Buffers/Comparators

Power-Supply Circuits

Interface

Analog Filters

Analog Multiplexers

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Introduction

Maxim Integrated Products designs, develops, manufactures and markets a broad range of linear and mixed-signal integrated products for use in a variety of electronic products. These products "connect" the real (analog) world to the digital world. They detect, measure, amplify and convert real world signals, such as temperature, pressure or sound, into digital signals a computer can process. Over the past six years, Maxim has introduced over 350 products - more analog ICs than any other company.

Maxim is committed to meeting the needs of the industry through aggressive product development and superior quality. The Company's products include: data converters and references, RS-232 interface circuits, amplifiers, power control circuits, timers and counters, display circuits, multiplexers and switches, voltage detectors and filters. Recognizing the growing demand for CMOS, the emerging technology of the future, Maxim has focused increasingly on CMOS-based products. These circuits are marketed worldwide, principally through distributors and independent sales representatives, and are available in several different packages and temperature ranges to meet varying customer requirements.

New Releases

Since the publication of our full line 1989/90 Integrated Circuits Data Book, more than 70 new products have been added to our product lines. These, and other older but unique Maxim products, are collected into a single volume in this new data book. We hope that this enables you to have quick access to "what is new and exciting from Maxim". Older products, and some recently introduced second-source products are left out of this book, but can be located using the Table of Contents or the Index. You can get data sheets for these products by contacting your local Sales Representative, or the factory directly.

Customer Service

Customer Service Representatives are available during normal business hours to provide you with information on orders placed directly with the factory or by any of our

franchised distributors. Please see the Appendix for a list of domestic and international sales representatives, and distributors.

Technical Support

The technical literature in this volume discusses the operation and applications of Maxim products as they apply to design problems. In addition to the individual data sheets/applications notes in this book, Maxim offers a full line *Integrated Circuits Data Book*, a *Military Products Data Book*, and a free subscription to the *Maxim Engineering Journal* - a quarterly magazine covering the application of Maxim analog ICs. For on-line technical support you can talk with a senior applications engineer at (408) 737-7600 extension 4000 or, after normal business hours, you can FAX in your questions at (408) 736-1831.

Reliability

Providing reliable, innovative analog ICs that solve customer problems is the cornerstone of Maxim's existence. Our programs offering free burn-in at 150°C (for all DIPs) and complete lot traceability, life test and pressure pot qualification are unique in the industry.

On July 1, 1988, Maxim became a certified manufacturer of MIL-STD-883 Class B, Rev. C products. To date, the company has announced over 40 of its 350 products screened to military standards, 28 are in qualification and more are scheduled for qualification in the future.

All of Maxim's products are available screened to a "High Reliability" flow that emulates Rev. C, MIL-STD-883, Class B standards. These "/HR" parts are fully tested over the military temperature range and are sold at significantly lower prices than /883 compliant products.

Following Maxim's charter to provide analog solutions in silicon, we will continue to offer /883B Rev. C and /HR devices, SMDs (Standard Military Drawings) when available and SCDs (Customer Source Control Drawings) in the future. We welcome you to visit our new facilities for a first hand inspection and look forward to the opportunity to serve you. Contact your local Sales Representative or the factory directly, (408) 737-7600 extension 6283, for more information.

Information furnished by Maxim Integrated Products is believed to be accurate and reliable. However, the company cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product; nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Maxim Integrated Products. Maxim reserves the right to change the circuitry and specifications without notice.

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Products in this book may be covered by one or more of the patents listed below. Additional patents are pending.
4,700,286, 4,679,134, 4,636,930, 4,859,963, 4,857,778, 4,897,774, 4,797,899, 4,806,875, 4,847,522, 4,812,891, 4,809,152, 4,801,888, 4,797,569, 4,777,580, 4,777,577.

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MAXIM

3³/₄ Digit DMM Circuit

MAX133/MAX134

General Description

The MAX133 and MAX134 are integrating A/D converters for 3³/₄ digit multimeters and data acquisition systems such as data loggers and weigh scales. The A/D's internal resolution is $\pm 40,000$ counts. An extra digit is supplied as a guard digit to allow autozero or tare of a 4000 count displayed reading to 1/10 of a displayed count. The conversion time is 50ms.

The MAX133 and MAX134 differ only in their microprocessor interface. The MAX133 has a 4 bit multiplexed address/data bus while the MAX134 has 3 separate address lines and a 4 bit bidirectional data bus. Both devices can be used with 4, 8, and 16 bit microprocessors.

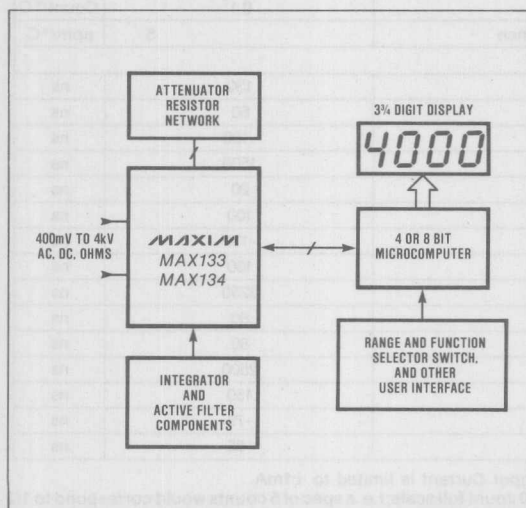
When controlled by a microprocessor, the MAX133 and MAX134 can perform auto-ranging measurements from $\pm 400.0\text{mV}$ to $\pm 4000\text{V}$ full scale. External attenuator resistors are required, but range switching is performed by the A/D.

The power supply is typically a 9V battery or $\pm 5\text{V}$. Operating current is typically $100\mu\text{A}$ while standby current is only $25\mu\text{A}$.

Applications

Digital Panel Meters
Weigh Scales
Data Loggers
Data Acquisition Systems

Typical Operating Circuit



Features

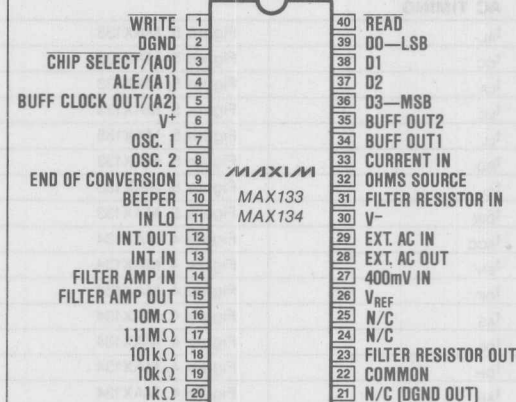
- ◆ 40,000 Count Resolution
- ◆ 0.025% Accuracy
- ◆ 20 Conversions per Second
- ◆ Microprocessor Interface
- ◆ $100\mu\text{A}$ Operating Supply Current
- ◆ Low External Component Count
- ◆ $5\mu\text{V}$ Resolution
- ◆ Demonstration Kit Available
MAX134/DEMO

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX133CPL	0° C to +70° C	40 Lead Plastic DIP
MAX133CQH	0° C to +70° C	44 Lead Plastic Chip Carrier
MAX133C/D	0° C to +70° C	Dice
MAX133EPL	-40° C to +85° C	40 Lead Plastic DIP
MAX133EQH	-40° C to +85° C	44 Lead Plastic Chip Carrier
MAX134CPL	0° C to +70° C	40 Lead Plastic DIP
MAX134CQH	0° C to +70° C	44 Lead Plastic Chip Carrier
MAX134C/D	0° C to +70° C	Dice
MAX134EPL	-40° C to +85° C	40 Lead Plastic DIP
MAX134EQH	-40° C to +85° C	44 Lead Plastic Chip Carrier

Pin Configuration

Top View



Pin Names in parentheses are for MAX134 only.

MAXIM

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3¾ Digit DMM Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
V ⁺ to V ⁻	+15V
V ⁺ to DGND	+6V
V ⁻ to DGND	-9V
Analog Input Voltage (any input) (Note 1)	V ⁺ to V ⁻

Reference Input Voltage	V ⁺ to V ⁻
Digital Inputs	(DGND - 0.3V) to (V ⁺ + 0.3V)
Power Dissipation	800mW
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering 10 sec)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V⁺ = 9V, T_A = +25°C, Test Circuit unless otherwise indicated)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ANALOG					
Zero Input Reading	Read Zero Mode, DC Volts Zero Input Offset Reading will be corrected Digitally in the μ P			±5000	Count
Δ Zero Input Reading	Difference between 1000VDC Scale, V _{IN} = 0 and 3VDC and Scale, V _{IN} = 0 (Note 3)	-2		+2	Count
I _{10MΩ}	Leakage Current into 10M Ω Pin			20	pA
Rollover Error	V _{IN+} = V _{IN-} = 3V	-10		+10	Count
Integral Linearity	Best Fit Line 300mVDC Scale Not production tested	-10		+10	Count
Differential Nonlinearity	Deviation from ideal Count size Not production tested		0.1	5	Count
Recovery Time	Number of Conversions to settle to within 2 Counts of final reading on 3 VDC Scale after attempting to measure a 2.95V Input on the 300mV Scale. Unfiltered DC Mode Settle to 1 Count		1 2		Conv.
CMRR	V _{CM} = ±500mV V _{CM} is (IN LO - Common)		86		dB
Noise	300mVDC Scale Zero Reading Mode Pk-Pk Value exceeded less than 5% of readings		2 2		Count
Zero Reading Drift			0.1		Count/°C
Scale Factor Tempco	300 mVDC scale 0ppm ext Reference			5	ppm/°C
AC TIMING					
t _{AL}	Figure 5, MAX133		130		ns
t _{CC}	Figure 5, MAX133		60		ns
t _{LA}	Figure 5, MAX133		-100		ns
t _{LC}	Figure 5, MAX133		1500		ns
t _{LL}	Figure 5, MAX133		20		ns
t _{RD}	Figure 5, MAX133		100		ns
t _{CL}	Figure 5, MAX133		-130		ns
t _{DW}	Figure 5, MAX133		100		ns
t _{ACC}	Figure 4, MAX134		3250		ns
t _{EN}	Figure 4, MAX134		80		ns
t _{OP}	Figure 4, MAX134		80		ns
t _{AS}	Figure 4, MAX134		2500		ns
t _{DS}	Figure 4, MAX134		150		ns
t _{DH}	Figure 4, MAX134		-75		ns
t _{AH}	Figure 4, MAX134		-85		ns

Note 1: Input Voltage may exceed supply voltages, provided the Input Current is limited to ±1mA.

Note 2: Analog performance is specified in counts relative to a 40,000 count full scale; i.e. a spec of 5 counts would correspond to 1/2 of one count on a 3¾ digit meter.

Note 3: This parameter is guaranteed by testing the input bias currents of the input pins 10M Ω and 1.11M Ω .

3³/₄ Digit DMM Circuit

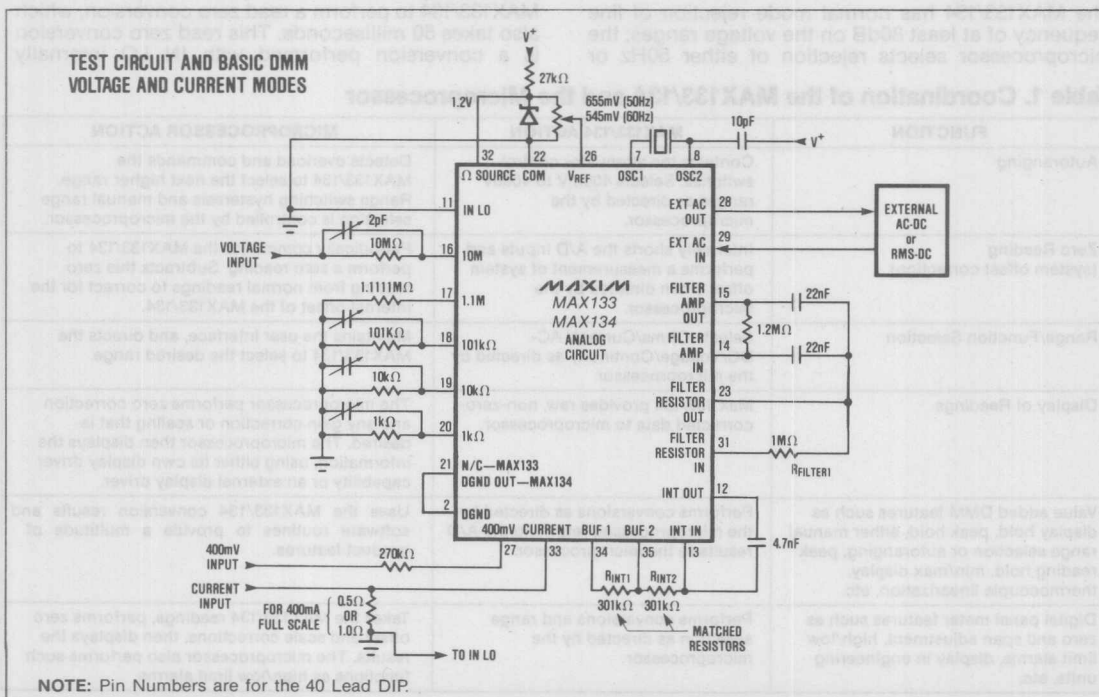
MAX133/MAX134

ELECTRICAL CHARACTERISTICS (continued)

(V⁺ = 9V, T_A = +25°C, Test Circuit unless otherwise indicated)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY AND DIGITAL SECTION						
Digital Ground Voltage	DGND	Referenced to V ⁺ 5μA < I _{SINK} < 500μA	-4.5	-5	-5.5	V
Analog COMMON Voltage		(V ⁺ - Common) 250kΩ between V ⁺ and COMMON	2.8	3.0	3.3	V
Analog COMMON Sink Impedance		ΔV, I _{COMMON} = 10μA to I _{COMMON} = 2mA		4	20	Ω
Analog Common Source Capability		For ΔV _{COMMON} < 0.5V		1		μA
Tempco of Common				80		ppm/°C
Output High	V _{OH}	D ₀₋₃ , Data Ready I _{OUT} = -100μA	V ⁺ - 0.5			V
Output Low	V _{OL}	D ₀₋₃ , Data Ready I _{OUT} = 400μA			0.4	V
Input High	V _{IH}	D ₀₋₃ , A ₀₋₃ , Data Ready, RD, WR	70	45		% (V ⁺ - DGND)
Input Low	V _{IL}	D ₀₋₃ , A ₀₋₃ , Data Ready, RD, WR		1.6	0.8	V
Supply Current	I _{SUPP}			100	250	μA
Sleep Current	I _{SLEEP}			25		μA
Low Battery	V _{LBAT}	Low Battery Flag On	6.3	6.8	7.5	V

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3³/₄ Digit DMM Circuit

System Considerations

The MAX133/134 is intended for use with a microprocessor. The MAX133/134 contains an A/D and auxiliary circuitry such as attenuator range switches, a piezoelectric beeper driver, an active filter, a low battery detector, and both analog and digital power supplies; but it does not include any display drive capability. The MAX133/134 reduces the component count and system cost by minimizing the external components required for the analog portion of the system, but does not restrict final product features by including autoranging or other digital control functions. The MAX133/134 is intended to work as the analog front end of a microprocessor, with the features of the end product being determined by the microprocessor software. Table 1 shows how the execution of several typical functions is partitioned between the MAX133/134 and the microprocessor.

The MAX133/134 provides all of the logic and counters for control of the conversion sequence, and the external microprocessor does not have to perform any critical timing or complex control of the MAX133/134. The MAX133/134 has range switches for a 5 decade attenuator which uses external resistors, and has additional mode-selection circuitry for performing voltage, current, AC or DC, ohms, and continuity measurements. The 5 decade attenuator and mode-selection circuitry is controlled by an external microprocessor via control bits written into the MAX133/134.

The MAX133/134 has normal mode rejection of line frequency of at least 80dB on the voltage ranges; the microprocessor selects rejection of either 50Hz or

60Hz by setting a MAX133/134 control bit. A two pole active filter can also be turned on by the microprocessor, adding about 40 dB normal mode rejection above 50Hz. See the "Digital Interface" section for details on which functions can be controlled by the external microprocessor.

The basic blocks of the MAX133/134 are

- A/D section
- Input Range Switching
- Ohms Circuitry
- Active Filter
- Power Supply, Common, Low Battery Detector
- Oscillator and Beeper Driver
- Digital Interface

A/D Section

The A/D uses a "residue multiplication" conversion scheme to provide a full $\pm 40,000$ count resolution reading every 50 milliseconds, while still providing the excellent noise performance and power line normal mode rejection associated with integrating A/Ds. See "Conversion Method and Timing" below for details of the conversion method. All timing and A/D conversion phase control is performed by the MAX133/134 without microprocessor intervention. The A/D section will perform a non-zero-corrected conversion every 50 milliseconds (20 conversions per second).

The microprocessor must periodically direct the MAX133/134 to perform a read zero conversion, which also takes 50 milliseconds. This read zero conversion is a conversion performed with IN LO internally

Table 1. Coordination of the MAX133/134 and the Microprocessor

FUNCTION	MAX133/134 ACTION	MICROPROCESSOR ACTION
Autoranging	Contains the attenuator control switches. Selects 400mV to 4000V ranges as directed by the microprocessor.	Detects overload and commands the MAX133/134 to select the next higher range. Range switching hysteresis and manual range selection is controlled by the microprocessor.
Zero Reading (system offset correction)	Internally shorts the A/D inputs and performs a measurement of system offset when directed by the microprocessor.	Periodically commands the MAX133/134 to perform a zero reading. Subtracts this zero reading from normal readings to correct for the internal offset of the MAX133/134.
Range/Function Selection	Selects Ohms/Current/ AC-DC/Voltage/Continuity as directed by the microprocessor.	Maintains the user interface, and directs the MAX133/134 to select the desired range.
Display of Readings	Max 133/134 provides raw, non-zero-corrected data to microprocessor.	The microprocessor performs zero correction and any gain correction or scaling that is desired. The microprocessor then displays the information, using either its own display driver capability or an external display driver.
Value added DMM features such as display hold, peak hold, either manual range selection or autoranging, peak reading hold, min/max display, thermocouple linearization, etc.	Performs conversions as directed by the microprocessor, returning the A/D results to the microprocessor.	Uses the MAX133/134 conversion results and software routines to provide a multitude of product features.
Digital panel meter features such as zero and span adjustment, high/low limit alarms, display in engineering units, etc.	Performs conversions and range selection as directed by the microprocessor.	Takes the MAX133/134 readings, performs zero offset and scale corrections, then displays the results. The microprocessor also performs such functions as high/low limit alarms.

3³/₄ Digit DMM Circuit

MAX133/MAX134

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shorted to IN HI, and the result of this zero conversion must be subtracted (by the microprocessor) from normal measurements to obtain a zero-corrected reading. The zero correction that must be subtracted is determined by the MAX133/134's internal offsets. Since these offsets are relatively slow changing, zero conversion readings need only be taken often enough to track long term drifts and temperature changes. The zero conversion reading will change slightly with a change in common mode input voltage or reference voltage, and a new zero conversion reading should be taken if either of these change.

In ratiometric ohms measurement the reference voltage will change significantly as the value of the unknown resistor varies. To reduce the errors caused by the system offset the MAX133/134 "chops" the input buffer and integrator. The "chop" consists of a reversal of the input transistors during the conversion cycle. The timing of this chop is such that in the R/2 or ohms measurement mode, the system offset is almost completely nulled out if the X2 mode is not selected. Even if the X2 mode is selected, the system offset does not exceed 5000 counts on any range. Since the internal full scale range of the MAX133/134 is greater than $\pm 49,000$ counts, at least $\pm 40,000$ counts of resolution are available after zero offset correction.

Each conversion result is latched into a Conversion Register which can be read by the microprocessor. The data format is nines complement BCD (a zero reading is 00000, a -1 reading is 99999, a -25000 reading is 75000). The nines complement form is the most convenient BCD format since the addition of the nines complement of a number is equivalent to subtracting that number. See "Software Notes" for simple BCD to binary conversion algorithms.

The last digit of conversion is used for digital autozero and is usually not displayed. Note that each count of the least significant digit of the MAX133/134 output corresponds to 1/10 of a count if a 4000 count full scale display is used. For current ranges with a voltage drop of only 200mV, the measured reading can be multiplied by two by using the X2 ("times 2") function of the MAX133/134. The X2 function reduces the R_{INT} resistor value by a factor of two during the Integrate phase. With the X2 range, a 200mV input voltage will result in a full scale, 4000.0 measured reading. Alternatively, the normal 400mV range can be used, with the multiplication by two being done by the microprocessor digitally. In this case, each count of the least significant digit is 1/5 of a displayed count. A 100mV full scale voltage drop can be achieved by using both the MAX133/134 X2 range and a digital times 2 multiplication in the microprocessor.

Each of the 20 conversions per second has a Zero Integrator phase to ensure rapid recovery from overload, and the MAX133/134 will recover to within 2 counts one conversion after an overload of 10 times full scale when the onboard active filter is not used.

Input Range Switching

In voltage measurement ranges other than 400mV, voltages are applied to the pin labeled 10M Ω through a 10M Ω resistor. By selecting the proper shunt resistors (1.1M Ω through 1K Ω) the input voltage will be attenuated to a 400mV range. The input attenuator switch section includes analog switches to switch both the input current and to sense the voltage on the shunt resistor. Other input switching functions select between the output of the input attenuator and the voltage developed across the current sensing resistors during current measurement. See Figure 1.

The 5pA input bias current of the MAX133/134 might result in unacceptable errors with a 10M Ω input resistor on the 400mV scale, so a separate pin with a 100k Ω to 1M Ω input resistor is used for the 400mV scale. The 10M Ω resistor used on the higher voltage ranges does not cause appreciable error since the input leakage current is shunted to ground through the 1.1M Ω to 1k Ω attenuator shunt resistors.

To avoid errors that might occur through coupling of high frequency, high voltage signals from the input of the attenuator to the low level 400mV and Current inputs, these two inputs have 10k Ω switches which connect them to Common whenever they are not selected.

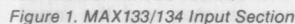
The input section also includes switches to allow an external AC-DC converter to be inserted into the signal path. Figure 10 shows a typical average-sensing RMS-calibrated AC-DC converter.

Ohms and Diode Measurement

The input attenuator resistors are also used as reference resistors in the ohms mode. Note that the 10M Ω resistor must be externally paralleled with the other resistors to get exactly 1M Ω , 100k Ω , etc. The ohms source buffer input is usually connected directly to the external bandgap reference or to another 1.25V source. In the 4k Ω through 40M Ω ranges there will be a total of 1.25V across the series combination of reference resistor, unknown resistor, and the input protection network; and the maximum voltage across the unknown resistor at full scale will be less than 400mV. On the 400 Ω range, the ohms voltage source is a diode connected to V^+ through a 2k Ω p-channel switch. With a 3V Common voltage, this supplies approximately 2.2V across the series combination of reference resistor, unknown resistor, and input protection network. This higher voltage is used on the 400 Ω range to compensate for the decrease in reference voltage caused by the input protection network. The MAX133/134 are designed to operate with PTC protection resistors of 2k Ω or less.

The voltage across the reference resistor is used as the reference voltage for the A/D when in the ohms mode, and the differential voltage between IN LO and IN HI is the input signal. The integration period is 500 counts, independent of the 50/60Hz control bit setting.

MAX133/MAX134


$$50000 \times \frac{R_{\text{UNKNOWN}}}{R_{\text{REF}}}$$

A 1k Ω reference resistor is used for the 400 Ω full scale, a 10k Ω reference for a 4k Ω full scale, etc. A 10M Ω reference resistor is used for both the 4M Ω full scale and the 40M Ω full scale. To get the correct results in the ohms measurement or R/2 mode, the conversion result must be multiplied by two either digitally by the microprocessor or by using the X2 range, except on the 40M Ω scale. The 40M Ω range has the same reference resistor as the 4M Ω range but a times 10 scale factor is obtained by not multiplying by 2, and by activating the $\div 5$ function. If the times 2

Since the input protection PTC resistor shown in Figure 2 reduces the reference and input voltage, particularly on the 400 Ω scale, the PTC resistance should be as low as is possible while maintaining the desired level of protection. Greater than 2k Ω PTC resistance will increase the noise level of measurements on the 400 Ω range.

3³/₄ Digit DMM Circuit

MAX133/MAX134

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Since the MAX133/134 does not use a reference capacitor, the only limit on the response time in the ohms mode is the active filter. Even when the active filter is turned off, $R_{FILTER1}$ is still connected, and the input voltage must charge the filter capacitors. This will generally be noticed only on the 4M Ω and 40M Ω ranges.

A diode test range can be implemented by simply connecting to V^+ the PTC used for input protection in the ohms ranges. The PTC then delivers approximately 1mA of current to the diode. The diode voltage can be measured either on the standard 4V scale, or on the 400mV scale with the $\div 5$ function activated to result in a 2V full scale. As always, the latched continuity circuit is active, and it will latch whenever the input voltage goes below approximately 100mV. The microprocessor can also test the measured voltage at the end of each conversion if a more precise detection of continuity threshold is desired.

Active Filter

The 2 pole active filter circuit is shown in Figure 3. The op amp's offset has no effect on the DC accuracy since the op amp is only AC coupled and the DC signal path is only through the passive 1M Ω resistor. Note that the active filter will limit the speed of response of the MAX133/134 to input voltage changes, and for that reason it may be desirable to disconnect the input filter during autoranging. Since the source impedance at the filter input varies with the input attenuator selected, the response time will be slower on the 4V range.

Oscillator and Beeper Driver

The MAX133/134 is designed to operate with a 32768Hz tuning fork crystal similar to the Statak

CX-1V, using only one external capacitor and no external resistors. If desired, the MAX133/134's OSC1 pin can be driven externally.

The 32kHz clock is used internally as the clock for the sequence and measurement counters. The 32kHz clock is also divided down to 2048Hz and 4096Hz for driving a beeper. The beeper output swings from V^+ to V^- and can directly drive piezoelectric beepers. Two control bits set by the microprocessor select the frequency (2048 or 4096 Hz) of the beeper and turn it on or off. Since the beeper is controlled by the microprocessor, it can be used for both continuity indication and for an audible operator feedback signal for peak hold or range changes.

Power Supply: Common, Digital Ground, Low Battery Detector

Both the MAX133 and MAX134 can operate from either a nominal 9V battery or a $\pm 5V$ supply. The maximum power supply current in DC voltage and DC current modes is 250 μA , with a typical operating current of 100 μA .

Analog Common is derived from a zener and is nominally 3.0V below V^+ . For lowest cost applications the Common voltage, with a tempco of 80ppm/ $^{\circ}C$, may be usable as a reference. In most applications, a bandgap reference will be connected to Common, with a pullup resistor to V^+ , and a voltage divider connected across the bandgap reference to generate the 545mV (60Hz operation) or 655 (50 Hz operation) reference voltage. In a battery powered meter, the Analog Common pin is used as the system ground reference point.

The MAX133 and MAX134 also generate a Digital Ground voltage, which is nominally 5V below V^+ ,

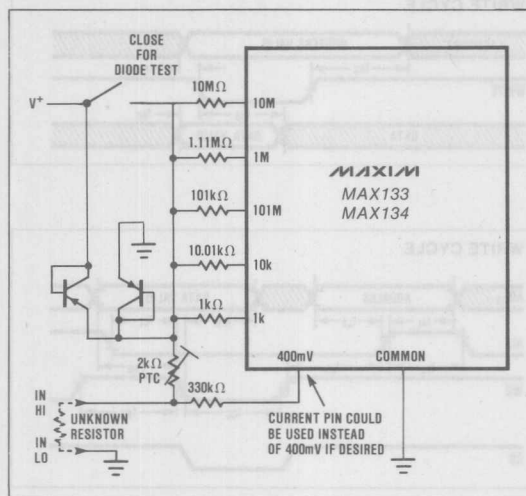


Figure 2. Ohms Mode and Diode Test

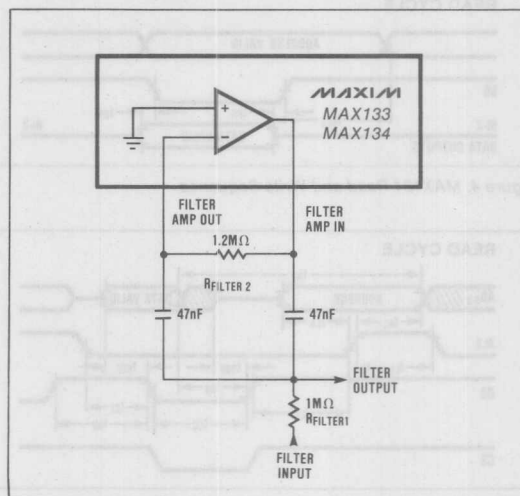


Figure 3. Active Filter

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and which will remain in the range of $5V \pm 10\%$ while sinking $5\mu A$ to $500\mu A$. The DGND generator has substantial current sinking capability, but can easily be pulled to a more negative voltage since the current sourcing capability is only $1\mu A$ typical. The MAX133 internally connects the Digital Ground generator to the DGND pin. Normally the MAX133 is powered by a 9V battery and the Ground, V^- , or V_{SS} pin of the microprocessor is connected to the MAX133 DGND pin.

The MAX134 connects the DGND voltage generator to the pin, DGND Out, and the MAX134 DGND pin is an input only. For use with 9V batteries, externally connect the MAX134 DGND Out pin to the MAX134 DGND pin. For use with external $\pm 5V$ power supplies, connect the DGND pin to ground, V^+ to $+5V$ and V^- to $-5V$.

The MAX133/134 has an onboard low battery detect circuit that will indicate when the battery voltage is approaching the minimum operating voltage of the MAX133/134, which is approximately 6.8V.

Digital Interface

The MAX133 and MAX134 differ only in their digital interface. The MAX133 has a multiplexed address and bidirectional data bus, while the MAX134 has 3 separate address lines in addition to a bidirectional data bus. In both products, the data bus has 4 bits, allowing the use of the MAX133/134 with both 4 bit and 8 bit microprocessors.

MAX134 Digital Interface

The digital interface between the MAX134 and the

controlling microprocessor is via a 4 bit bidirectional bus, D0-D3. In addition to the 4 data bus lines, there are 3 address lines and 2 control signals: A0-A2, WR, and RD.

The three address lines, A0-A2 select one of 5 control registers. When WR goes low, data will be written from the bus into the MAX134 control register addressed by A0-A2. When RD is low, the MAX134 will drive the bidirectional bus, placing on it the data contained in the results or status register addressed by the address inputs A0-A2. Figure 4 shows typical read and write sequences.

Digital Interface, MAX133

The MAX133 uses only 7 lines to interface with the microprocessor. The microprocessor first selects the register to be read or written to by placing the address of the register onto the 4 bit multiplexed address/data bus. The microprocessor then pulses the Address Latch Enable (ALE) line high to latch the register address into the MAX133. To read the selected register, the microprocessor then drives the Read line low, and the MAX133 places the register data onto the data bus. To write to the selected register the address is latched as described above, then the microprocessor places the data onto the bus and then pulses the Write line low. The MAX133 latches the data into the data into the selected register on the rising edge of Write. See Figure 5. The Chip Select (CS) line must be low to enable either the RD or WR lines, but ALE is not gated by CS.

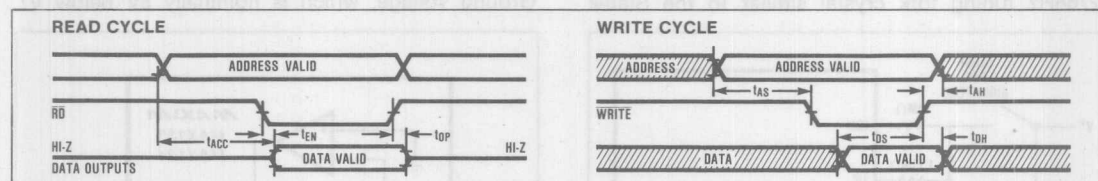


Figure 4. MAX134 Read and Write Sequence

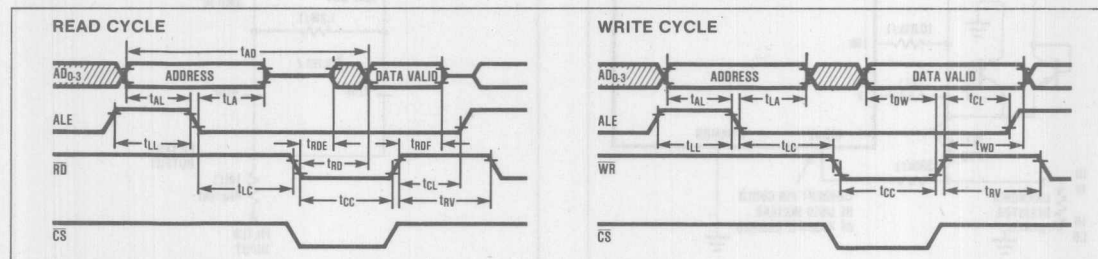


Figure 5. MAX133 Read and Write Sequence

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MAX133/MAX134

1

Digital Interface, MAX133 and MAX134

In most cases, the EOC signal will be either monitored by an I/O pin, or it will drive an Interrupt pin on the microprocessor. In battery powered systems, it may be desirable to put the microprocessor into a sleep or standby mode until EOC goes high. The microprocessor then performs any required data processing and display updates, then reenters the sleep mode. This conserves battery power since the microprocessor power consumption is minimized.

The data that has been latched in the MAX133/134 control registers does not immediately affect operation. The input registers are double buffered, and the control bits take effect during the 21st clock cycle after EOC goes high. In the hold mode, the double buffered registers are transparent, and any updates to the registers take effect immediately, as do any changes made during the one clock cycle period at the end of each conversion during which the second rank of buffers are being updated.

Description of Output Bits

The data format is nine's complement BCD. For example:

MEASUREMENT RESULT	BCD DATA
+40000	40000
—	—
+00100	00100
—	—
+00001	00001
+00000	00000
(there is NO -00000)	
-00001	99999
—	—
-00100	99900
—	—
-40000	60000

Table 2: Register Map of Output Data
From the MAX133/134 to the Microprocessor

ADDRESS OR REGISTER NUMBER	REGISTER NAME	REGISTER CONTENTS
0	Ones	Conversion Result BCD data for least significant digit (The undisplayed digit used for digital autozero)
1	Tens	BCD data of Conversion Result (Least significant displayed digit)
2	Hundreds	BCD Data of Conversion Result
3	Thousands	BCD Data of Conversion Result
4	10 Thousands	BCD Data of Conversion Result
5	Status	D3 D2 D1 D0 Always 1 Latched Continuity Holding Low Battery

The Latched Continuity bit will be high if the input voltage has gone below the continuity threshold of approximately 100mV since the last time the register was read. Each time this register (Register 5) is read, the continuity latch is reset.

The Low Battery bit is high whenever the battery voltage is below the low battery detect voltage.

The Holding bit is low whenever the MAX133/134 is in the hold state.

Description of Control Bits

Hold. A 1 in Hold will stop conversions at the end of the next conversion. If the MAX133/134 is in the Hold mode, a conversion will start on the next clock cycle after Hold is set to 0. The oscillator continues to run and all circuitry is active during the Hold mode.

High Frequency. A 1 in the High Frequency bit will select 4096Hz as the beeper frequency. A 0 will select 2048Hz.

Beeper On. A 1 turns on the beeper driver.

Sleep. A 1 in Sleep puts the MAX133/134 into the standby or sleep mode. The Common voltage buffer is turned off and the internal analog circuits are turned off, but the DGND circuitry is still active. The oscillator continues to run. Current consumption is reduced to 25 μ A. Several conversions must be performed after exiting the Sleep mode before full conversion accuracy is obtained.

10-0 through 10-4. These bits control the attenuator network switches. The 10-0 bit selects the 10M Ω input without activating any shunt resistors. This is an alternate 400mV input. The 10-1 bit activates the 10:1 attenuation by selecting the 10M Ω input and connecting the 1.11M Ω shunt. Similarly, 10-2, 10-3, and 10-4 bits selects input attenuation factors of 100, 1000, and 10,000 respectively. In the ohms mode these bits set the resistance range.

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**Table 3. Register Map of Input Data
From the Microprocessor to the MAX133/134**

ADDRESS OR REGISTER NUMBER	D3	D2	D1	D0
0	Hold	High Frequency	Beeper ON	Sleep
1	10-0	Filter Short	+5	50Hz
2	10-4	10-3	10-2	10-1
3	DC	Ext AC	Divider Sense	Ohms R/2
4	Current	X2	Read Zero	Filter On

BIT SET	VOLTAGE RANGE	OHMS RANGE
10-0	400mV	4M Ω and 40M Ω
10-1	4V	400k Ω
10-2	40V	40k Ω
10-3	400V	4k Ω
10-4	4000V	400 Ω

NOTE: The divider sense bit must also be set to enable the 10-0 through 10-4 bits.

50Hz. When set to 1 the integration period for voltage measurement is one cycle of the 50Hz power mains (655 clock cycles). When 0, the integration period is one 60Hz power line cycle (545 clock cycles).

X2. Setting the bit to 1 activates the MAX133/134 "times 2" function. When X2 is active, R_{INT2} only is used as the integrator resistor during the integration phase. R_{INT1} and R_{INT2} in series are used as the integration resistor for all deintegration phases and for the integration phase when X2 is 0. If R_{INT1} = R_{INT2} then setting the X2 bit doubles the digital output for a given input voltage.

+5. When this bit is set to a 1 the integration period is reduced by a factor of 5. This reduces the digital output code by a factor of 5, and allows a higher input voltage to be used. The full scale input voltage is multiplied by 5 when this bit is set, but caution should be used to make sure that the 2 μ A maximum recommended integrator output current is not exceeded, or the MAX133/134 linearity will be degraded.

Ohms or R/2. Setting this bit to a 1 selects the ohms measurement mode. See "Ohms and Diode Measurement" section above. Set the Divider Sense to 0 for ohms measurements.

Read Zero. Setting this bit to a 1 causes the next conversion to be a Read Zero conversion. A read zero conversion is performed with In Hi and In Lo internally shorted, and the reference selected by the other control bits is used. The read zero conversion result is proportional to the internal offsets of the MAX133/134, and this result should be subtracted from other measurements to get zero-corrected readings.

Filter On and Filter Short. These bits control the active filter. See Figures 1 and 3.

FILTER ON	FILTER SHORT	FUNCTION
1	0	Normal filter on condition
1	1	Filter on, R _{FILTER1} is bypassed. Use this bit combination to compensate for the higher source impedance of the 4V range.
0	1	Bypasses the Filter.
0	0	Invalid combination, do not use.

DC. This bit selects the DC mode when set to 1 and selects the AC mode when it is 0. This bit should also be set for ohms measurement.

External AC. This bit should be set to 1 whenever the AC mode is selected (DC=0).

Divider Sense. This bit, the 10-0 through 10-4, and the Current bits select the input signal source. Divider sense should be 1 whenever the input attenuator is selected. Set Divider Sense to 0 to select the 400mV input.

Current. Set divider sense to 0 and the Current bit to 1 to select the Current input. Note that while this bit and the associated pin are named "Current", the actual input is the voltage drop across an external current sensing resistor.

Component Selection

Integration Resistors

For an accurate times 2 multiplication in the X2 mode, the two R_{INT} resistors must be exactly equal. If the X2 mode is not needed, then connect a 604k Ω R_{INT1} between Buffer Out1 and the integration capacitor C_{INT}, and leave Buffer Out2 open. The value of both R_{INT1} and R_{INT2} is normally 301k Ω for a 545mV or 655mV reference. This sets the integrator output current to 2 μ A during the Deintegrate phase. resistors proportionately. Do not exceed 8 μ A integrator current.

Integration Capacitor

The normal value for the integration capacitor is 4.7nF. This value, in combination with the integrator output current and the clock frequency sets the integrator swing to about 3V for the voltage ranges when $R_{INT1} = R_{INT2} = 301k\Omega$ and the clock frequency is 32,768Hz. While the same integrator swing can be achieved with other values of capacitors by changing the value of R_{INT} , lower values of C_{INT} may introduce more noise through increased pickup of noise and 50/60Hz signals. Excessively high values of C_{INT} will also cause noise problems by reducing the integrator swing to unacceptably low values, causing the comparator noise to dominate the conversion errors. Large values of C_{INT} will also cause linearity errors since the settling time of the internal times 10 circuitry is affected by the value of C_{INT} .

The dielectric absorption of the integration capacitor directly affects the integral linearity, and high quality polypropylene capacitors are recommended. Polycarbonate and polystyrene capacitors may give satisfactory performance in less demanding applications, while the fourth choice, polyester (Mylar), will cause about 0.1% integral non-linearity.

Active Filter Components

The RC time constant of the active filter components sets the rolloff frequency of the filter. The effective value of the $R_{FILTER1}$ (Figure 3) is the sum of its value plus the source impedance driving the filter. In the 30V range for example, the effective source impedance is the 101k Ω resistor in the attenuator. In the 3V range, the effective source impedance is 1M Ω . This variable source impedance will alter the filter characteristics somewhat as the different voltage ranges are selected. The effect of the different source impedances can be minimized by increasing the value of the filter resistors while decreasing the value of the filter capacitors proportionately. This, however, will increase the offset error caused by the A/D input leakage current flowing through the filter resistors. For most applications, filter resistor values between 1M Ω and 3M Ω are optimal.

The RC time constant sets the filter rolloff frequency. A low rolloff frequency improves the normal mode rejection, but at the expense of a longer settling time in response to input voltage step changes. Another consideration when an LCD bargraph is used is aliasing. If the bargraph is updated at 20 times per second and there is a 19Hz component in the signal being measured, the beat frequency of 1Hz will appear on the LCD bargraph display. To avoid aliasing effects, the filter time constant is normally set to less than 10Hz. A 3Hz rolloff ($RC = 40ms$) further reduces the aliasing effects and increases normal mode rejection while still maintaining an acceptable transient response with fast varying signals.

Dielectric absorption in the filter capacitors will create a small, long time constant settling error; therefore polypropylene capacitors are recommended.

Crystal, and Crystal Oscillator Capacitor

The MAX133/134 oscillator is designed to use high Q, low power 32,768Hz crystals such as the Statek CX-1V. The series resistance should be less than 30k Ω .

The oscillator capacitor connected to OSC2 is typically 10pF, but should be adjusted to optimize performance with the chosen crystal. If overtone oscillations are observed, then increase the value of the oscillator capacitor. If on the other hand, the oscillator has start-up problems, then reduce or eliminate the oscillator capacitor. Keep the stray capacitance across the crystal to a minimum since excessive stray capacitance will prevent oscillation.

Attenuator Network

The attenuator network and the associated range selection switches are shown in Figure 1. If the resistance of the internal range selection switches were 0 Ω , then the theoretically ideal values for the attenuator network would be 10M Ω , 1.1111M Ω , 101.101k Ω , 10.01k Ω and 1.0001k Ω .

The voltage coefficient of the 10M Ω resistor should be as low as possible, since it will have high voltages applied to it in the 400V and 4,000V ranges. In addition, the temperature coefficients of the various attenuator resistors should be as low as practical since this affects the accuracy of the ohms measurements. The temperature coefficients of the attenuator resistors should track each other since the ratio of the resistor values sets the accuracy of the voltage measurements.

Input Attenuator Compensation Capacitors

The input attenuator is often compensated with low value capacitors to maintain a constant attenuation ratio over a wide bandwidth. The value of the compensation capacitors should be as low as practical, otherwise the 10M Ω pin will be driven above V^+ or below V^- when high frequency, high voltage signals are applied to the attenuator input, causing gross conversion errors.

Positive Temperature Coefficient Resistor (PTC)

As shown in Figure 2, a PTC is normally used as part of the protection circuit in the ohms mode. Excessive values of PTC resistance, however, reduce the voltage across the unknown and reference resistors, particularly on the 400 Ω range. PTC resistances above 2k Ω will degrade system performance by reducing the signal level on the 400 Ω range, thereby increasing the conversion noise. Values above 5k Ω will cause additional error since the voltage drop across the PTC appears at the A/D as a common mode difference between IN HI and Ref LO.

Microprocessors

For low cost 2 chip digital multimeters, 4 bit microprocessors with LCD display drive capability are

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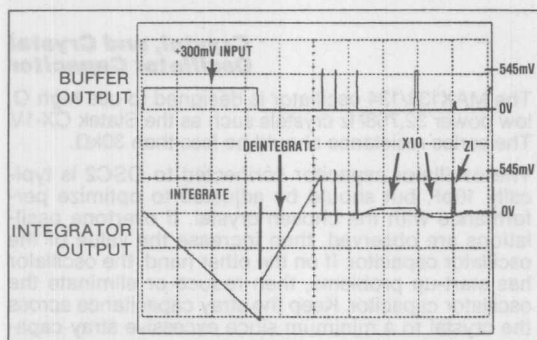


Figure 6. Buffer and Integrator Waveforms with Fullscale Positive Input Voltage

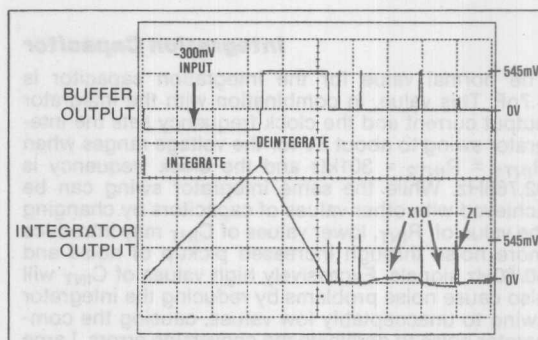


Figure 7. Buffer and Integrator Waveforms with Fullscale Negative Input Voltage

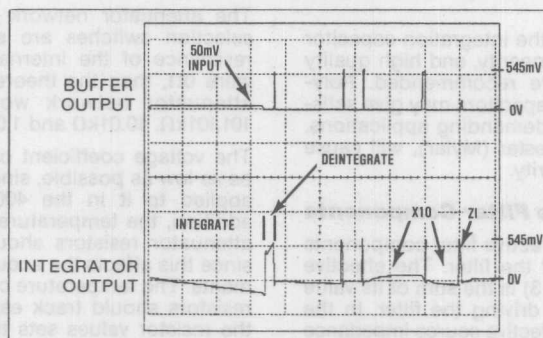


Figure 8. Buffer and Integrator Waveforms with a Small Positive Input Voltage

recommended. Typical 4 bit microprocessor families include the Sharp SM4 and SM5, the NEC μ PD75XX family, and the Hitachi LCD-III and LCD-IV families. If additional calculation power is needed, or if software development costs and time need to be minimized, then 8 bit microcontrollers such as the 8048, 8051 or 6803 should be used.

A/D Conversion Method and Timing

The MAX133/134 uses a "residue multiplication" technique to perform a $\pm 40,000$ count conversion in only 1638 clock cycles. Figures 6, 7 and 8 show typical integrator and buffer waveforms for a large positive, a large negative, and a small positive input voltage respectively.

Integration Phase

The unknown signal is integrated by connecting the non-inverting input of the integrator to IN LO, and the buffer input to IN HI. The integration period varies from 100 counts to 655 counts as shown in Table 5. The MAX133/134 is in the Zero Integration phase while in hold, between conversions, and before the start of the integration period.

Table 5. Integration Periods

MODE	INTEGRATION PERIOD (clock cycles)	
Voltage, 60Hz	545	(16.63ms)
Voltage, 50Hz	655	(19.99ms)
Voltage, 60Hz, $\div 5$	109	
Voltage, 50Hz, $\div 5$	131	
Ohms	500	
Ohms, $\div 5$	100	

$$\text{Digital Output Code} = \text{Integration Period} \times 100 \times \frac{V_{IN}}{V_{REF}}$$

where V_{IN} is the differential voltage applied to the A/D's internal IN HI and IN LO, and V_{REF} is the differential voltage applied to the A/D's internal REF HI and REF LO.

First Deintegration Phase

The polarity of the first Deintegrate phase is determined by polarity of the voltage on the integration capacitor at the end of the integration period. Figure 9 shows the MAX133/134 A/D section. Note that no reference capacitor is needed, thereby improving the response time in ohms measurement. Also note that since the non-inverting input of the integrator is connected to Ref Hi for a positive deintegration, the voltage at the integrator output will have a step voltage change equal to the reference voltage.

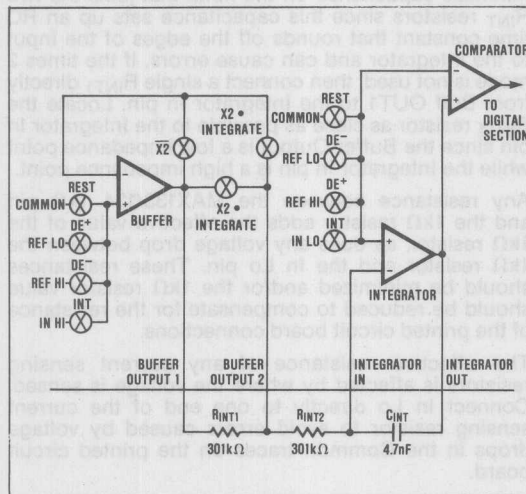


Figure 9. A/D Analog Section.

The first deintegration phase terminates when the comparator detects that the integration capacitor has been discharged. The MAX133/134 then goes into an "Idle" state where both the buffer input and the non-inverting input of the integrator are connected to common. This causes the system offset to be integrated.

Near the end of the maximum allowable deintegration period, the polarity of the voltage on the integration capacitor is again tested and either a positive or negative deintegration cycle occurs.

Times 10 (X10) Phase

When zero crossing is detected at the end of a deintegration phase the deintegration is continued until the next clock cycle. This causes the integrator to overshoot zero crossing slightly, leaving a small residual voltage on the integration capacitor. Any comparator delay causes an additional residual voltage on the integration capacitor. The times 10 phase inverts and multiplies this residual by a factor of 10.

Second Deintegration Phase

The second deintegration phase deintegrates the residual voltage on the integration capacitor that has been inverted and multiplied by 10 in the X10 phase. Note that, since the voltage across the integration capacitor has been multiplied by 10, each clock cycle of deintegration during the second deintegration corresponds to 1/10 of one clock cycle during the first deintegration.

Second X10 and Third Deintegration

The residual voltage left on the integration capacitor after the second deintegrate phase is multiplied by the second X10 phase, and this multiplied residual is deintegrated in the third deintegration phase. Since the residual voltage on the integration capacitor has twice been multiplied by 10, the third deintegration phase has 100 times finer resolution than does the first deintegration phase.

Sequence Counter and Results Counter

The sequencing or timing of the various conversion phases are controlled by a binary sequence counter. This counter counts upward continuously except during the hold mode. Some phases, such as the integration periods, are both started and stopped at preset counts. The deintegration phases are started at predetermined counts, but are terminated when the comparator detects zero crossing at the integrator output.

The results counter accumulates counts during all deintegration phases. It is an up/down BCD counter, with the count direction being determined by the deintegration polarity. The first deintegration phase causes the results counter to count by hundreds. Since the second deintegration phase is deintegrating a residual voltage that has been multiplied by 10, the results counter is incremented or decremented by tens during the second deintegration phase. The results counter is incremented or decremented by ones during the third deintegration phase. The content of the results counter is transferred to the results register at the end of each conversion.

Application Notes

Sleep and Hold Mode

The Hold mode stops the internal sequence counter at the end of the next conversion but does not turn off the oscillator or any analog circuitry. The Hold mode can be used to speed up autoranging — see "Autoranging", below. Dielectric absorption in the integration capacitor will cause the first two or three readings after an extended Hold period to have a lower magnitude than the steady state reading.

The Sleep mode puts the MAX133/134 into a low power quiescent mode by shutting off all analog circuitry except the DGND power supply and the oscillator. A typical use of the Sleep mode is to reduce power consumption by turning off the MAX133/134 if the meter is idle for a long period. A

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typical method of detecting when the meter is no longer being used is to detect when the reading stays constant and there are no operator inputs such as range or mode changes for an extended period.

Since the Sleep mode turns off all analog circuitry, the first conversion after coming out of the sleep mode is not valid. It will take several readings before the reading has stabilized to within 1 count.

Input Protection for Digital Multimeters

Figure 2 shows a typical multimeter input circuit for ohms measurement. The positive temperature coefficient (PTC) thermistor normally has a resistance of only 2k Ω , but under overload conditions it limits the fault current since the fault current heats the PTC, thereby increasing its resistance several orders of magnitude. Protection on the voltage ranges is automatic, since the 10M Ω input resistor will limit the input current to safe limits, even with 4000V applied. Current ranges must be protected with fuses or circuit breakers, and the current sense resistors should be bypassed with diodes to limit the voltage drop across the current sense resistors to no more than 2 diode drops.

External AC-DC Converter

Figure 10 shows a typical half wave external AC-DC converter. This circuit is an average-sensing, RMS-calibrated AC-DC converter. This means that the output is proportional to the average AC value rather than the RMS value, but that the output has been multiplied by the 1.11 to correct for the ratio of the average voltage to the RMS voltage of a sine wave. If desired, a true RMS to DC converter can be connected between Ext AC Out and Ext AC In.

Printed Circuit Board Layout

Since the integrator output makes common mode voltage steps equal to the reference voltage to perform a positive deintegration, any stray capacitance on the integration capacitor will cause errors. Stray capacitive loading on the Buffer output should also be minimized to avoid ringing on the buffer output.

The Integrator In node is particularly sensitive to stray pickup of noise and 50/60Hz, therefore C_{INT} should be located as near as possible to the Integrator In pin.

Minimize capacitance on the node that joins the two R_{INT} resistors since this capacitance sets up an RC time constant that rounds off the edges of the input to the integrator and can cause errors. If the times 2 mode is not used, then connect a single R_{INT1} directly from Buff OUT1 to the Integrator In pin. Locate the R_{INT1} resistor as close as possible to the Integrator In pin since the Buffer Output is a low impedance point while the Integrator In pin is a high impedance point.

Any resistance between the MAX133/134 1k Ω pin and the 1k Ω resistor adds the effective value of the 1k Ω resistor, as does any voltage drop between the 1k Ω resistor and the In Lo pin. These resistances should be minimized and/or the 1k Ω resistor value should be reduced to compensate for the resistance of the printed circuit board connections.

The effective resistance of any current sensing resistors is affected by where the voltage is sensed. Connect In Lo directly to one end of the current sensing resistor to avoid errors caused by voltage drops in the Common traces on the printed circuit board.

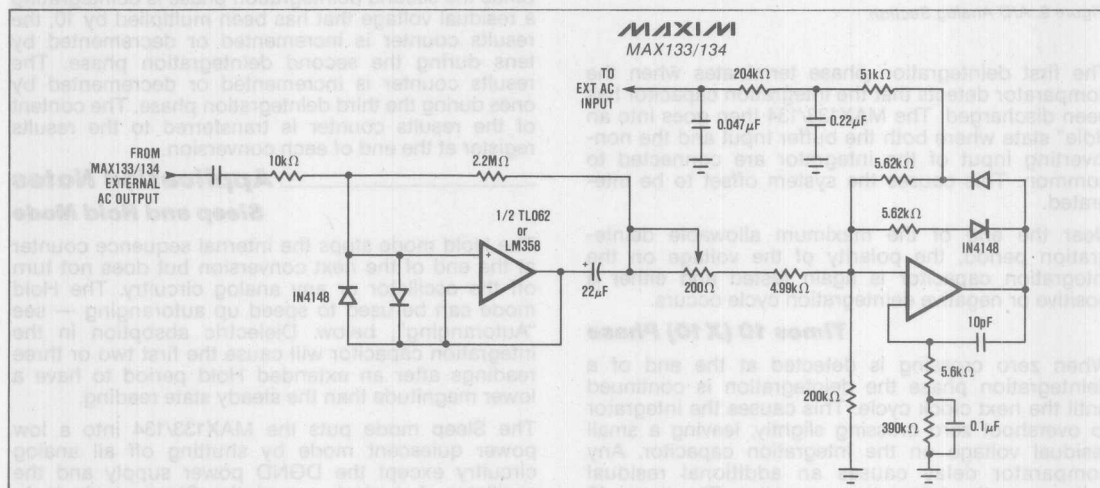


Figure 10. External AC-DC Converter.

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MAX133/MAX134

Software Notes Autoranging

The sequence in which the registers are loaded has no effect provided that all registers are loaded before the next end of conversion. Control bits take effect only when the MAX133/134 is in Hold or completes the current conversion. If the MAX133/134 runs continuously, the autoranging sequence will be as

shown in Figure 11A. If the MAX133/134 is put into the hold mode during autoranging the autoranging time can be reduced in those cases where several ranges must be tried. See Figure 11B. A simple test that detects most overrange readings is to check if the two most significant digits (Registers 3 and 4) are greater than ± 45 . A second test of the zero-corrected reading should also be performed to make sure that it is within the desired full scale range.

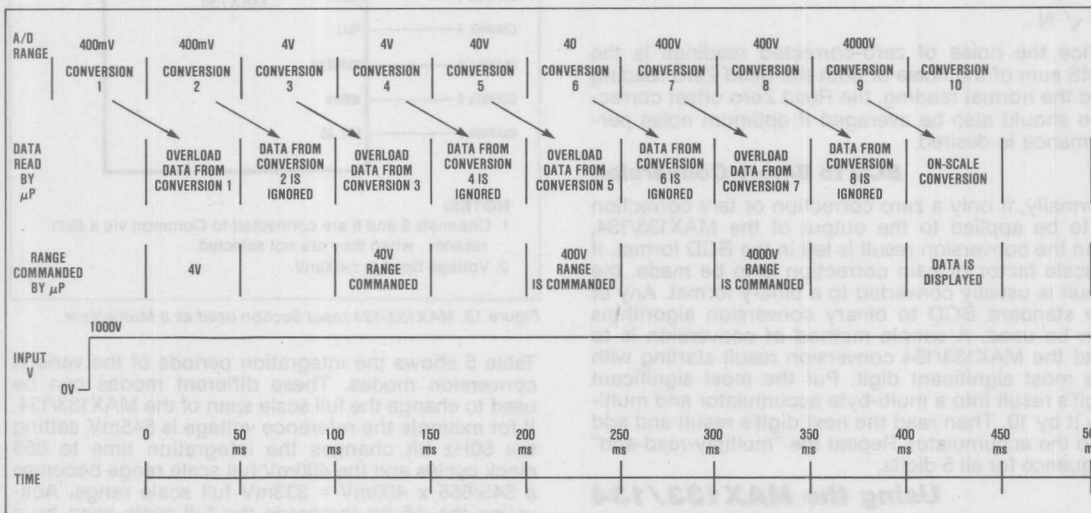


Figure 11a. Autoranging with MAX133/134 Running Continuously

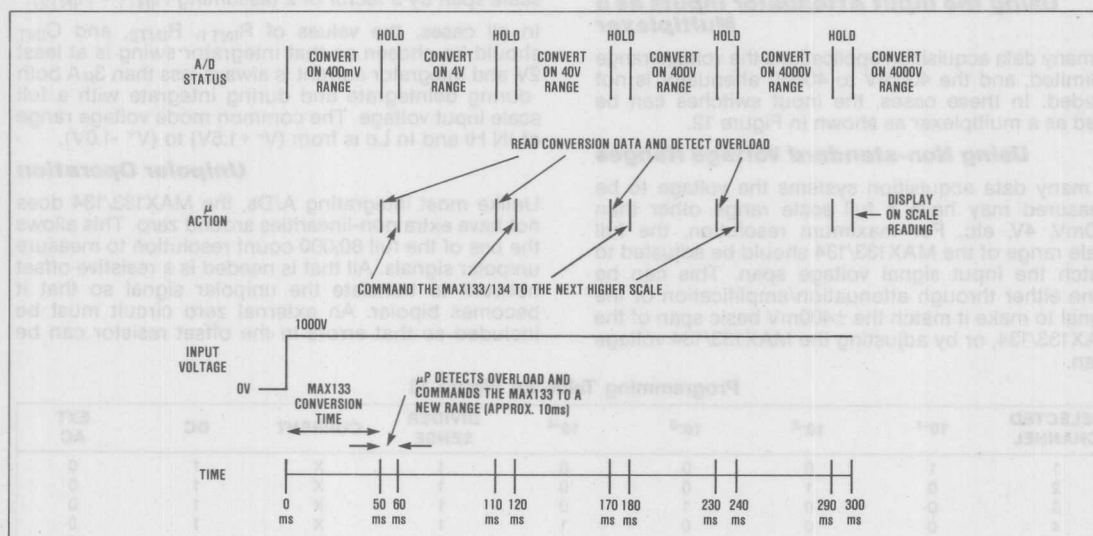


Figure 11b. Autoranging With Hold Between Conversions

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Reduction of Conversion Noise by Averaging Readings

The MAX133/134 has approximately ± 1 counts of noise. In most cases where only 4000 counts are being displayed, averaging is not required since the noise is only 1/10 of one displayed count. In data acquisition systems where the full resolution is being used, averaging N readings will reduce the noise by a factor of

$$\sqrt{N}.$$

Since the noise of zero-corrected readings is the RMS sum of the noise of both the Read Zero reading and the normal reading, the Read Zero offset correction should also be averaged if optimum noise performance is desired.

BCD to Binary Conversion

Normally, if only a zero correction or tare correction is to be applied to the output of the MAX133/134, then the conversion result is left in the BCD format. If a scale factor or gain correction is to be made, the result is usually converted to a binary format. Any of the standard BCD to binary conversion algorithms can be used. A simple method of conversion is to read the MAX133/134 conversion result starting with the most significant digit. Put the most significant digit's result into a multi-byte accumulator and multiply it by 10. Then read the next digit's result and add it to the accumulator. Repeat the "multiply-read-add" sequence for all 5 digits.

Using the MAX133/134 in Data Acquisition Systems

Using the Input Attenuator Inputs as a Multiplexer

In many data acquisition applications the voltage range is limited, and the 400mV to 4000V attenuator is not needed. In these cases, the input switches can be used as a multiplexer as shown in Figure 12.

Using Non-standard Voltage Ranges

In many data acquisition systems the voltage to be measured may have a full scale range other than 400mV, 4V, etc. For maximum resolution, the full scale range of the MAX133/134 should be adjusted to match the input signal voltage span. This can be done either through attenuation/amplification of the signal to make it match the ± 400 mV basic span of the MAX133/134, or by adjusting the MAX133/134 voltage span.

Programming Table for Figure 13

SELECTED CHANNEL	10 ⁻¹	10 ⁻²	10 ⁻³	10 ⁻⁴	DIVIDER SENSE	CURRENT	DC	EXT AC
1	1	0	0	0	1	X	1	0
2	0	1	0	0	1	X	1	0
3	0	0	1	0	1	X	1	0
4	0	0	0	1	1	X	1	0
5	0	0	0	0	0	1	1	0
6	0	0	0	0	0	0	1	0
7	0	0	0	0	X	X	0	1

0 = set to 0 1 = set to 1 X = Don't Care

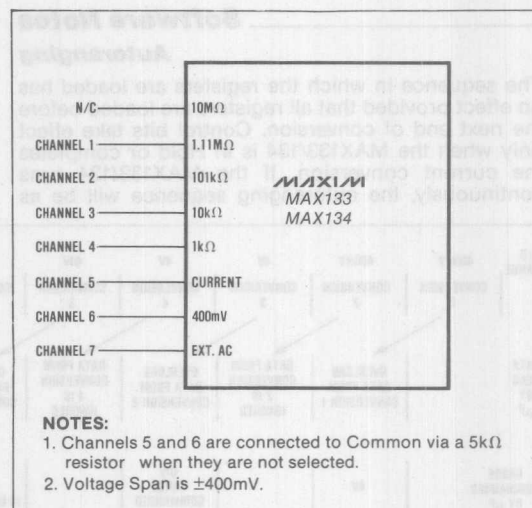


Figure 12. MAX133/134 Input Section used as a Multiplexer.

Table 5 shows the integration periods of the various conversion modes. These different modes can be used to change the full scale span of the MAX133/134. If for example the reference voltage is 545mV, setting the 50Hz bit changes the integration time to 655 clock cycles and the 400mV full scale range becomes a $545/655 \times 400$ mV = 333mV full scale range. Activating the $\div 5$ bit increases the full scale span by a factor of 5, while setting the X2 bit decreases the full scale span by a factor of 2 (assuming $R_{INT1} = R_{INT2}$).

In all cases, the values of R_{INT1} , R_{INT2} , and C_{INT} should be chosen so that integrator swing is at least 2V, and integrator current is always less than 3μ A both during deintegrate and during integrate with a full scale input voltage. The common mode voltage range of IN Hi and IN Lo is from ($V^- + 1.5$ V) to ($V^+ - 1.0$ V).

Unipolar Operation

Unlike most integrating A/Ds, the MAX133/134 does not have extra non-linearities around zero. This allows the use of the full 80,000 count resolution to measure unipolar signals. All that is needed is a resistive offset network to translate the unipolar signal so that it becomes bipolar. An external zero circuit must be included so that errors in the offset resistor can be

3 $\frac{3}{4}$ Digit DMM Circuit

MAX133/MAX134

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measured and subtracted. Note that the zero correction software is the same as would be used to correct for the internal zero error of the MAX133/134, except that in this case the external zero offset will be nearly 40,000 counts.

Ratiometric Measurements of Load Cell and Strain Gauges

In many weigh scale, pressure transducer, and load cell applications ratiometric measurements are desired. If the reference voltage is referenced to the ground or Common pin, then simply connect the reference voltage to the Ref In pin, connect the voltage to be measured to In Hi and In Lo and perform any of the voltage mode conversions. If, on the other hand, the reference voltage is a differential signal, use the circuit of Figure 13 and select the ohms measurement mode. Note that the non-inverting input of the integrator will be connected to either Ref Lo or REF HI during deintegration. The integrator swing should be reduced if the integrator output goes within 0.5V of either V⁺ or V⁻. In no case should either Ref Hi or Ref Lo be lower than (V⁻ + 1.5V) or higher than (V⁺ - 1.0V).

Operation with Clock Frequencies Other Than 32,768Hz

Operation with clock frequencies lower than 32kHz slightly improves the noise performance, while at the same time reducing the reading rate proportionately. With clock frequencies less than 10kHz, leakages during the X10 phase will introduce differential linearity errors at high temperatures.

Clock frequencies higher than 50kHz are not recommended since the X10 period will not completely settle within its allotted time period, causing differential nonlinearity errors. Another potential problem at very high clock frequencies is that, although the comparator delay is a fixed time period, it increases in terms of clock cycles as the clock frequency increases. At very high clock frequencies the residue cannot be fully deintegrated in the allotted number of clock cycles after having been multiplied by 10 in the X10 phase.

When using a clock frequency other than 32,768Hz, change the value of the integration capacitor C_{INT} to keep integrator swing at approximately 2V.

Converting the Times 2 Mode to a $\pm 40\text{mV}$ Full Scale Range

The sensitivity of the times two mode is increased by the factor

$$\frac{R_{\text{INT1}} + R_{\text{INT2}}}{R_{\text{INT2}}}$$

In the normal DMM application $R_{\text{INT1}} = R_{\text{INT2}}$ and the X2 mode increases the sensitivity of the MAX133/134 by a factor of 2. If the two resistors have a 9 to 1 ratio, the X2 bit will increase the sensitivity of the MAX133/134 by a factor of 10. This can be used to get 1 μ V resolution on a 40mV scale.

Disabling the Active Filter

Since the signal source impedance in many data acquisition systems is very low, the value of the filter resistors, R_{FILTER1} and R_{FILTER2}, can be lowered to reduce the error caused by the leakage current of the A/D flowing through R_{FILTER1}. If rapid settling is needed in a multichannel data acquisition system, then the filter should be disabled by leaving the pins Filter Resistor In and Filter Resistor Out open, and shorting Filter Amp Out to Filter Amp In. Do not leave the filter amplifier connection open circuited, since oscillations may occur.

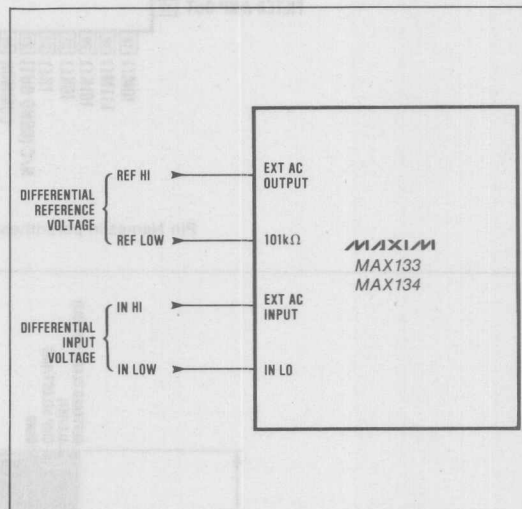


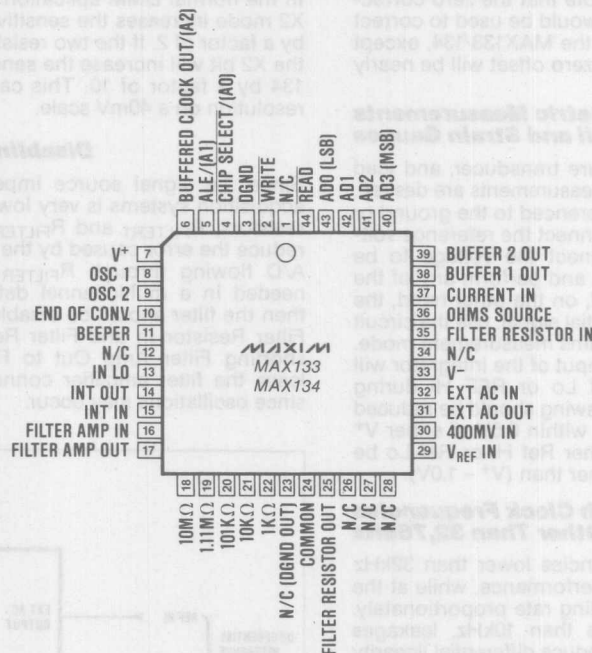
Figure 13. Configuration for Differential Reference Input.

BIT PATTERN					
10 ⁻⁰ TO 10 ⁻⁴	R/2	DIVIDER SENSE	CURRENT	DC	EXT AC
0	1	1	0	0	1

3 3/4 Digit DMM Circuit

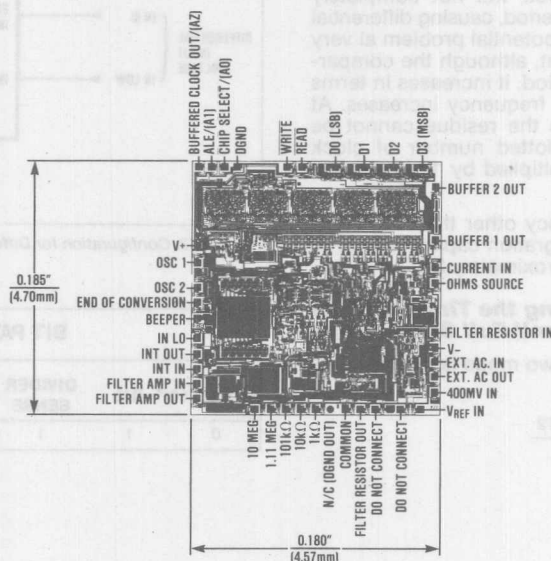
Pin Configuration

TOP VIEW



Pin Names in parentheses are for MAX134 only.

Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

General Description

The MAX138 and MAX139 are 3½ digit A/D converters with onboard LCD (MAX138) and LED (MAX139) display drivers. The MAX138 and MAX139 also contain a charge pump voltage inverter. The charge pump inverter allows the MAX138/139 to measure both positive and negative input voltages while operating from a single power supply voltage from +2.5V to +7V. The operating circuits of the MAX138 and MAX139 are similar to those of the ICL7136 and ICL7137 respectively, except that the MAX138/139 have an internal oscillator, and an external charge pump capacitor is connected to pins 38 and 40.

MAX140 is a low segment current version of MAX139 intended for use with low current LED displays.

Features

- ◆ Single Supply +2.5V to +7.0V Operation
- ◆ Measures Both Positive and Negative Input Voltages
- ◆ Charge Pump Voltage Inverter Generates a Negative Supply Voltage
- ◆ Internal Bandgap Reference
- ◆ Onboard Display Driver
- ◆ Low Segment Current (MAX140)

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX138CPL	0°C to +70°C	40 Lead Plastic DIP
MAX138CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX138C/D	0°C to +70°C	Dice
MAX138EPL	-40°C to +85°C	40 Lead Plastic DIP
MAX138EQH	-40°C to +85°C	44 Lead Plastic Chip Carrier
MAX139CPL	0°C to +70°C	40 Lead Plastic DIP
MAX139CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX139C/D	0°C to +70°C	Dice
MAX139EPL	-40°C to +85°C	40 Lead Plastic DIP
MAX139EQH	-40°C to +85°C	44 Lead Plastic Chip Carrier
MAX140CPL	0°C to +70°C	40 Lead Plastic DIP
MAX140CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX140C/D	0°C to +70°C	Dice
MAX140EPL	-40°C to +85°C	40 Lead Plastic DIP
MAX140EQH	-40°C to +85°C	44 Lead Plastic Chip Carrier

Applications

+5V Powered Panel Meters

+3V Powered DMMs

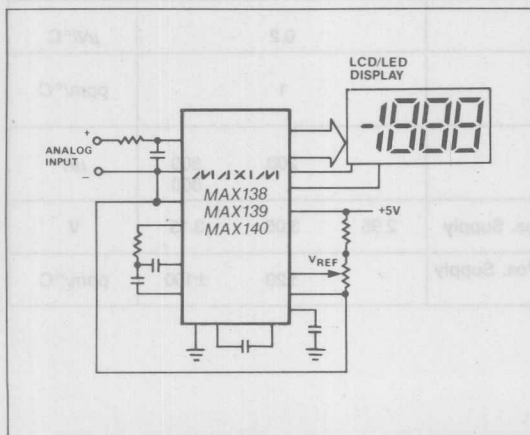
Instruments

Portable Monitors

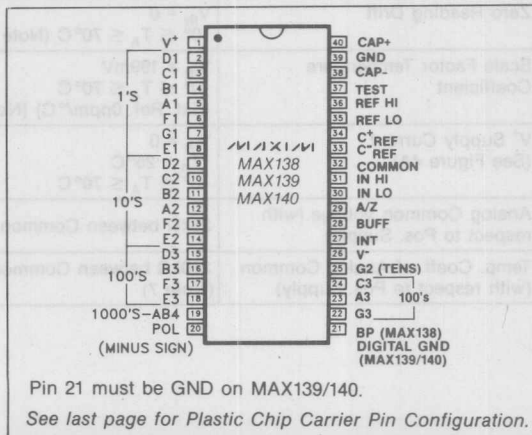
Weigh Scales

Digital Thermometers

Typical Operating Circuit



Pin Configuration



MAX138/139/140

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MAXIM

Maxim Integrated Products 1-19

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3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to GND)	7.5V
Supply Voltage (V^+ to GND)	
MAX138	+7.5V
MAX139, MAX140	+6.0V
Analog Input Voltage (either input) (Note 2)	V^+ to V^-
Reference Input Voltage (either input)	V^+ to V^-
Power Dissipation (Note 3)	
CERDIP Package	1000mW
Plastic Package	1142mW
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Note 1: V^- is generated on the device and is equal to V^+ but opposite in polarity.

Note 2: Input voltages may exceed the supply voltages, provided the input current is limited to $\pm 1\text{mA}$.

Note 3: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS (MAX138, MAX139, MAX140)

($V^+ = +5\text{V}$, $T_A = +25^\circ\text{C}$, test circuit—Figure 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	$V_{IN} = 0.0\text{V}$, Full Scale = 200mV $T_A = 25^\circ\text{C}$ (Note 4) $0^\circ \leq T_A \leq 70^\circ\text{C}$ (Note 5)	-000.0 -000.0	± 000.0 ± 000.0	+000.0 +000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, $V_{REF} = 100\text{mV}$ $T_A = 25^\circ\text{C}$ (Note 4) $0^\circ \leq T_A \leq 70^\circ\text{C}$ (Note 5)	999 998	999/1000 999/1000	1000 1001	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \cong 200\text{mV}$ $T_A = 25^\circ\text{C}$ (Note 4) $0^\circ \leq T_A \leq 70^\circ\text{C}$ (Note 5)	-1	± 0.2 ± 0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or full scale = 2.000V (Note 6)	-1	± 0.2	+1	Counts
Common Mode Rejection Ratio	$V_{CM} = \pm 1\text{V}$, $V_{IN} = 0\text{V}$ Full Scale = 200mV		50		$\mu\text{V/V}$
Noise (Pk-Pk value not exceeded 95% of time)	$V_{IN} = 0\text{V}$ Full Scale = 200mV		15		μV
Input Leakage Current	$V_{IN} = 0$ $T_A = 25^\circ\text{C}$ (Note 4) $0^\circ \leq T_A \leq 70^\circ\text{C}$		1 20	10 200	pA
Zero Reading Drift	$V_{IN} = 0$ $0^\circ \leq T_A \leq 70^\circ\text{C}$ (Note 4)		0.2		$\mu\text{V}/^\circ\text{C}$
Scale Factor Temperature Coefficient	$V_{IN} = 199\text{mV}$ $0^\circ \leq T_A \leq 70^\circ\text{C}$ (Ext. Ref. 0ppm/ $^\circ\text{C}$) (Note 4)		1		ppm/ $^\circ\text{C}$
V^+ Supply Current (See Figure 4A)	$V_{IN} = 0$ $T_A = 25^\circ\text{C}$ $0^\circ \leq T_A \leq 70^\circ\text{C}$		200	500 800	μA
Analog Common Voltage (with respect to Pos. Supply)	25k Ω between Common & Pos. Supply	2.95	3.05	3.15	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250k Ω between Common & Pos. Supply (Note 7)		± 20	± 100	ppm/ $^\circ\text{C}$

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

ELECTRICAL CHARACTERISTICS (MAX138)

(V⁺ = +5V, T_A = +25°C; test circuit—Figure 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Pk-Pk Segment Drive Voltage		4	5	6	V
Pk-Pk Backplane Drive Voltage					
Test Pin Voltage	With Respect to V ⁺	4	5	6	V

ELECTRICAL CHARACTERISTICS (MAX139, MAX140)

(V⁺ = +5V, T_A = +25°C; test circuit—Figure 2)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Segment Drive Current	MAX139	Except Pin 19	5	9	15	mA
		Pin 19	10	18	30	
	MAX140	Except Pin 19	1.5	2.5	4	mA
		Pin 19	3	5	8	

Note 4: Test condition is V_{IN} applied between pin IN HI and IN LO through a 1MΩ series resistor as shown in Figures 1 and 2.

Note 5: 1MΩ resistor is removed in Figures 1 and 2.

Note 6: Guaranteed by design.

Note 7: Sample tested to ensure compliance.

Basic Applications

Figures 1 and 2 show the typical operating circuit for the MAX138/139/140 when powered by a single +5V supply.

Compatibility with ICL7106, ICL7136 and ICL7137

The MAX138/139/140 can replace the ICL7106/ICL7136 and ICL7137 with minor circuit and component value changes. The ICL7106/36/37 oscillator components are not used, and are replaced with a 1μF capacitor connected between pins 38 and 40. There must be a 1μF filter capacitor connected to V⁻. The filter capacitor can be connected between either V⁻ and GND or V⁻ and V⁺.

System Reference Point

The analog block diagram of the MAX138/139 is shown in Figure 3. The MAX138/139 use the IN LO pin as the reference point for the integrator.

The circuit configuration of the MAX138/139 results in a superior 120dB rejection of common mode voltages applied to IN HI and IN LO. The MAX138/139 configuration, though, does not have good rejection of AC noise on the IN LO pin during de-integration. If an AC-DC converter is used with a MAX138/139, it should either be a half-wave circuit or should have adequate filtering to avoid inducing additional noise.

Detailed Description

Conversion Method

The MAX138/139/140 use the dual-slope integration method of conversion, with the addition of an auto-zero phase to compensate for the offset of the buffer and integrator, and the addition of a zero integrator phase to ensure rapid recovery from an overrange

conversion. Refer to the ICL7106 data sheet for a detailed description of the conversion phases and timing.

The conversion result is 1000 × (IN HI-IN LO)/(REF HI-REF LO), with a maximum conversion result of ±1999. If the input voltage is greater than full scale, the MAX138/139/140 will blank the lower three digits, and will display the leading "1" digit and, if the input voltage is negative, will also turn on the Minus segment.

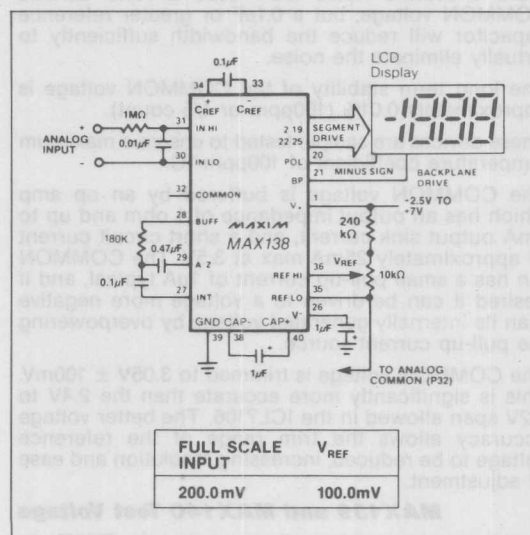


Figure 1. MAX138 Typical Operating Circuit

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

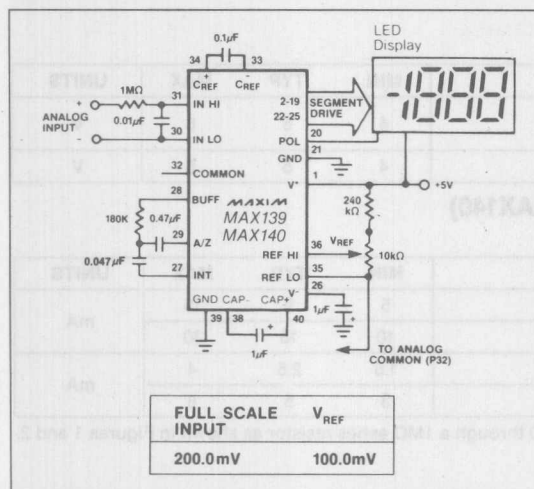


Figure 2. MAX139/MAX140 Typical Operating Circuit

Common Pin Voltage Reference

The COMMON voltage is derived from a bandgap reference, unlike earlier devices which derive the COMMON voltage from a zener. The bandgap reference eliminates the excessive long term drift associated with low current zeners, and the MAX138/139/140 can be a source of a high quality reference voltage without the use of external bandgap reference diodes. The COMMON voltage does have slightly more wideband noise than does a zener-derived COMMON voltage, but a 0.1μF or greater reference capacitor will reduce the bandwidth sufficiently to virtually eliminate the noise.

The long term stability of the COMMON voltage is approximately 0.01% (100ppm or 1/5 count).

These devices are sample tested to ensure a maximum temperature coefficient of 100ppm/°C.

The COMMON voltage is buffered by an op amp which has an output impedance of 1 ohm and up to 2mA output sink current, and a short circuit current of approximately 25mA max at 3.5V. The COMMON pin has a small pull-up current of 1μA typical, and if desired it can be driven to a voltage more negative than its internally generated voltage by overpowering the pull-up current source.

The COMMON voltage is trimmed to 3.05V ± 100mV. This is significantly more accurate than the 2.4V to 3.2V span allowed in the ICL7106. The better voltage accuracy allows the trim range of the reference voltage to be reduced, increasing resolution and ease of adjustment.

MAX139 and MAX140 Test Voltage

This internal test voltage is coupled to the TEST pin via a 500 ohm resistor. When this pin is pulled high, all segments are turned on.

Oscillator

The MAX138/139/140 oscillator circuit uses no external components. It is trimmed during production to 40kHz nominal. This results in a conversion rate of approximately 2.5 conversions per second. The typical characteristics graph (Figure 4B) shows the variation with changes in supply voltage.

In Lo and In Hi Differential Inputs

These A/D converters measure the differential voltage between IN LO and IN HI. The typical common mode rejection ratio (CMRR) is 120dB.

IN HI has a guaranteed maximum input leakage current of only 10pA, and can be directly driven by high source impedances such as pH sensors and by the 10 Megohm input impedance attenuators normally used in digital multimeters. Both IN HI and IN LO have protection clamp diodes to V⁺ and V⁻. If the input voltage can go above V⁺ or below V⁻, then the input currents should be limited to less than 1mA to prevent damage to the A/D.

The MAX138/139/140 common mode voltage range for IN HI and IN LO is a minimum of ±1V around COMMON. Under some circumstances, IN HI and IN LO can range from V⁺ + 1.5V to V⁺ - 1.5V. See "Common Mode Voltage Range Considerations" section of the Application Notes for further information.

Reference and C_{REF} Pins

As shown in the analog block diagram, Figure 3, REF HI and REF LO are connected to the C_{REF} pins during autozero and zero integrate phases via analog switches. This charges an external reference capacitor, which is then used as either a positive or a negative reference voltage as needed during the de-integration phase. The common mode voltage range (CMVR) of REF HI and REF LO is V⁺ to V⁻—any voltage between V⁺ and V⁻ can be used to drive the REF HI and REF LO inputs. The differential voltage between REF HI and REF LO sets the full scale voltage. A full scale output of ±1999 counts occurs with an input voltage of ±1.999 times the differential voltage between REF HI and REF LO. If the differential reference voltage is 1.0V the full scale input voltage is 1.999V. With 100mV reference the full scale input voltage is 199.9mV.

LCD Display Driver Outputs

The MAX138 LCD display driver outputs swing from V⁺ to GND at a frequency of 20 times the conversion rate. The output impedance is approximately 3k ohms. The LCD display driver outputs are non-multiplexed or direct drive, and drive in-phase with the backplane output to turn an LCD segment off and drive 180° out of phase with the backplane output to turn an LCD segment on.

The BP or backplane output has an output impedance of 500Ω. The LCD drive waveforms are 50% duty cycle with matched rise and fall times to minimize the DC component across the LCD display.

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

MAX138/139/140

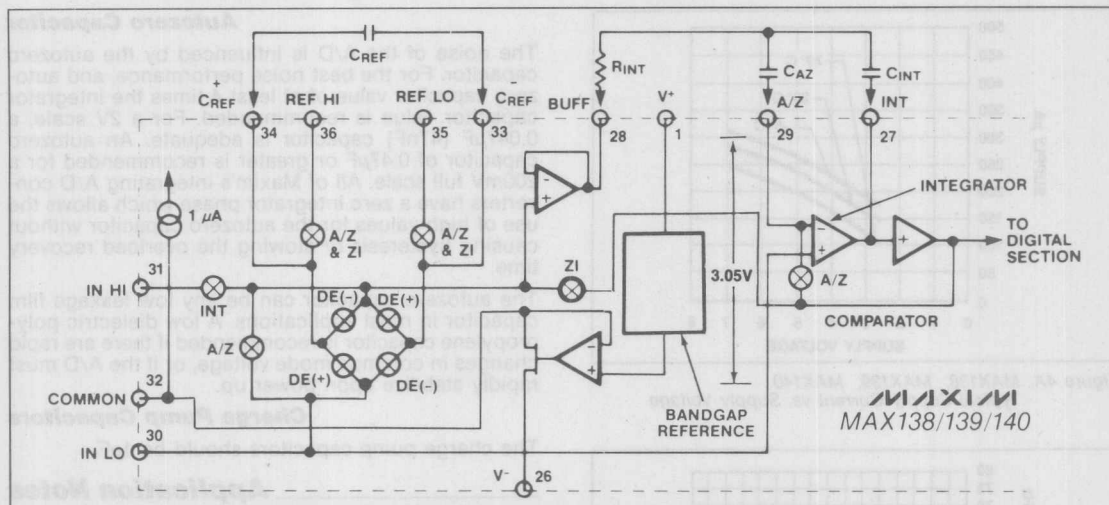


Figure 3. Analog Section of MAX138, MAX139, and MAX140

The MAX139/140 LED display driver outputs are N-Channel current sinks with output current vs. voltage characteristics as shown in the typical characteristics graphs.

Component Selection

Integrator Resistor, R_{INT}

The MAX138/139/140 integrator and buffer amplifiers have a class A output stage which can deliver up to $4\mu\text{A}$ with high linearity. Normally, the MAX138/139/140 integrator resistor is chosen to set the maximum current to $1.1\mu\text{A}$ by setting its value to $2 \times V_{REF}/1.1\mu\text{A}$. For a 1V reference the correct value is $1.8\text{M}\Omega$. For a 100mV reference the correct value is $180\text{k}\Omega$. Since the absolute value of R_{INT} does not affect the conversion accuracy, the type of resistor used for R_{INT} is not critical.

Integrator Capacitor

The integrator capacitor is normally polypropylene, which has low dielectric absorption. Dielectric absorption will cause integral linearity errors. For example, if polyester or Mylar is used, the measured value of inputs near full scale will be approximately 0.1% lower than expected, while the measured value of low input voltages will be as expected.

Proper selection of the integrator capacitor value can be verified by monitoring the output swing of the integrator with \pm full scale input voltages. In a properly operating circuit, \pm full scale input voltages will cause the integrator output (INT pin) to swing to about $\pm 2\text{V}$. The integrator output can drive to about 0.3V from either supply while maintaining high linearity.

If the value of the integrator capacitor or integrator resistor is too low, \pm full scale inputs will cause the integrator to saturate as it attempts to drive above V^+

or below V^- . If this occurs, operation will appear normal for low input voltages, but the conversion results for higher output voltages will be less than full scale.

Very low integrator swing will increase the amount of noise or "flicker" of the conversions. A full scale integrator swing of $\pm 1\text{V}$ is sufficient to avoid any significant degradation of the noise performance, and should be used for operation with a 2.5V supply.

Reference Capacitor

For most circuits a reference capacitor value of $0.1\mu\text{F}$ is adequate. However, a larger value is needed to prevent rollover error if there is significant stray capacitance at the reference capacitor terminals. Minimize the stray capacitance on the reference capacitor terminals to reduce the rollover error, and if necessary, increase the reference capacitor value to $1.0\mu\text{F}$.

The printed circuit board should be carefully cleaned to minimize leakage at the C_{REF} terminals since leakage will cause both gain and rollover errors. Due to the increased leakage of the MAX138/139/140 at $+70^\circ\text{C}$, a $1.0\mu\text{F}$ reference capacitor is recommended to reduce rollover and gain errors at high temperature.

The reference capacitor is typically a low leakage film capacitor. Polyester (Mylar) is acceptable in applications where the reference voltage is constant. A low dielectric absorption capacitor such as polypropylene should be used if the reference voltage is variable, since any dielectric absorption will increase the settling time in response to a change in reference voltage. Since the reference voltage varies in circuits which measure resistance ratiometrically, a polypropylene reference capacitor should be used in ohmmeters.

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

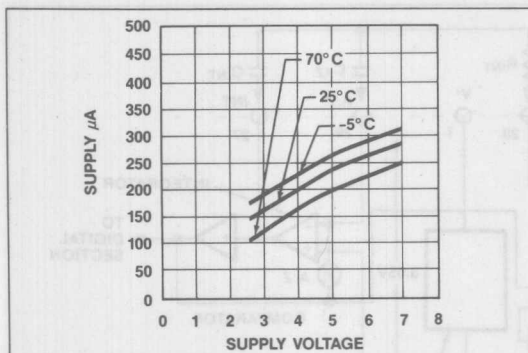


Figure 4A. MAX138, MAX139, MAX140
Typical Supply Current vs. Supply Voltage

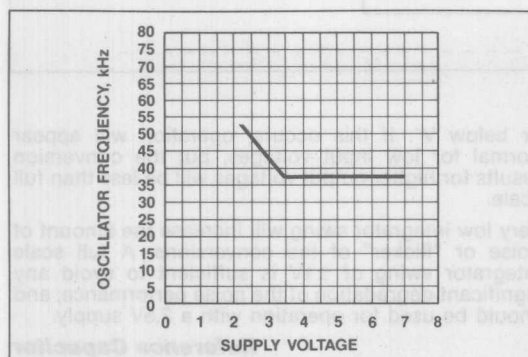


Figure 4B. MAX138, MAX139, MAX140 Typical
Oscillator Frequency vs. Supply Voltage

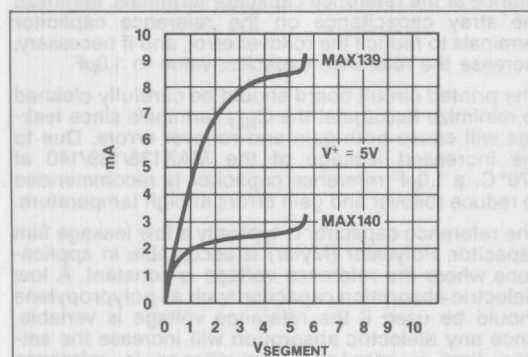


Figure 5. Output Current vs. Output Voltage

Autozero Capacitor

The noise of the A/D is influenced by the autozero capacitor. For the best noise performance, and autozero capacitor value of at least 4 times the integrator capacitor value is recommended. For a 2V scale, a 0.047μF (47nF) capacitor is adequate. An autozero capacitor of 0.47μF or greater is recommended for a 200mV full scale. All of Maxim's integrating A/D converters have a zero integrator phase which allows the use of high values for the autozero capacitor without causing hysteresis or slowing the overload recovery time.

The autozero capacitor can be any low leakage film capacitor in most applications. A low dielectric polypropylene capacitor is recommended if there are rapid changes in common mode voltage, or if the A/D must rapidly stabilize upon power up.

Charge Pump Capacitors

The charge pump capacitors should be 1μF.

Application Notes

Common Mode Voltage Range Considerations

Operation with low supply voltages, or operation with either IN LO or IN HI near either supply calls for careful evaluation of the effect of common mode voltages.

Since the MAX138/139/140 perform all conversion phases, including autozero and de-integration, using IN LO as the reference point, they have excellent normal mode rejection of approximately 120dB.

There are three basic internal limitations on the allowable common mode voltage (see Figure 3):

- 1) The buffer input CMVR is ($V^- + 1.5V$) to ($V^+ - 1.5V$).
- 2) The integrator CMVR is ($V^- + 1.5V$) to ($V^+ - 1.5V$).
- 3) The integrator output swing is limited to V^- to V^+ .

Figure 3 shows that the buffer input can be connected to either IN HI, (IN LO + V_{REF}), or (IN LO - V_{REF}). The integrator non-inverting input is always connected to IN LO.

Combining both system CMVR limitations with the possible connections results in the limitations shown in Table 1.

Low Battery Detector Circuit

Since the voltage between Common and V^+ is between 2.95V and 3.15V until the voltage between V^+ and V^- falls to less than 4V, a simple low battery detector can be made using transistor voltage detector as shown in Figure 6. When Q1 is off the Low Battery segment is driven in phase with the backplane and is off. When Q1 turns on, the Low Battery LCD segment becomes visible. Q1 turns on when the voltage at the base of Q1 is one base-emitter voltage more positive than COMMON voltage.

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

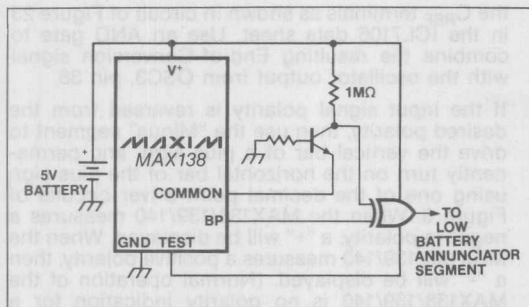


Figure 6. Low Battery Detector and LCD Segment Drive

Overload Display

The least significant three digits are blanked if the input voltage exceeds full scale. The leading "1" is displayed for positive overloads, and a "-1" is displayed for negative overloads. Any of the conditions that cause erratic readings as discussed above may cause overload readings. In addition, check the differential voltage between IN HI and IN LO and make sure that it is no more than twice the differential voltage between REF HI and REF LO. Also make sure that the voltage at REF HI is more positive than the voltage at REF LO, since incorrect reference polarity will always cause an overload reading.

Gross Nonlinearity

If the results are linear for low input voltages, but the displayed result stops increasing as higher input voltages are applied, then the most likely cause is saturation of the integrator output. With a full scale voltage applied, look at the voltage on the INT pin. It should not come closer than 0.3V to either supply. Increase the integrator capacitor value if the INT output swing is excessive. Alternatively, increase the oscillator frequency by changing the oscillator resistor and capacitor values.

Nonlinearities of 2 to 20 Counts

A polyester (Mylar) integrator capacitor will result in about 2 or 3 counts of nonlinearity at full scale. Use polypropylene for best linearity. Leakages into the integrator capacitor, the autozero capacitor, or the reference capacitor will also cause linearity errors. Make sure that printed circuit boards are thoroughly cleaned after soldering.

Gain Error and Rollover Error

A gross gain error will result if the integrator output

current capabilities are exceeded. Make sure that $R_{INT} \geq V_{REF}/0.6\mu A$.

Gain errors less than ten counts are generally caused by either too much stray capacitance on the C_{REF} terminals, or by excessive printed circuit board leakage. Stray capacitance and leakage can be detected by reducing the reference capacitor by a factor of ten. If the error dramatically increases, then either stray capacitance or leakage at the reference capacitor terminals is the culprit. Error caused by stray capacitance tend to be a pure gain error, while errors due to leakage tend to be nonlinear—typically square law. Errors due to leakage can also be detected by cleaning the board, then baking to reduce moisture content.

Missing Segments on the LCD Display

This is very, very rarely a problem of the MAX138. More often it is caused open circuits in the LCD connector/bezel, particularly if an elastomeric connector (zebra strip) is used. Check the voltage waveform at the pins of the MAX138. A signal in-phase with the backplane turns off an LCD segment, a signal 180° out of phase from the backplane turns on an LCD segment.

Noisy Readings

The most common reason for noisy readings, particularly in engineering labs, is simply that the input signal is noisy. The 1MΩ/10nF input filter shown in Figures 1 and 2 will significantly reduce high frequency noise, and the capacitor value can be increased to further attenuate 50/60Hz.

If the input signal is clean, then the next thing to check is integrator swing since low integrator swing will increase the noise. If the integrator swing must be reduced to less than 1V for some reason, then increasing the value of the autozero capacitor will improve the noise performance. For most circuits, the integrator swing should be approximately ±2V.

A very low value for the autozero capacitor will also make the readings noisy. The value of the autozero capacitor should be at least twice the value of the integration capacitor, and increasing the autozero capacitor value to between 4 and 10 times that of the integrator capacitor will improve the noise performance, particularly with low reference voltages.

Stray coupling of noise signals, either digital/microprocessor noise or 50/60Hz and 100/120Hz ripple can also be a cause of noisy readings. The circuit area most likely to pick up stray signals is the autozero capacitor. The distance between the autozero capacitor and the AZ pin should be minimized, as should the distance between the autozero capacitor and the

Table 1. Common Mode Voltage Limits

INPUT POLARITY	IN HI	IN LO	INTEGRATOR SWING
IN HI > IN LO	$V^+ + 1.5V$ to $V^+ - 1.5V$	$V^+ + (1.5V + V_{REF})$ to $V^+ - 1.5V$	$(IN LO - V^+)$
IN HI < IN LO	$V^+ + 1.5V$ to $V^+ - 1.5V$	$V^+ + 1.5V$ to $V^+ - (1.5V + V_{REF})$	$(V^+ - IN LO)$

3½ Digit A/D Converters with Bandgap Reference and Charge Pump Voltage Converter

integration resistor and capacitor. Since the BUFF and INT pins are the outputs of op amps, they are less sensitive to noise pick-up than is the AZ pin, which is the input of an op amp.

The MAX138/139/140 are sensitive to AC noise at IN LO during the de-integrate phase. In particular, full wave AC-DC converters should be used only if both outputs of the AC-DC converter output are well filtered.

The COMMON output of the MAX138/139/140, being derived from a bandgap reference, are noisier than the ICL7106 and ICL7136 Common outputs, which are derived from zeners. This could cause an increase in conversion noise, but only if the C_{REF} is less than $0.1\mu F$, and there is no bypassing at the reference inputs.

Poor bypassing of the supply voltage may cause a couple of counts of noise in the readings, particularly if the power supply also powers digital logic, since high frequency spikes on the power supply might cause the comparator to falsely indicate zero crossing one or two clock cycles early. Ordinary $0.1\mu F$ bypass capacitors are adequate in most cases. Since the MAX138/139/140 draw very little current, a simple RC filter can be used to provide greater spike and ripple attenuation in those cases where the power supply is exceptionally noisy.

Since the oscillator frequency is slightly affected by the supply voltage, large changes in the supply voltage during a conversion may cause a few counts of error. A typical case where the effect must be considered is in a battery powered circuit where the battery is also being used to drive high current loads such as motors or lamps. For extreme cases where high current loads momentarily change the battery voltage a volt or more, use a series diode and a capacitor of $10\mu F$ or greater.

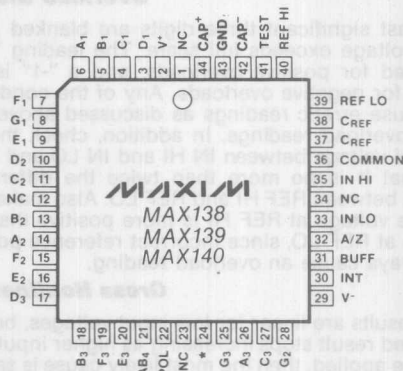
Application Hints

1. See the ICL7136 and ICL7106 data sheets for a variety of application circuits which can also be used with the MAX138/139/140.
2. In some applications it may be useful to apply a fixed reference voltage between IN HI and IN LO, and to apply the signal to REF HI and REF LO. In this mode of operation the displayed reading is inversely proportional to the input voltage. In other words, the displayed reading is the result of *dividing* the fixed reference voltage by the signal voltage. A typical application where this function is useful is in an RPM meter, where a voltage proportional to the period of a signal is divided into a fixed voltage to convert period into RPM (frequency). Another example is in a conductance meter, where the conversion between ohms and Siemens is performed by swapping the positions of the unknown and reference resistors.
3. A serial output pulse stream can be obtained from the MAX138/139/140 by monitoring the voltage at

the C_{REF} terminals as shown in circuit of Figure 23 in the ICL7106 data sheet. Use an AND gate to combine the resulting End-of-Conversion signal with the oscillator output from OSC3, pin 38.

4. If the input signal polarity is reversed from the desired polarity, then use the "Minus" segment to drive the vertical bar of a plus sign, and permanently turn on the horizontal bar of the plus sign using one of the decimal point driver circuits of Figure 6. When the MAX138/139/140 measures a negative polarity, a "+" will be displayed. When the MAX138/139/140 measures a positive polarity, then a "-" will be displayed. (Normal operation of the MAX138/139/140 is no polarity indication for a positive input, and a "-" sign for a negative input.)

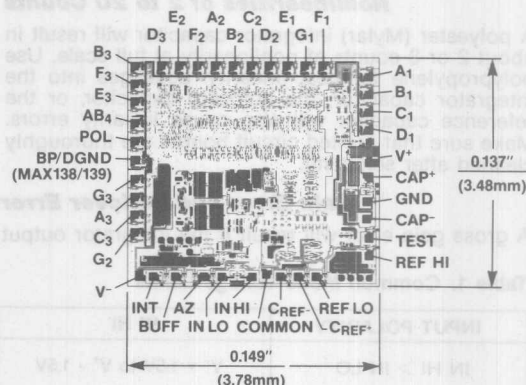
Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

*Note: BP (MAX 138)
DIGITAL GND (MAX139/140)

Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

300kHz 10-Bit A/D Converter with Reference and Track/Hold

MAX151

General Description

The MAX151 is a high-speed, easy-to-use, microprocessor (μ P) compatible 10-bit Analog-to-Digital Converter (ADC) with Track-and-Hold (T/H). Half-flash technique allows a typical conversion time of 1.9μ s with a Total Unadjusted Error (TUE) of ± 1 LSB (Max). The converter has a 0V to +5V analog input voltage range and uses ± 5 V supplies.

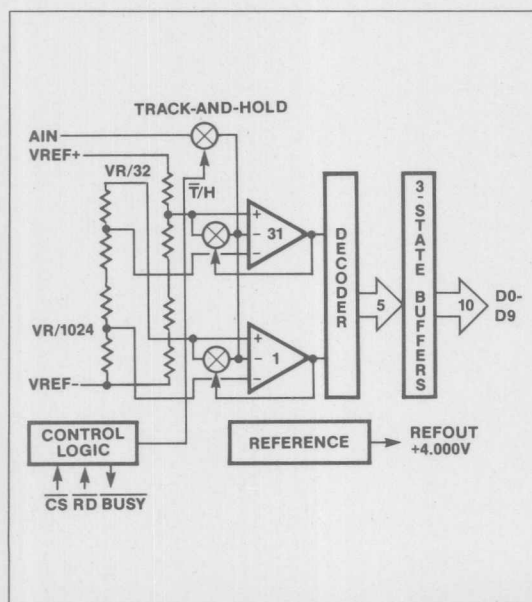
The MAX151 internally tracks and holds the analog input signal, eliminating the need for an external T/H for up to 40kHz signals. The MAX151 also contains an internal 4V reference, making the part a complete low-cost ADC. The part has a typical power consumption of 275mW and is available in both 0.3" DIP and Wide SO packages.

The MAX151 interfaces directly to a μ P by appearing as a memory location or Input/Output (I/O) port. Read (RD) and Chip Select (CS) inputs control the three-state outputs. Two memory modes ensure compatibility with most popular μ Ps.

Applications

Digital Signal Processing
High-Speed Data Acquisition
Telecommunications
High-Speed Servo Loops
Audio Systems

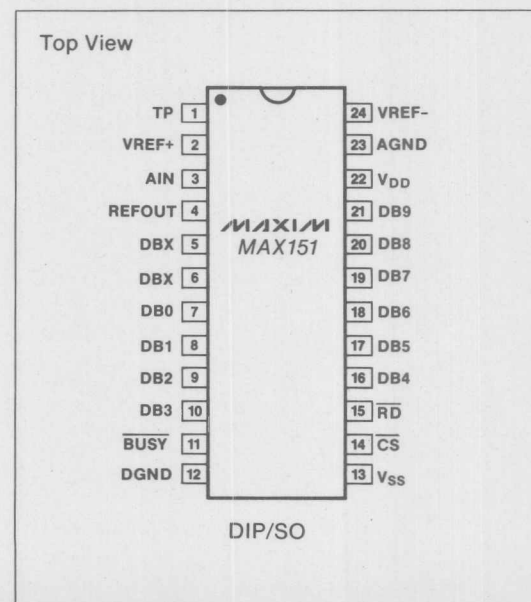
Block Diagram



Features

- ◆ 10-Bit Resolution and Accuracy
- ◆ ± 1 LSB Total Unadjusted Error
- ◆ 2.5 μ s Max Conversion Time (0.5 μ s Input Acquisition Time)
- ◆ 300kHz Sampling Rate
- ◆ T/H to Digitize 40kHz Signals
- ◆ Internal 60ppm/ $^{\circ}$ C Buried Zener Reference
- ◆ 1ppm/ $^{\circ}$ C A/D Gain and Offset Drift
- ◆ Internal Clock
- ◆ ± 5 V Supplies with 275mW Power Dissipation
- ◆ 24-Pin 0.3" DIP and Wide SO packages
- ◆ Slow Memory and ROM Mode μ P Interfaces
- ◆ DC and Dynamic Specified

Pin Configuration



High-Speed, 8-Bit ADCs with 8/4 Simultaneous T/Hs and Reference

General Description

The MAX155/MAX156 are high-speed, multi-channel 8-bit A/D converters (ADC) with simultaneous Track-and-Hold (T/H) and 8 x 8 dual-port RAM. The MAX155 has 8 analog input channels, and the MAX156 has 4 analog input channels. Each channel has a separate T/H that holds the signal for the internal A/D. The A/D converts each channel in 3 μ s and stores the result in the RAM. The MAX155/MAX156 also feature a 2.5V on-chip reference, forming a complete high-speed data acquisition system.

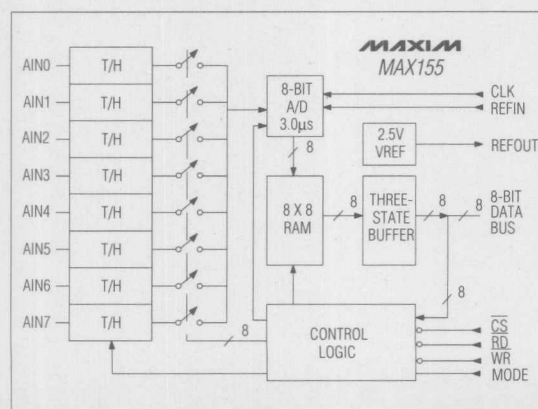
These devices can be used with a single 5V supply and perform unipolar or bipolar conversions with single-ended or differential inputs. For applications where an extended input range or bipolar conversion about ground is important, an optional negative supply pin (labeled Vss/AGND) is provided.

Conversions are initiated with a \overline{WR} pulse, and data is accessed with a RD pulse. Bidirectional Input/Output pins can be used to update the chip's command register. Hard-wired modes of operation, which bypass the command register, are also provided.

Applications

Digital Oscilloscope
Vibration Analysis
Input for DSP
Digital-Strip Chart Recorder
High-Speed Phase-Sensitive Data Acquisition

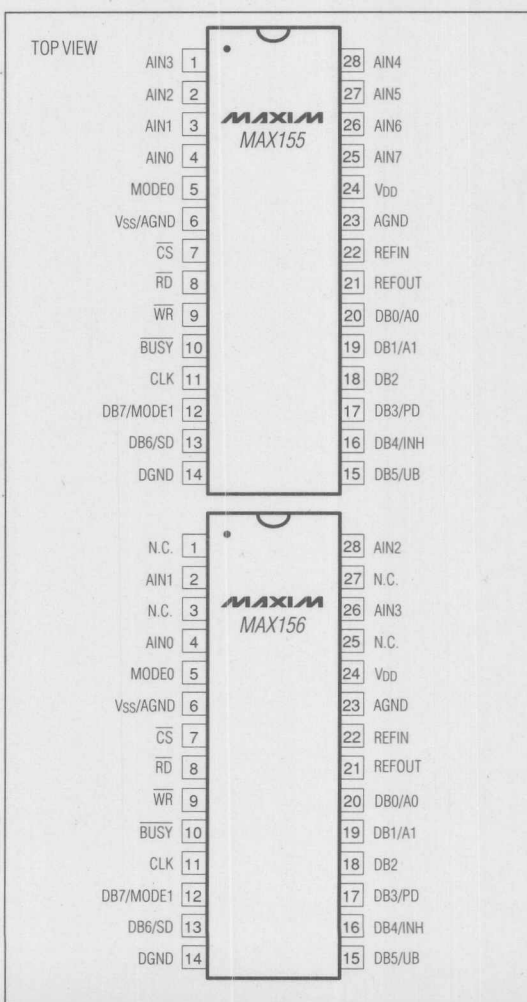
Functional Diagram



Features

- ◆ One-Chip Data Acquisition System
- ◆ 8 or 4 Analog Input Channels
- ◆ Single-Ended or Differential Inputs
- ◆ Simultaneous T/H
- ◆ 3.0 μ s Conversion Time per Channel
- ◆ On-Chip 8 x 8 Dual-Port RAM
- ◆ Internal 2.5V Reference
- ◆ Single +5V Supply Operation

Pin Configurations



MAX155/MAX156

1



Complete High-Speed CMOS 12-Bit ADC

General Description

The MAX162 and MX7572 are complete 12-Bit analog-to-digital converters (ADC's) that combine high speed, low power consumption, and an on-chip voltage reference. The conversion times are 3 μ s (MAX162) and 5 and 12 μ s (MX7572). The buried zener reference provides low drift and low noise performance.

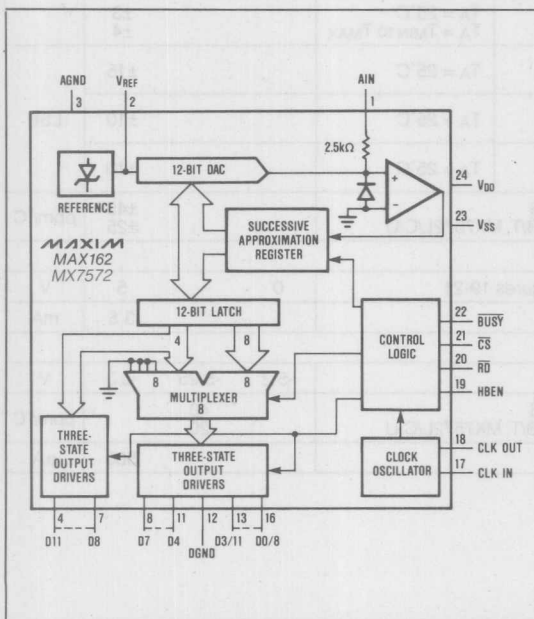
External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX162/MX7572 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)
High Accuracy Process Control
High Speed Data Acquisition
Electro-Mechanical Systems

Functional Diagram



Features

- ◆ 12-Bit Resolution and Linearity
- ◆ 3 μ s (MAX162), 5 μ s and 12 μ s (MX7572) Conversion Times
- ◆ No missing Codes
- ◆ On-Chip Voltage Reference
- ◆ 90ns Access Time
- ◆ 215mW Max Power Consumption
- ◆ 24-Lead Narrow DIP Package

Ordering Information

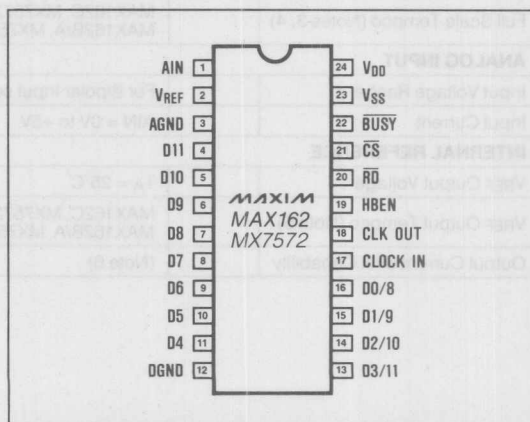
PART	TEMP. RANGE	PACKAGE*	ERROR
3μs CONVERSION TIME			
MAX162ACNG	0°C to +70°C	Plastic DIP	$\pm\frac{1}{2}$ LSB
MAX162BCNG	0°C to +70°C	Plastic DIP	± 1 LSB
MAX162CCNG	0°C to +70°C	Plastic DIP	± 1 LSB
MAX162ACWG	0°C to +70°C	Wide S.O.	$\pm\frac{1}{2}$ LSB
MAX162BCWG	0°C to +70°C	Wide S.O.	± 1 LSB
MAX162CCWG	0°C to +70°C	Wide S.O.	± 1 LSB
MAX162CC/D	0°C to +70°C	Dice**	± 1 LSB
MAX162AING	-25°C to +85°C	Plastic DIP	$\pm\frac{1}{2}$ LSB
MAX162BING	-25°C to +85°C	Plastic DIP	± 1 LSB
MAX162CING	-25°C to +85°C	Plastic DIP	± 1 LSB
MAX162AMRG	-55°C to +125°C	CERDIP	$\pm\frac{1}{2}$ LSB
MAX162BMRG	-55°C to +125°C	CERDIP	± 1 LSB
MAX162CMRG	-55°C to +125°C	CERDIP	± 1 LSB

* All devices — 24 lead packages

** Consult factory for dice specifications

Ordering Information continued on last page.

Pin Configuration



MAXIM is a registered trademark of Maxim Integrated Products.

Maxim Integrated Products 1-31

MAX162/MX7572

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Complete High-Speed CMOS 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND	-0.3V to +7V
V _{SS} to DGND	+0.3V to -17V
AGND to DGND	-0.3V, V _{DD} + 0.3V
AIN to AGND	-15V to +15V
Digital Input Voltage to DGND	-0.3V, V _{DD} + 0.3V (Pins 17, 19-21)
Digital Output Voltage to DGND	-0.3V, V _{DD} + 0.3V (pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges

MAX162XC, MX7572JN, KN, LN, JCWG, KCWG, LCWG	0°C to +70°C
MAX162XI, MX7572AQ, BQ, CQ	-25°C to +85°C
MAX162XM, MX7572SQ, TQ, UQ	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Power Dissipation (any Package) to +75°C	1000mW
Derates Above +75°C by	10mW/°C
Lead Temperature (Soldering 10 seconds)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -15V ±5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted.
f_{CLK} = 4MHz for MAX162, 2.5MHz for MX7572XX05 and 1MHz for MX7572XX12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
ACCURACY								
Resolution				12			Bits	
Integral Non-Linearity	INL	MAX162A, MX7572L/C/U	T _A = 25°C				±1/2	
		MAX162AC, AI, MX7572L/C					±1/2	
		MAX162AM, MX7572U					±3/4	
		MAX162B/C, MX7572K/B/T/J/A/S					±1	
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temp.					±1	LSB
Offset Error (Note 1)		MAX162C, MX7572J/A/S	T _A = 25°C T _A = T _{MIN} to T _{MAX}				±4 ±6	
		MAX162B, MX7572K/B/T	T _A = 25°C T _A = T _{MIN} to T _{MAX}				±3 ±5	
		MAX162A, MX7572L/C/U	T _A = 25°C T _A = T _{MIN} to T _{MAX}				±3 ±4	
Full Scale Error (Note 2)		MAX162C, MX7572J/A/S	T _A = 25°C				±15	
		MAX162B, MX7572K/B/T	T _A = 25°C				±10	
		MAX162A, MX7572L/C/U	T _A = 25°C				±10	
Full Scale Tempco (Notes 3, 4)		MAX162C, MX7572J/A/S MAX162B/A, MX7572K/B/T, MX7572L/C/U			±45 ±25			ppm/°C
ANALOG INPUT								
Input Voltage Range		For Bipolar Input see Figures 19-21		0		5	V	
Input Current		AIN = 0V to +5V				3.5	mA	
INTERNAL REFERENCE								
VREF Output Voltage		T _A = 25°C		-5.2	-5.25	-5.3	V	
VREF Output Tempco (Note 5)		MAX162C, MX7572J/A/S MAX162B/A, MX7572K/B/T, MX7572L/C/U		40 20			ppm/°C	
Output Current Sink Capability		(Note 6)					500	μA

Complete High-Speed CMOS 12-Bit ADC

MAX162/MX7572

1

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V ±5%, V_{SS} = -15V ±5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted.
f_{CLK} = 4MHz for MAX162, 2.5MHz for MX7572XX05 and 1MHz for MX7572XX12)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REJECTION						
V _{DD} Only		FS Change, V _{SS} = -15V, V _{DD} = 4.75 to 5.25V		±1/2		LSB
V _{SS} Only		FS Change, V _{DD} = 5V MAX162/MX7572 MAX162		±1/8 ±1/8		LSB LSB
LOGIC INPUTS						
Input Low Voltage	V _{IL}	$\overline{\text{CS}}$, $\overline{\text{RD}}$, HBEN, CLKIN			0.8	V
Input High Voltage	V _{IH}	$\overline{\text{CS}}$, $\overline{\text{RD}}$, HBEN, CLKIN	2.4			V
Input Capacitance (Note 7)	C _{IN}	$\overline{\text{CS}}$, $\overline{\text{RD}}$, HBEN, CLKIN			10	pF
Input Current	I _{IN}	$\overline{\text{CS}}$, $\overline{\text{RD}}$, HBEN, CLKIN VIN = 0 to V _{DD}			±10 ±20	μA
LOGIC OUTPUTS						
Output Low Voltage	V _{OL}	D11-D0/8, $\overline{\text{BUSY}}$, CLKOUT I _{SINK} = 1.6mA			0.4	V
Output High Voltage	V _{OH}	D11-D0/8, $\overline{\text{BUSY}}$, CLKOUT I _{SOURCE} = 200μA	4			V
Floating State Leakage Current	I _{LKG}	D11-D0/8, V _{OUT} = 0V to V _{DD}			±10	μA
Floating State Output Capacitance (Note 7)	C _{OUT}				15	pF
CONVERSION TIME						
MAX162	t _{CONV}	f _{CLK} = 4MHz Synchronous (13 clock cycles) Asynchronous (12 to 13 clock cycles)	3		3.25 3.25	μs
MX7572XX05	t _{CONV}	f _{CLK} = 2.5MHz Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	4.8		5 5.2	μs
MX7572XX12	t _{CONV}	f _{CLK} = 1MHz Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	12		12.5 13	μs
POWER REQUIREMENTS						
V _{DD}		±5% for Specified Performance	4.75	5	5.25	V
V _{SS} (Note 8)		±5% MAX162 ±5% MX7572		-12 or -15 -15		V
I _{DD}		$\overline{\text{CS}}$ = $\overline{\text{RD}}$ = V _{DD} , AIN = 5V		5	7	mA
I _{SS}		$\overline{\text{CS}}$ = $\overline{\text{RD}}$ = V _{DD} , AIN = 5V		8	12	mA
Power Dissipation		V _{DD} = +5V, V _{SS} = -15V		145	215	mW

Note 1: Typical change over temp is ±1LSB

Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5.000V, Ideal last code transition = FS - 3/2LSB

Note 3: Full Scale TC = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.

Note 4: Includes internal reference drift.

Note 5: V_{REF} TC = ΔV_{REF}/ΔT, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.

Note 6: Output current should not change during conversion.

Note 7: Guaranteed by design, not subject to test.

Note 8: V_{SS} = -12V ±5% for the MAX162 only. Functional operation is guaranteed by testing offset error and full scale error.

Complete High-Speed CMOS 12-Bit ADC

TIMING CHARACTERISTICS (Note 9)

($V_{DD} = +5V$, $V_{SS} = -15V$; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	$T_A = 25^\circ C$			MAX162C/I MX7572J/K/L MX7572A/B/C		MAX162M MX7572S/T/U		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CS to RD Setup Time	t_1		0			0		0		ns
RD to BUSY Delay	t_2	$C_L = 50pF$		90	190		230		270	ns
Data Access Time (Note 10)	t_3	$C_L = 20pF$ $C_L = 100pF$		60 70	90 125		110 150		120 170	ns
RD Pulse Width	t_4		t_3			t_3		t_3		
\overline{CS} to \overline{RD} Hold Time	t_5		0			0		0		ns
Data Setup Time After \overline{BUSY} Note (10)	t_6			70			90		100	ns
Bus Relinquish Time (Note 11)	t_7		20		75	20	85	20	90	ns
HBEN to \overline{RD} Setup Time	t_8		0			0		0		ns
HBEN to \overline{RD} Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: Timing specifications are sample tested at $25^\circ C$ to ensure compliance. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

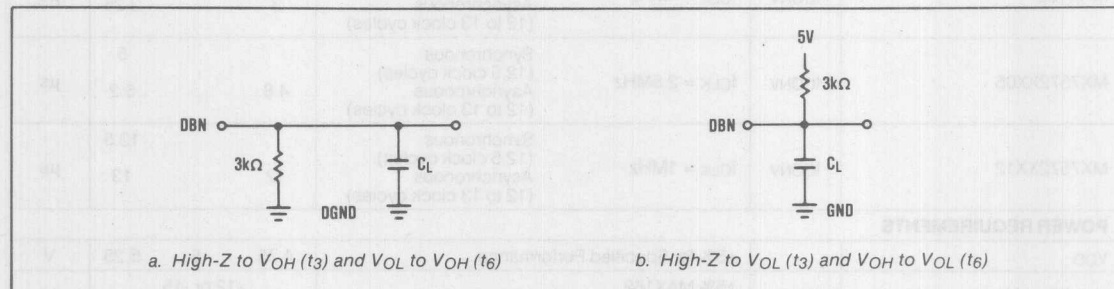


Figure 1. Load Circuits for Access Time

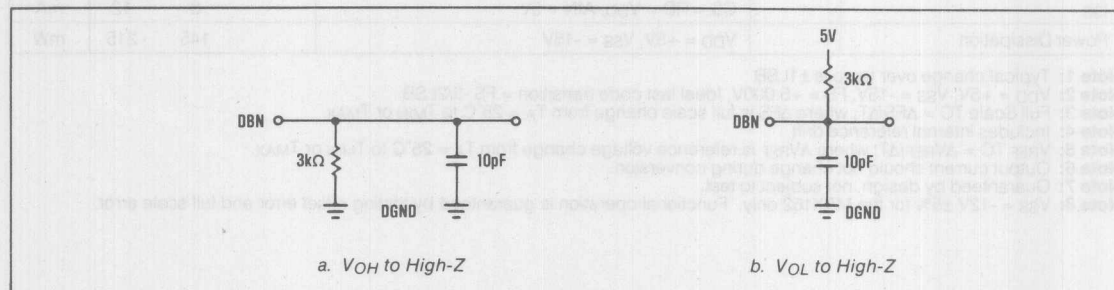


Figure 2. Load Circuits for Output Float Delay

Complete High-Speed CMOS 12-Bit ADC

Pin Description

PIN	NAME	FUNCTION
1	AIN	Analog Input, 0 to +5V unipolar input
2	V _{REF}	-5.25V Reference Output
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3/11-D0/8	Three-State Data Outputs
17	CLKIN	Clock Input. An external TTL/CMOS compatible clock may be applied to this pin or a crystal can be connected between CLKIN and CLKOUT.
18	CLKOUT	Clock Output. An inverted CLKIN signal appears at this pin.

PIN	NAME	FUNCTION
19	HBEN	High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7-D0/8). HBEN also disables conversion starts when HIGH.
20	$\overline{\text{RD}}$	READ Input. This active low signal starts a conversion when CS and HBEN are low. RD also enables the output drivers when CS is low.
21	$\overline{\text{CS}}$	The CHIP SELECT Input must be low for the ADC to recognize RD and HBEN inputs.
22	$\overline{\text{BUSY}}$	The BUSY Output is low when a conversion is in progress.
23	V _{SS}	Negative Supply, -15V for MX7572 and -15V or -12V for MAX162.
24	V _{DD}	Positive Supply, +5V.

Data Bus Output, $\overline{\text{CS}}$ & $\overline{\text{RD}}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Note:

* D11 ... D0/8 are the ADC data output pins.
DB11 ... DB0 are the 12-bit conversion results, DB11 is the MSB.

Converter Operation

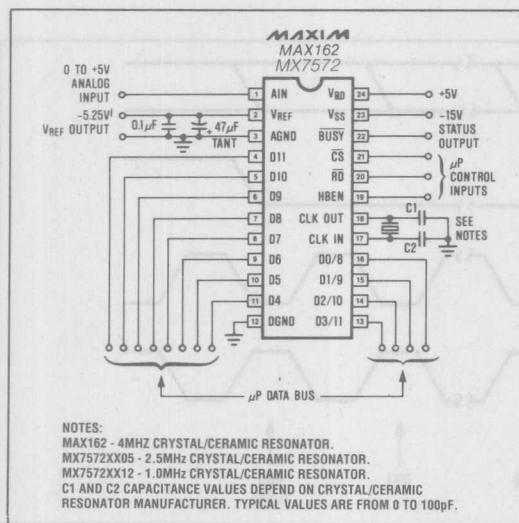


Figure 3. MAX162/MX7572 Operational Diagram

The MAX162 and MX7572 use a successive approximation technique to convert an unknown analog input to a 12 bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only a few external passive components to perform the analog-to-digital function. Figure 3 shows the MAX162/MX7572 in its simplest operational configuration.

Figure 4 shows the MAX162/MX7572 analog equivalent circuit. The internal voltage output DAC is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero crossing detector and its output is fed back to the SAR input.

Conversion start is controlled by the $\overline{\text{CS}}$, $\overline{\text{RD}}$ and HBEN digital inputs. A conversion starts at the falling edge of CS and RD while HBEN is low. Once started, conversion cannot be stopped. The BUSY output goes low as soon as the conversion starts. BUSY may be used to control an external sample-and-hold when wide bandwidth input signals are being measured.

Complete High-Speed CMOS 12-Bit ADC

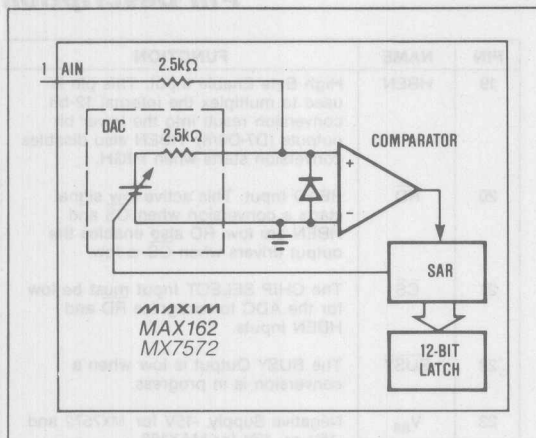


Figure 4. MAX162/MX7572 Analog Equivalent Circuit

The SAR is set to half scale as soon as the \overline{CS} and \overline{RD} inputs go low. This reset is asynchronous with the clock input. The analog input is then compared to one half of the full scale voltage. About 30ns after the second falling edge of CLKIN (or rising edge of CLKOUT), the output of the comparator is latched into the SAR MSB bit (see Figure 5). The bit is kept if the analog input is greater than half scale, or dropped if it is smaller. The next bit (bit 11) is then set with the DAC output either at 1/4 scale (if the MSB was dropped) or 3/4 scale (if the MSB was kept). The conversion continues in this manner until the LSB is tried. Following a falling CLKIN signal, the BUSY output goes high and the SAR result is latched into the three-state output buffers.

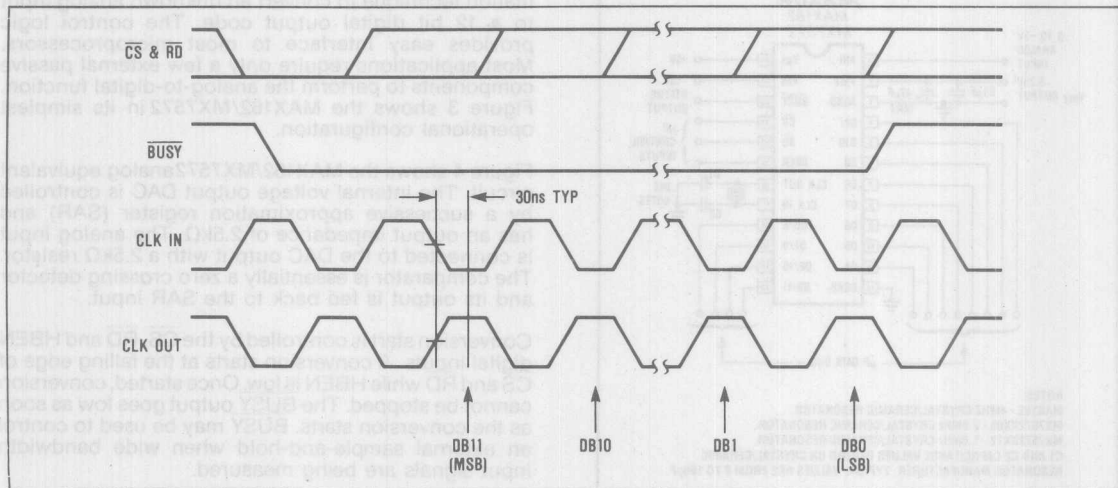


Figure 5. Operating Waveforms Using an External Clock Source for CLKIN.

Clock Operation

Clock Oscillator

Figure 6 shows the MAX162/MX7572 clock circuitry. The capacitive load on the CLKOUT pin must be minimized for low power dissipation and to avoid digital coupling of the CLKOUT buffer currents to the comparator. If an external clock source is being used to drive CLKIN, CLKOUT should be left open. The external clock source must have a 50% duty cycle. If the internal oscillator is being used, a crystal/ceramic resonator should be connected between CLKOUT and CLKIN as shown in Figure 6.

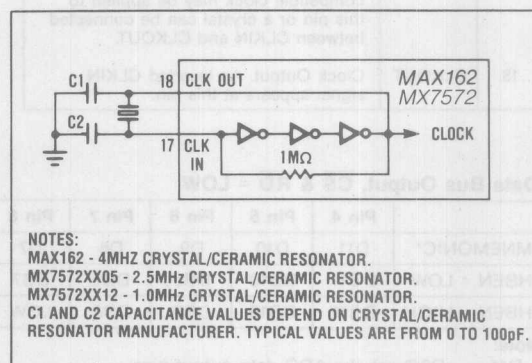


Figure 6. MAX162/MX7572 Internal Clock Circuit

Complete High-Speed CMOS 12-Bit ADC

Control Input Synchronization

In applications where the \overline{RD} control input is not synchronized with the ADC clock, the conversion time can vary from 12 to 13 clock cycles. The SAR changes state on the falling edge of the CLKIN input (or rising edge on the CLKOUT pin). To ensure a fixed conversion time use the following guidelines for synchronization:

MAX162

For the MAX162 the \overline{RD} input should go low at the falling edge of CLKIN. In this case the conversion lasts 13 clock cycles and the conversion time is $3.25\mu\text{s}$ when $f_{\text{CLK}} = 4\text{MHz}$. If the CLKIN and \overline{RD} falling edges are skewed, the skew must not be more than 50ns to ensure the 13 period conversion time (See Figure 7). The MSB is tried at the second clock falling edge, leaving two clock cycles for the external sample-and-hold to settle from hold transients.

The MX7572 \overline{RD} input can go low at the rising edge of CLKIN. In this case the conversion lasts 12.5 clock cycles and the conversion time is $5\mu\text{s}$ when $f_{\text{CLK}} = 2.5\text{MHz}$ and $12.5\mu\text{s}$ when $f_{\text{CLK}} = 1\text{MHz}$. The delay from the falling edge of \overline{RD} to the falling edge of CLKIN must not be less than 180ns to ensure the 12.5 clock cycle conversion time (See Figure 8). This leaves the external sample-and-hold 1.5 clock cycles to settle from hold transients. An additional half clock cycle of settling can be allowed for driving the sample-and-hold by having \overline{RD} go low at the falling edge of CLKIN, similar to the MAX162. This results in a 13 cycle conversion time ($5.2\mu\text{s}$ when $f_{\text{CLK}} = 2.5\text{MHz}$, $13\mu\text{s}$ when $f_{\text{CLK}} = 1\text{MHz}$).

MX7572

MAX162/MX7572

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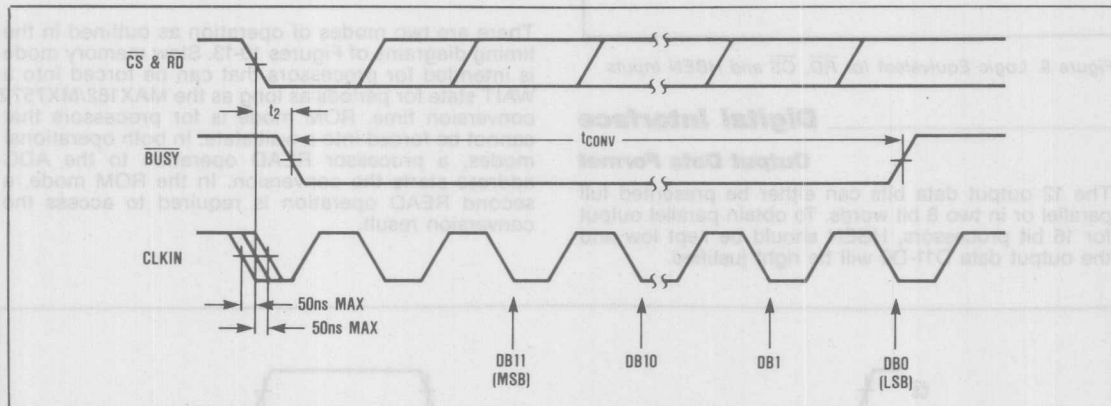


Figure 7. MAX162 \overline{RD} and CLKIN For Synchronous Operation

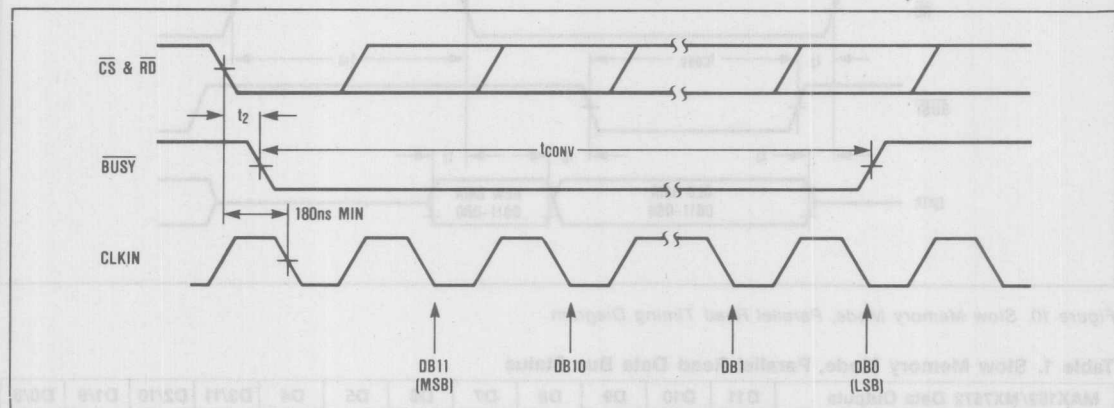


Figure 8. MX7572 \overline{RD} and CLKIN For Synchronous Operation

Complete High-Speed CMOS 12-Bit ADC

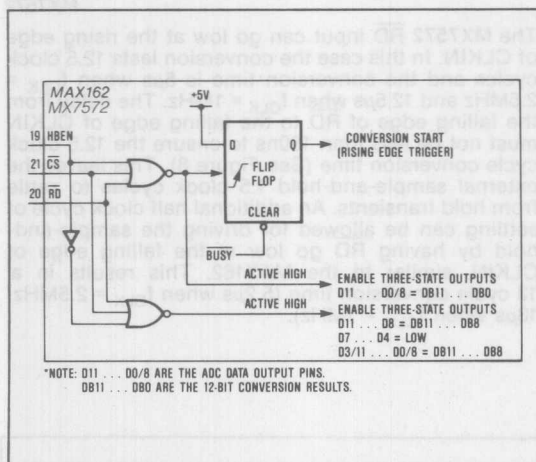


Figure 9. Logic Equivalent for \overline{RD} , \overline{CS} and HBEN Inputs

Digital Interface

Output Data Format

The 12 output data bits can either be presented full parallel or in two 8 bit words. To obtain parallel output for 16 bit processors, HBEN should be kept low and the output data D11-D0 will be right justified.

For a two byte data read, outputs D7-D0/8 are used. Byte selection is controlled by HBEN which multiplexes the data outputs. When HBEN is low, the lower 8 bits are presented at the data outputs. When HBEN is high, the upper 4 bits are presented with the leading 4 bits being low for D7-D0/8.

Note that the 4 MSB's always appear at digital outputs D11-D8 whenever the digital drivers are enabled, regardless of the state of HBEN.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs; HBEN, CS and RD. Figure 9 shows the logic equivalent for the conversion and data output control circuitry. A logic low is required on all three inputs to start a conversion. Once a conversion is in progress, it cannot be re-started. The BUSY output is low during the entire conversion cycle.

There are two modes of operation as outlined in the timing diagrams of Figures 10-13. Slow memory mode is intended for processors that can be forced into a WAIT state for periods as long as the MAX162/MX7572 conversion time. ROM mode is for processors that cannot be forced into a wait state. In both operational modes, a processor READ operation to the ADC address starts the conversion. In the ROM mode, a second READ operation is required to access the conversion result.

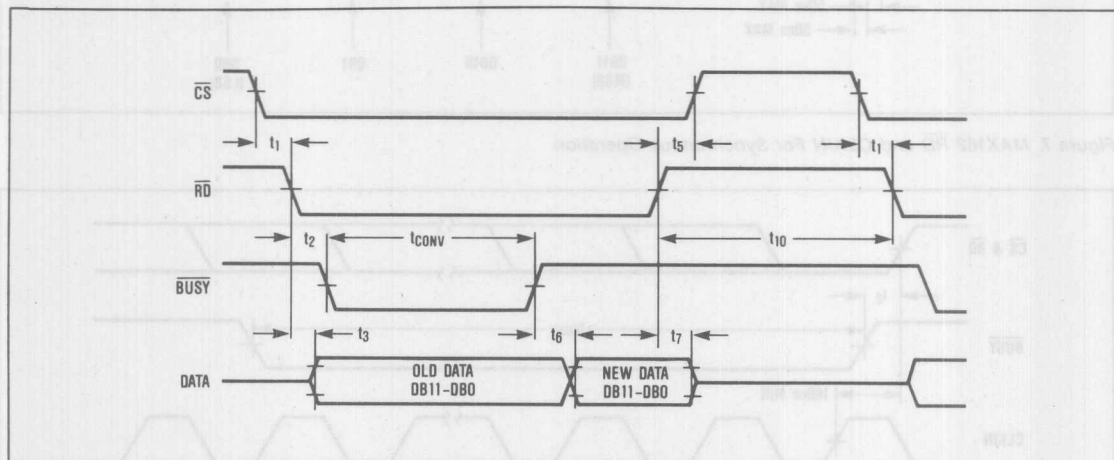


Figure 10. Slow Memory Mode, Parallel Read Timing Diagram

Table 1. Slow Memory Mode, Parallel Read Data Bus Status

MAX162/MX7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Complete High-Speed CMOS 12-Bit ADC

MAX162/MX7572

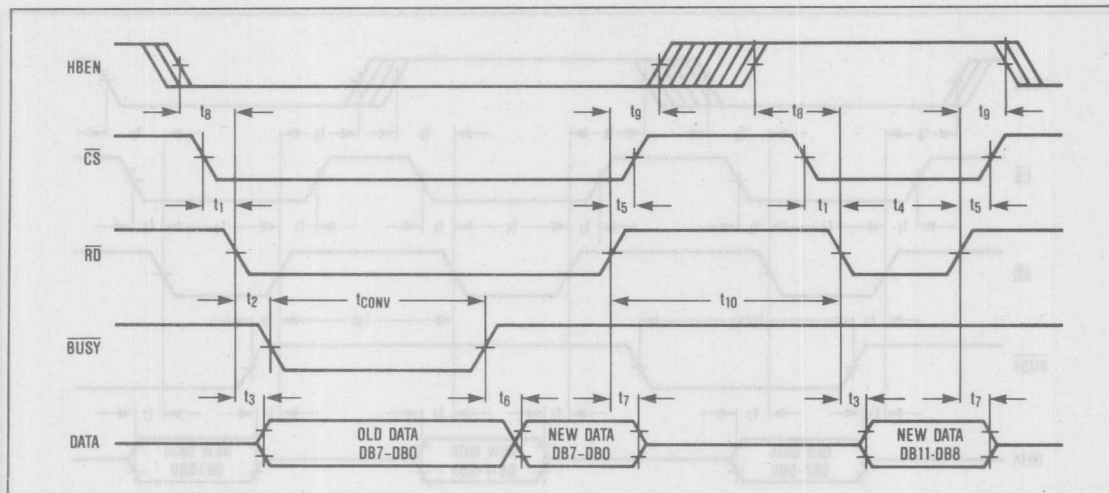


Figure 11. Slow Memory Mode, Two Byte Read Timing Diagram

Table 2. Slow Memory Mode, Two Byte Read Data Bus Status

MAX162/MX7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

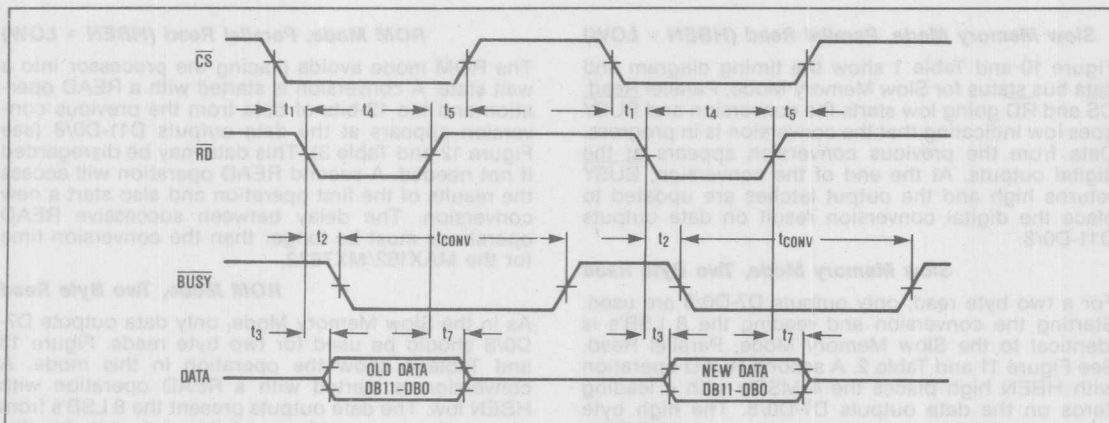


Figure 12. ROM Mode, Parallel Read Timing Diagram

Table 3. ROM Mode, Parallel Read Data Bus Status

MAX162/MX7572 Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Complete High-Speed CMOS 12-Bit ADC

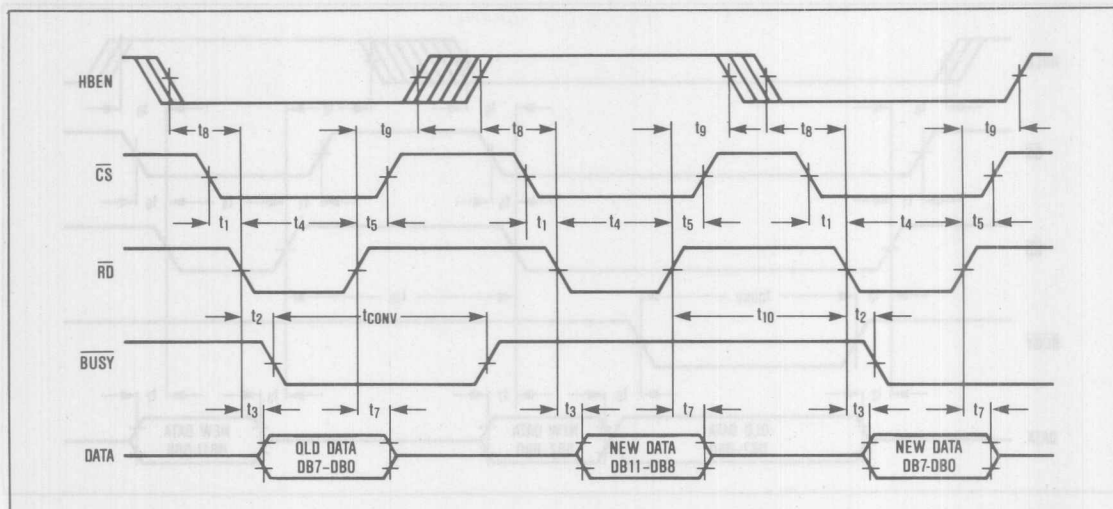


Figure 13. ROM Mode, Two Byte Read Timing Diagram

Table 4. ROM Mode, Two Byte Read Data Bus Status

MAX162/MX7572 Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Slow Memory Mode, Parallel Read (HBEN = LOW)

Figure 10 and Table 1 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. CS and RD going low starts the conversion and BUSY goes low indicating that the conversion is in progress. Data from the previous conversion appears at the digital outputs. At the end of the conversion, BUSY returns high and the output latches are updated to place the digital conversion result on data outputs D11-D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read, only outputs D7-D0/8 are used. Starting the conversion and reading the 8 LSB's is identical to the Slow Memory Mode, Parallel Read. See Figure 11 and Table 2. A second READ operation with HBEN high places the 4 MSB's with 4 leading zeros on the data outputs D7-D0/8. The high byte read does not start another conversion since HBEN is high.

ROM Mode, Parallel Read (HBEN = LOW)

The ROM mode avoids placing the processor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion appears at the data outputs D11-D0/8 (see Figure 12 and Table 3). This data may be disregarded if not needed. A second READ operation will access the results of the first operation and also start a new conversion. The delay between successive READ operations must be longer than the conversion time for the MAX162/MX7572.

ROM Mode, Two Byte Read

As in the Slow Memory Mode, only data outputs D7-D0/8 should be used for two byte reads. Figure 13 and Table 4 show the operation in this mode. A conversion is started with a READ operation with HBEN low. The data outputs present the 8 LSB's from the previous conversion and this data can be disregarded if not required. Two more READ operations are needed to access the conversion result. The first READ must be with HBEN high, where the 4 MSB's with 4 leading zero's are accessed. The second READ is with HBEN low, which reads in the 8 LSB's and starts a new conversion.

000	010	0110	1100	00	00	00	10	00
000	100	000	000	000	000	000	000	000
000	100	000	000	000	000	000	000	000

Complete High-Speed CMOS 12-Bit ADC

Interface Application Hints

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, LSBs of error can be caused due to coupling from the data pins to the ADC comparator. Using the Slow Memory Mode avoids this problem by placing the processor in a wait state during the conversion. In the ROM mode, if the data bus is going to be active during the conversion, the bus should be isolated from the ADC using three-state drivers.

ROM Mode

Considerable digital noise is generated in the ADC when RD or CS go high and the output data drivers are disabled after a conversion is started. This noise will feed into the ADC comparator and cause large errors if it coincides with the time the SAR is latching a decision to keep or drop a bit. To avoid this problem, RD and CS should be active for less than one clock cycle. In other words, the RD and CS low pulse should be shorter than 250ns for the MAX162, 400ns for the MX7572XX05 and 1 μ s for the MX7572XX12. If this cannot be done, the RD or CS signal must go high at a rising edge of CLKIN, since the comparator output is always latched at falling edges of CLKIN.

Analog Considerations

Application Hints

Physical Layout

For best system performance printed circuit boards should be used for the MAX162/MX7572. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX162/MX7572 package.

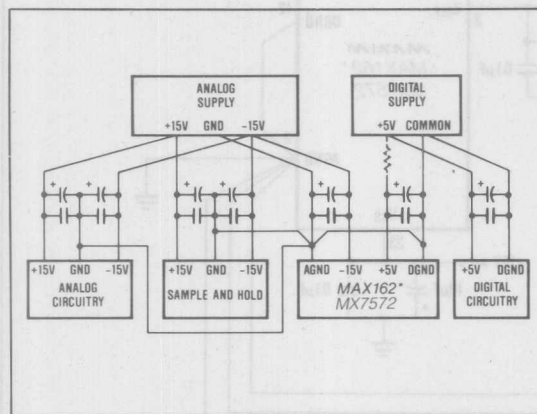


Figure 14. Power Supply Grounding Practice

Grounding

Figure 14 shows the recommended system ground connections. A single point analog STAR ground should be established at pin 3 (AGND) of the MAX162/MX7572 separate from the logic ground. All other analog grounds and pin 12 (DGND) of the MAX162/MX7572 should be connected to this STAR ground and no other digital grounds should be connected to this STAR point. The ground return to the power supply from this STAR ground should be low impedance for noise free operation of the ADC.

Power Supply Bypassing

The high speed comparator in the ADC is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be by-passed to the analog STAR ground with 0.1 μ F and 10 μ F by-pass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small (10-20 ohms) resistor can be connected as shown in Figure 14 to filter external noise.

Internal Reference

The MAX162/MX7572 has an internal buried zener reference which provides the DAC reference voltage. The reference voltage is -5.25V \pm 1% and has a low temperature coefficient. The reference output is available at pin 2, and should be bypassed to analog ground (pin 3) with a 47 μ F tantalum capacitor in parallel with 0.1 μ F capacitor to minimize noise and provide low impedance at high frequencies. This by-pass capacitor must not be less than 4.7 μ F. The internal reference output buffer can sink up to 500 μ A.

Driving The Analog Input

The input signal leads to AGND and AIN should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5k Ω . The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion (4MHz for MAX162 and 2.5 or 1MHz for the MX7572). The output impedance of the driving amplifier is equal to its open loop output impedance divided by the loop gain at the frequency of interest.

MX7572 The MX7572 maximum clock rate of 2.5MHz makes it possible to drive it with amplifiers like the OP-42, AD711 or OP-27. At 1MHz clock rate a MAX400 or OP-07 can also be used.

MAX162 The MAX162 with a maximum 4MHz clock rate might cause settling problems with the above amplifiers. An LF356, LF400 or LT1056 can be used to drive the input. Alternatively, an emitter follower buffer inside the feedback loop of a OP-42, AD711 or OP-27 can be used to improve high frequency output impedance.

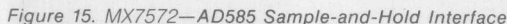
MAX162/MX7572

The analog input to the ADC must be stable to within 1/2 LSB during the entire conversion for specified 12 bit accuracy. This limits the input signal bandwidth to less than 6Hz for sinusoidal inputs, even when using the faster MAX162. For higher bandwidth signals a sample-and-hold should be used.

edge of **BUSY**.

To achieve the maximum sampling rate, the MAX162/MX7572 data must be read within the time allowed for the sample-and-hold to acquire a new input voltage.

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock allowing for a 3 μ s sample-and-hold acquisition time.



Complete High-Speed CMOS 12-Bit ADC

MAX162/MX7572

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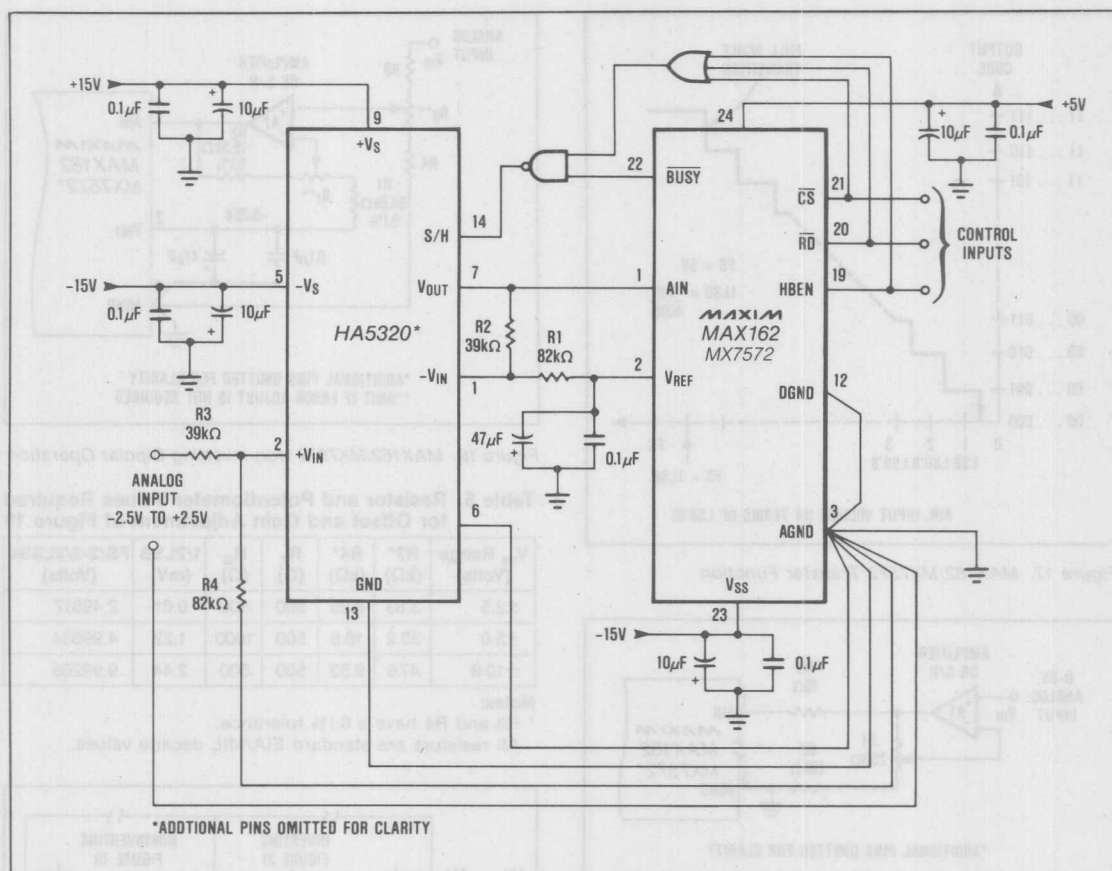


Figure 16. MAX162/MX7572-HA5320 Sample-and-Hold Interface

MAX162 Figure 16 shows the MAX162 to HA5320 interface. The maximum sampling rate is 210kHz with a 4MHz clock which allows for a 1.5μs acquisition time. The HA5320 can also be replaced by a HA5330 for higher throughput.

Unipolar Input Operation

Figure 17 shows the nominal input/output transfer function of the MAX162/MX7572. Code transitions occur half way between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 18. Note that the amplifier shown

could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS-3/2LSB (4.99817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 5 and 6.

Complete High-Speed CMOS 12-Bit ADC

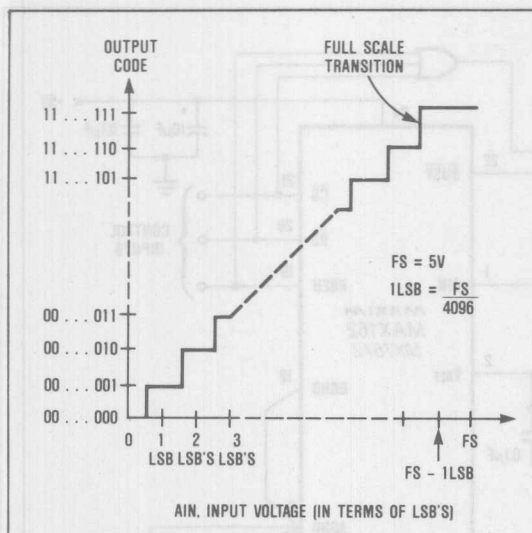


Figure 17. MAX162/MX7572 Transfer Function

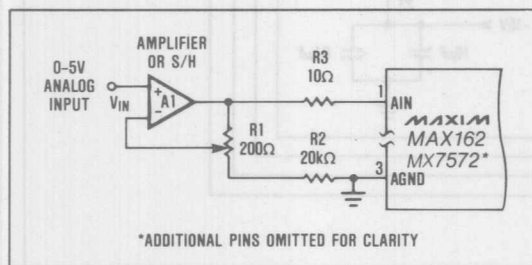


Figure 18. Full-Scale Adjustment

Figure 19 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 20 shows the ideal transfer function for this mode.

Figure 21 shows the bipolar operation in the inverting mode, where the output coding is complementary offset binary. Figure 20 shows the ideal transfer function for the circuit in Figure 21.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drifts. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

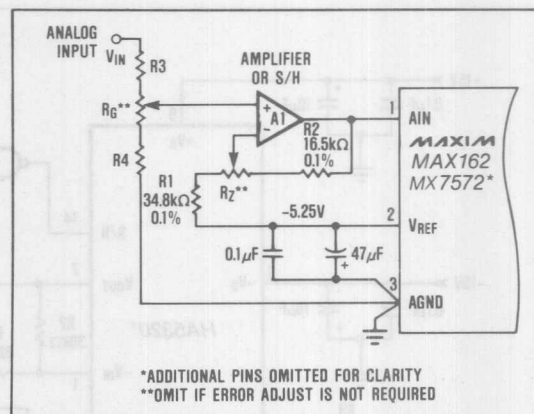


Figure 19. MAX162/MX7572 Non-inverting Bipolar Operation

Table 5. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 19

V _{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R _Z (Ω)	R _G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

Notes:

* R3 and R4 have a 0.1% tolerance.
All resistors are standard EIA/MIL decade values.

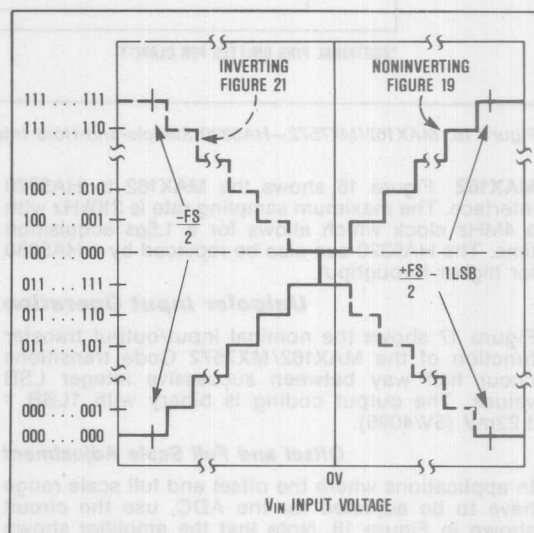


Figure 20. Ideal Input/Output Transfer Characteristic for the Bipolar circuits in Figures 19 and 21.

Complete High-Speed CMOS 12-Bit ADC

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply $+1/2\text{LSB}$ to the analog input (see tables 5 and 6) and adjust R_z until the output code flickers between the following codes:

For Non-inverting (Figure 19) 1000 0000 0000
1000 0000 0001

For inverting (Figure 21) 0111 1111 1111
0111 1111 1110

Apply $\text{FS}-3/2\text{LSB}$ (see tables 5 and 6) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-inverting (Figure 19) 1111 1111 1110
1111 1111 1111

For inverting (Figure 21) 0000 0000 0001
0000 0000 0000

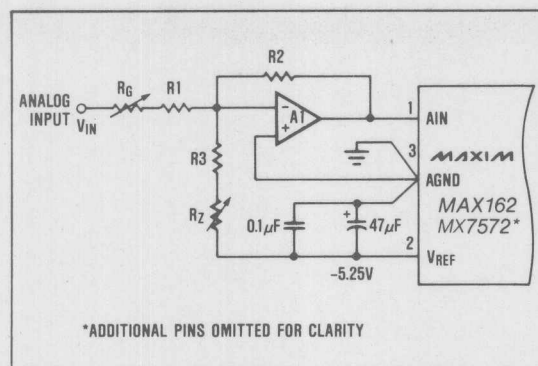
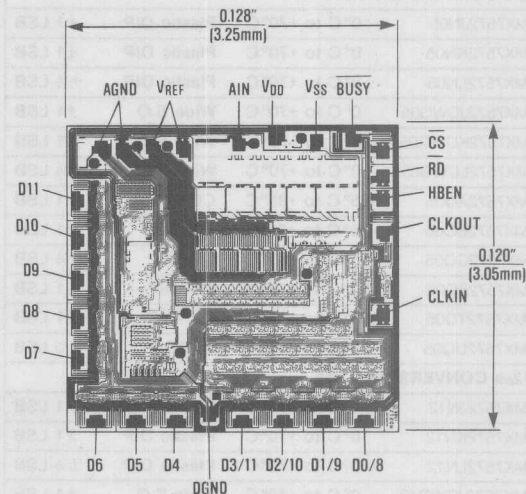


Figure 21. MAX162/MX7572 Inverting Bipolar Operation

Chip Topography



MAX162/MX7572

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Table 6. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 21

V_{IN} Range (Volts)	R_1^* (k Ω)	R_2^* (k Ω)	R_3^* (k Ω)	R_z (Ω)	R_G (Ω)	$1/2\text{LSB}$ (mV)	$\text{FS}/2-3/2\text{LSBs}$ (Volts)
± 2.5	20	20.5	42.2	2000	1000	0.61	2.49817
± 5.0	20	10.2	21	1000	1000	1.22	4.99634
± 10.0	20	5.11	10.5	500	1000	2.44	9.99268

Notes:

* R_1 , R_2 , and R_3 have a 0.1% tolerance.

All resistors are standard EIA/MIL decade values.

Complete High-Speed CMOS 12-Bit ADC

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
5μs CONVERSION TIME			
MX7572JN05	0°C to +70°C	Plastic DIP	± 1 LSB
MX7572KN05	0°C to +70°C	Plastic DIP	± 1 LSB
MX7572LN05	0°C to +70°C	Plastic DIP	$\pm \frac{1}{2}$ LSB
MX7572JCWG05	0°C to +70°C	Wide S.O.	± 1 LSB
MX7572KCWG05	0°C to +70°C	Wide S.O.	± 1 LSB
MX7572LCWG05	0°C to +70°C	Wide S.O.	$\pm \frac{1}{2}$ LSB
MX7572AQ05	-25°C to +85°C	CERDIP	± 1 LSB
MX7572BQ05	-25°C to +85°C	CERDIP	± 1 LSB
MX7572CQ05	-25°C to +85°C	CERDIP	$\pm \frac{1}{2}$ LSB
MX7572SQ05	-55°C to +125°C	CERDIP	± 1 LSB
MX7572TQ05	-55°C to +125°C	CERDIP	± 1 LSB
MX7572UQ05	-55°C to +125°C	CERDIP	$\pm \frac{1}{2}$ LSB
12μs CONVERSION TIME			
MX7572JN12	0°C to +70°C	Plastic DIP	± 1 LSB
MX7572KN12	0°C to +70°C	Plastic DIP	± 1 LSB
MX7572LN12	0°C to +70°C	Plastic DIP	$\pm \frac{1}{2}$ LSB
MX7572JCWG12	0°C to +70°C	Wide S.O.	± 1 LSB
MX7572KCWG12	0°C to +70°C	Wide S.O.	± 1 LSB
MX7572LCWG12	0°C to +70°C	Wide S.O.	$\pm \frac{1}{2}$ LSB
MX7572AQ12	-25°C to +85°C	CERDIP	± 1 LSB
MX7572BQ12	-25°C to +85°C	CERDIP	± 1 LSB
MX7572CQ12	-25°C to +85°C	CERDIP	$\pm \frac{1}{2}$ LSB
MX7572SQ12	-55°C to +125°C	CERDIP	± 1 LSB
MX7572TQ12	-55°C to +125°C	CERDIP	± 1 LSB
MX7572UQ12	-55°C to +125°C	CERDIP	$\pm \frac{1}{2}$ LSB

* All devices — 24 lead packages

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MAXIM

CMOS 12-Bit A/D Converters With Track-and-Hold

General Description

The MAX163, MAX164, and MAX167 are complete CMOS sampling 12-bit analog-to-digital converters (ADCs) that combine an on-chip track-and-hold and voltage reference along with high conversion speed and low power consumption. A conversion time of 8.33 μ s includes settling time for the track-and-hold. An internal buried zener reference provides low drift with low noise.

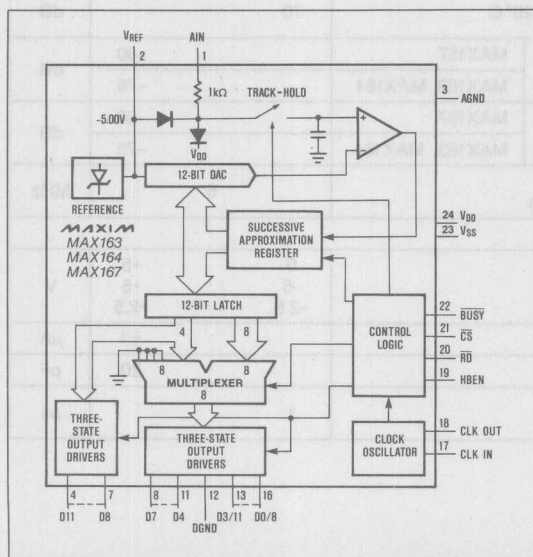
The three A/Ds differ only in their analog input range. The MAX163 accepts 0V to +5V inputs, the MAX164 accepts -5V to +5V inputs, and the MAX167's input range is -2.5V to +2.5V. External components are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry can either be driven from an external clock source or a crystal.

The MAX163/164/167 employ a standard micro-processor interface. Three-state data outputs can be configured for 8- or 12-bit data buses. Data access and bus release timing specs are compatible with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)
Audio and Telecom Processing
High Accuracy Process Control
High Speed Data Acquisition

Functional Diagram



Features

- ◆ 12-Bit Resolution
- ◆ 8.33 μ s Conversion Time
- ◆ Internal Analog Track-and-Hold
- ◆ 6MHz Full Power Bandwidth
- ◆ On-Chip Voltage Reference
- ◆ High Input Resistance (500M Ω)
- ◆ 100ns Data Access Time
- ◆ 180mW (Max) Power Consumption
- ◆ AD7572/MAX162/MAX172 Plug-In Replacement
- ◆ 24 Lead Narrow DIP and SO Packages

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX167ACNG	0°C to +70°C	Plastic DIP	$\pm\frac{1}{2}$ LSB
MAX167BCNG	0°C to +70°C	Plastic DIP	± 1 LSB
MAX167CCNG	0°C to +70°C	Plastic DIP	± 1 LSB
MAX167ACWG	0°C to +70°C	Wide SO	$\pm\frac{1}{2}$ LSB
MAX167BCWG	0°C to +70°C	Wide SO	± 1 LSB
MAX167CCWG	0°C to +70°C	Wide SO	± 1 LSB
MAX167AEWG	-40°C to +85°C	Wide SO	$\pm\frac{1}{2}$ LSB
MAX167BEWG	-40°C to +85°C	Wide SO	± 1 LSB
MAX167CEWG	-40°C to +85°C	Wide SO	± 1 LSB
MAX167CC/D	0°C to +70°C	Dice**	± 1 LSB
MAX167AENG	-40°C to +85°C	Plastic DIP	$\pm\frac{1}{2}$ LSB

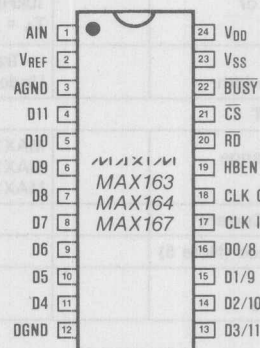
* All devices—24 lead packages

**Consult factory for dice specifications

Ordering information continued on last page.

Pin Configuration

Top View



CMOS 12-Bit A/D Converters With Track-and-Hold

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND -0.3 to +7V
V_{SS} to DGND +0.3V to -17V
AGND to DGND -0.3V to $V_{DD} + 0.3V$
AIN to AGND -15V to +15V
Digital Input Voltage to DGND -0.3V to $V_{DD} + 0.3V$ (Pins 17, 19-21)
Digital Output Voltage to DGND -0.3V to $V_{DD} + 0.3V$ (Pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges

MAX16XXC 0°C to +70°C
MAX16XXE -40°C to +85°C
MAX16XXM -55°C to +125°C
Storage Temperature Range -65°C to +160°C
Power Dissipation (any Package) 1000mW
Derates Above +75°C by 10mW/°C
Lead Temperature (Soldering 10 seconds) +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not

ELECTRICAL CHARACTERISTICS

($V_{DD} = +5V \pm 5\%$, $V_{SS} = -11.4V$ to $-15.75V$, Slow Memory Mode (see text), $T_A = T_{MIN}$ to T_{MAX} , $f_{CLK} = 1.6MHz$ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
Integral Non-Linearity	INL	MAX16XB, MAX16XC MAX167A			± 1 $\pm 1/2$	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temperature			± 1	LSB
Offset Error (Note 1)		MAX163 MAX164, MAX167			± 4 ± 6	LSB
Full Scale Error (Note 2)		$T_A = 25^\circ C$, Includes Reference Error			± 10	LSB
Full Scale Tempco (Notes 3, 5)		Excludes Internal Reference Drift			± 5	ppm/°C
Conversion Time	t_{CONV}	Synchronous (12.5 Clock Cycles) (13 Clock Cycles)			7.81 8.13	μs
Clock Frequency	f_{CLK}		0.1		1.6	MHz
DYNAMIC ACCURACY (Sample Rate = 100kHz)						
Signal to Noise plus Distortion Ratio	S/(N+D)	10kHz Input Signal, $T_A = 25^\circ C$	70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD	10kHz Input Signal, $T_A = 25^\circ C$			-80 -76	dB
Peak Harmonic or Spurious Noise		10kHz Input Signal, $T_A = 25^\circ C$			-80 -76	dB
Full Power Sampling Bandwidth		In Track Mode, Under Sampled Waveform		6		MHz
ANALOG INPUT						
Input Voltage Range (Note 4)		MAX163 MAX164 MAX167	0 -5 -2.5		+5 +5 +2.5	V
Input Leakage Current					± 1	μA
Input Capacitance (Note 5)					20	pF
Track-Hold Acquisition Time			1			μs

CMOS 12-Bit A/D Converters With Track-and-Hold

MAX163/164/167

1

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +5V \pm 5\%$, $V_{SS} = -11.4V$ to $-15.75V$, Slow Memory Mode (see text), $T_A = T_{MIN}$ to T_{MAX} , $f_{CLK} = 1.6MHz$ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
V_{REF} Output Voltage		$T_A = 25^\circ C$	-4.98	-5.00	-5.02	V
V_{REF} Output Tempco (Note 6)		MAX16XB, MAX16XA MAX16XC			25 45	ppm/ $^\circ C$
Reference Load Sensitivity		$\Delta FS / \Delta I_{REF}$, I_{REF} Load Change: 0 to 5mA		0.2	1	LSB/mA
Output Sink Current					5	mA
LOGIC INPUTS						
Input Low Voltage	V_{IL}	\overline{CS} , \overline{RD} , HBEN, CLK IN			0.8	V
Input High Voltage	V_{IH}	\overline{CS} , \overline{RD} , HBEN, CLK IN	2.4			V
Input Capacitance (Note 5)	C_{IN}	\overline{CS} , \overline{RD} , HBEN, CLK IN			10	pF
Input Current	I_{IN}	$V_{IN} = 0V$ to V_{DD} \overline{CS} , \overline{RD} , HBEN CLK IN			10 20	μA
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D11-D0/8, \overline{BUSY} , CLK OUT $I_{SINK} = 1.6mA$			0.4	V
Output High Voltage	V_{OH}	D11-D0/8, \overline{BUSY} , CLK OUT $I_{SOURCE} = 200\mu A$	4			V
Three-State Leakage Current	I_L	D11-D0/8, $V_{OUT} = 0V$ to V_{DD}			± 10	μA
Three-State Output Capacitance	C_O	(Note 5)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	$\pm 5\%$ For Specified Performance		5		V
Negative Supply Voltage	V_{SS}	$\pm 5\%$ For Specified Performance	-12		-15	V
Positive Supply Rejection		FS Change, $V_{SS} = -15V$ or $-12V$ $V_{DD} = 4.75V$ to $5.25V$		$\pm 1/2$		LSB
Negative Supply Rejection		FS Change, $V_{DD} = 5V$ $V_{SS} = -14.25V$ to $-15.75V$ $V_{SS} = -11.4V$ to $-12.6V$		$\pm 1/8$ $\pm 1/8$		LSB
Positive Supply Current	I_{DD}	$\overline{CS} = \overline{RD} = V_{DD}$, $A_{IN} = 5V$		4	6	mA
Negative Supply Current	I_{SS}	$\overline{CS} = \overline{RD} = V_{DD}$, $A_{IN} = 5V$		7	10	mA
Power Dissipation		$V_{DD} = +5V$, $V_{SS} = -12V$		104	150	mW

Note 1: Typical change over temp is ± 1 LSB.

Note 2: Ideal last code transition = FS - 3/2 LSB, adjusted for offset.

Note 3: Full Scale Tempco = $\Delta FS / \Delta T$, where ΔFS is full scale change from $T_A = 25^\circ C$ to T_{MIN} or T_{MAX} .

Note 4: V_{IN} must not exceed V_{DD} for specified accuracy.

Note 5: Guaranteed by design, not subject to test.

Note 6: V_{REF} Tempco = $\Delta V_{REF} / \Delta T$, where ΔV_{REF} is reference voltage change from $T_A = 25^\circ C$ to T_{MIN} or T_{MAX} .

CMOS 12-Bit A/D Converters With Track-and-Hold

TIMING CHARACTERISTICS (See Figures 9-12)

($V_{DD} = +5V$, $V_{SS} = -12V$ or $-15V$, $T_A = T_{MIN}$ to T_{MAX} , Note 7, specifications in bold type are 100% tested, others are guaranteed by design, unless otherwise noted).

PARAMETER	SYMBOL (Figures 9-12)	CONDITIONS	$T_A = 25^\circ C$			MAX16XXC/E		MAX16XXM		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CS to \overline{RD} Setup Time	t_1		0			0		0		ns
\overline{RD} to BUSY Delay (Note 8)	t_2	$CL = 50pF$		80	170		220		260	ns
Data Access Time (Notes 8, 9)	t_3	$CL = 100pF$		50	100		130		150	ns
\overline{RD} Pulse Width	t_4		100			130		150		ns
CS to \overline{RD} Hold Time	t_5		0			0		0		ns
Data Setup Time After BUSY (Notes 8, 9)	t_6			40	80		105		120	ns
Bus Relinquish Time (Notes 8, 10)	t_7			30	50		65		75	ns
HBEN to \overline{RD} Setup Time	t_8		0			0		0		ns
HBEN to \overline{RD} Hold Time	t_9		0			0		0		ns
Delay Between READ Operations	t_{10}		200			200		200		ns
Delay Between Conversions	t_{11}		1			1		1		μs
Aperture Delay	t_{12}	Jitter $< 50ps$		25						ns
CLK to BUSY Delay	t_{13}		80	170		220		260		ns

Note 7: All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 8: This specification is 100% production tested.

Note 9: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 10: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Positive Supply Voltage	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$
Negative Supply Voltage	$V_{SS} = -12V$ or $-15V$	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$	$V_{SS} = -12V$ or $-15V$	$V_{DD} = +5V$	$V_{SS} = -12V$ or $-15V$
Positive Supply Current	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$
Negative Supply Current	$I_{SS} = 10\mu A$	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$	$I_{SS} = 10\mu A$	$I_{DD} = 10\mu A$	$I_{SS} = 10\mu A$
Power Dissipation	$P_D = 100mW$	$P_D = 100mW$	$P_D = 100mW$	$P_D = 100mW$	$P_D = 100mW$	$P_D = 100mW$	$P_D = 100mW$	$P_D = 100mW$	$P_D = 100mW$	$P_D = 100mW$

CMOS 12-Bit A/D Converters With Track-and-Hold

Pin Description

PIN	NAME	FUNCTION
1	AIN	Sampling Analog Input, MAX163: 0V to +5V Unipolar MAX164: $\pm 5V$ Bipolar MAX167: $\pm 2.5V$ Bipolar
2	V _{REF}	-5.00V Reference Output
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3/11-D0/8	Three-State Data Outputs
17	CLK IN	Clock Input. An external TTL compat- ible clock may be connected, or a crystal may be connected between CLK IN and CLK OUT.
18	CLK OUT	Clock Output. An inverted CLK IN signal appears at this pin.
19	HBEN	High Byte Enable Input. Used to multi- plex the internal 12-bit conversion result into the lower order outputs (D7-D0/8). HBEN also disables conver- sion starts when HIGH.
20	\overline{RD}	READ Input. This active low input starts a conversion when \overline{CS} and HBEN are low. \overline{RD} also enables the output drivers when \overline{CS} is low.
21	\overline{CS}	The CHIP SELECT Input must be low for the ADC to recognize \overline{RD} and HBEN inputs.
22	\overline{BUSY}	The \overline{BUSY} Output is low when a con- version is in progress.
23	V _{SS}	Negative Supply, -15V or -12V
24	V _{DD}	Positive Supply, +5V

A/D Converter Operation

The MAX163/164/167 use successive approximation and input track-and-hold circuitry to convert an analog signal to a series of 12-bit digital output codes. The control logic provides easy interface to microprocessors so that most applications require only passive components to perform analog-to-digital conversions. No "hold" capacitor is required. Figure 3 shows the MAX163/164/167 in their simplest operational configuration.

Analog Input—Track-and-Hold

In Figure 4, the equivalent input circuit illustrates the sampling architecture of the ADC's analog comparator. The comparator's input capacitance acts as the "hold" capacitor and must be completely charged by the input signal with every A/D conversion (but NOT every clock cycle). The capacitance is charged through an internal 1k Ω protection resistor in series with the input.

To an input signal, AIN appears as a capacitor switching between analog ground and the input signal. Between conversions (BUSY high and RD or CS or HBEN high) the capacitor is connected to AIN. When a conversion starts, the capacitor disconnects from AIN, thus sampling the input, and is internally discharged. At the end of the conversion it reconnects to the input and charges to the input signal. The loading effect of AIN on the analog signal is such that a high speed input buffer is usually NOT needed. This is because the A/D disconnects from the input during the actual conversion.

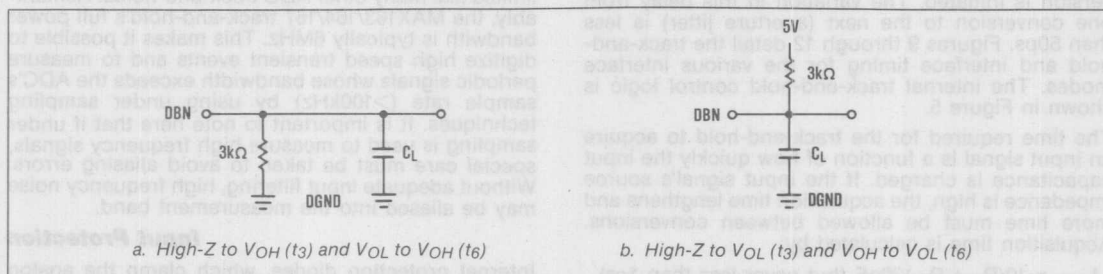


Figure 1. Load Circuits for Access Time

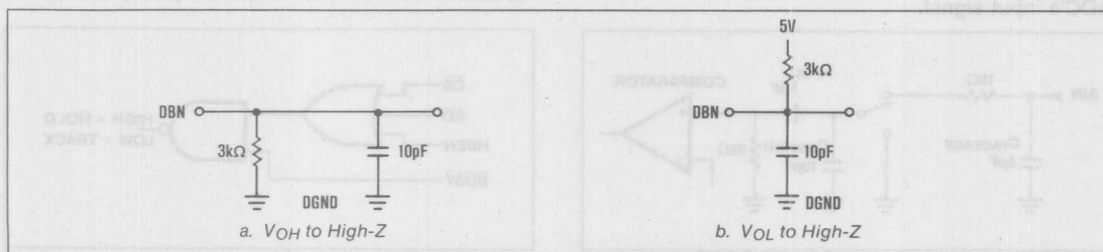


Figure 2. Load Circuits for Bus Relinquish Time

CMOS 12-Bit A/D Converters With Track-and-Hold

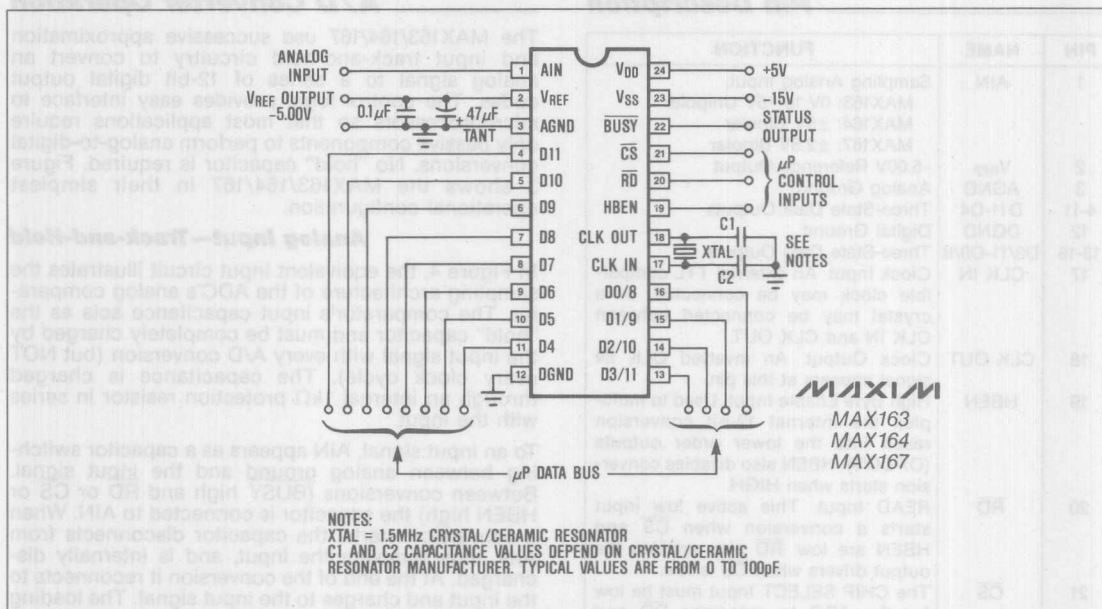


Figure 3. MAX163/164/167 Operational Diagram

The track-and-hold enters its "tracking" mode when the ADC is deselected (CS high) and BUSY is high. "Hold" mode starts approximately 25ns after a conversion is initiated. The variation in this delay from one conversion to the next (aperture jitter) is less than 50ps. Figures 9 through 12 detail the track-and-hold and interface timing for the various interface modes. The internal track-and-hold control logic is shown in Figure 5.

The time required for the track-and-hold to acquire an input signal is a function of how quickly the input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 10(R_S + R_{IN})20pF \text{ (but never less than } 1\mu s)$$

Where $R_{IN} = 1k\Omega$, and R_S = source impedance of the ADC's input signal.

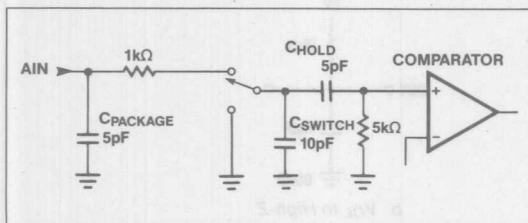


Figure 4. Equivalent Input Circuit

Input Bandwidth

The A/D's input tracking circuitry has excellent large signal and wide bandwidth behavior. It is not slew limited like many other ADC track-and-holds. Remarkably, the MAX163/164/167 track-and-hold's full power bandwidth is typically 6MHz. This makes it possible to digitize high speed transient events and to measure periodic signals whose bandwidth exceeds the ADC's sample rate (>100kHz) by using under sampling techniques. It is important to note here that if under sampling is used to measure high frequency signals, special care must be taken to avoid aliasing errors. Without adequate input filtering, high frequency noise may be aliased into the measurement band.

Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{REF} , work with an internal series resistance to allow over drives of up to $\pm 15V$ at AIN

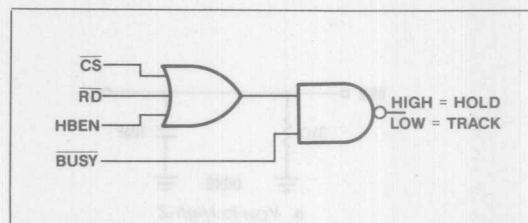


Figure 5. Track-Hold Internal Control Logic

CMOS 12-Bit A/D Converters With Track-and-Hold

MAX163/164/167

with no risk of damage to the A/D. However, for accurate conversions near full scale (MAX163 and MAX164 only), AIN should not exceed V_{DD} because A/D accuracy is affected while the protection diodes are even slightly turned on.

Starting a Conversion

The ADC is controlled by the \overline{CS} , \overline{RD} and HBEN inputs. The track-and-hold enters Hold Mode and a conversion starts at the falling edge of \overline{CS} and \overline{RD} while HBEN is low. The BUSY output goes low as soon as the conversion starts. On the falling edge of the 13th input clock pulse after the conversion starts, BUSY goes high and the conversion result is latched into three-state output buffers.

Internal/External Clock

Figure 6 shows the MAX163/164/167 clock circuitry. The capacitive load on the CLK OUT pin must be minimized to avoid digital coupling of the CLK OUT buffer currents to the ADC's analog comparator. If an external clock source drives CLK IN, then CLK OUT should be left open. Acceptable external clock duty cycles are between 20% and 80%, so a precise square wave is not required. If the internal oscillator is used, a crystal or ceramic resonator is connected between CLK OUT and CLK IN as shown in Figure 6.

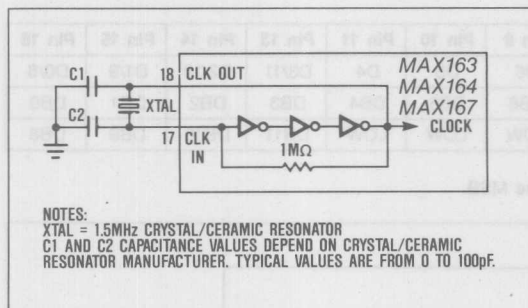


Figure 6. Internal Clock Circuit

Internal Reference

The MAX163/164/167 have a -5.00V buried zener reference which biases the internal DAC. The reference output is available at V_{REF} (Pin 2) and should be bypassed to AGND (Pin 3) with a 47 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor. This minimizes noise and maintains a low impedance at high frequencies. A resistor should NOT be connected between the bypass capacitors and Pin 2. The internal reference output buffer can sink up to 5mA.

Digital Interface

Clock and Control Synchronization

For best analog performance, the MAX163/164/167 clock should be synchronized to the \overline{RD} and \overline{CS} control inputs as shown in Figure 7, with at least

100ns separating convert start from the nearest clock edge. This ensures that transitions at CLK IN and CLK OUT do not couple to the analog input and get sampled by the track-and-hold. The magnitude of this feedthrough is only a few millivolts, but if CLK and convert start (\overline{CS} and \overline{RD}) are asynchronous, frequency components caused by mixing of the clock and convert signals may increase the apparent input noise.

When the clock and convert signals are synchronized, small endpoint errors (offset and full scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be eliminated by ensuring that the start of a conversion (\overline{RD} and \overline{CS} falling edge) does not occur within 100ns of a clock transition, as in Figure 7. Nevertheless, even without observing this guideline, the MAX163/164/167 are still compatible with either the MAX162/172 or the MX7572 synchronization modes, with no increase in linearity error. This means that either the falling or rising edge of CLK IN may be near \overline{RD} 's falling edge.

Output Data Format

The 12 data bits can be output either in full parallel or as two 8-bit bytes. The data bus output format is shown in Table 1. To obtain parallel output for 16-bit processors, HBEN is permanently tied low. The output data, DB11-DB0, is then right justified, i.e., DB0, the LSB, is the right most bit in the 16-bit word.

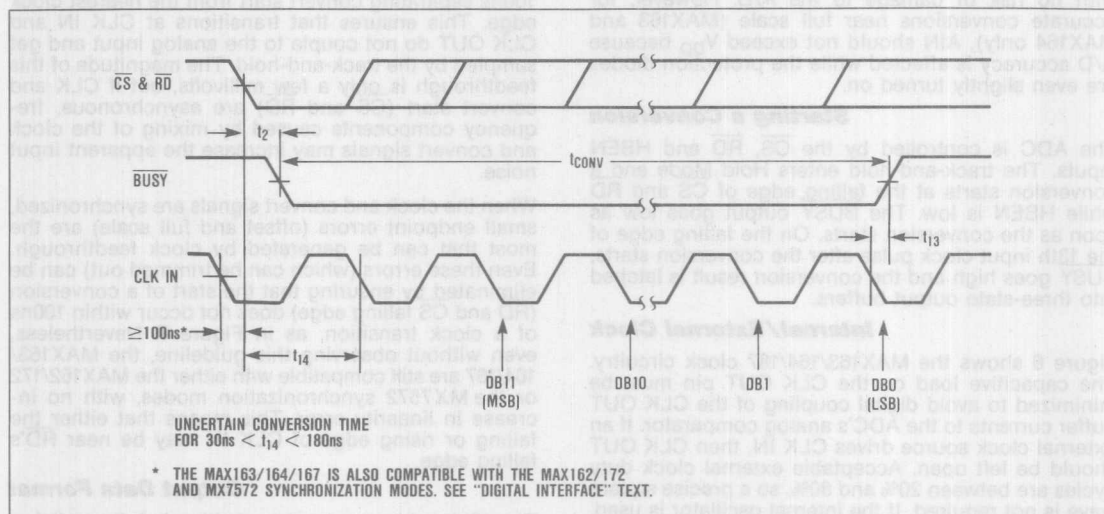
For a two byte read, outputs D7 through D0/8 are used. Byte selection is controlled by HBEN which multiplexes the data outputs. When HBEN is low, the lower 8 bits are presented at the data outputs. When HBEN is high, the upper 4 bits are presented at DB0-DB3 with the leading 4 bits low in locations D4-D7. Note that the 4 MSBs always appear at D11-D8 whenever the outputs are enabled, regardless of the state of HBEN.

Timing And Control

Conversion start and data read operations are controlled by three digital inputs, HBEN, \overline{CS} and \overline{RD} . Figure 8 shows the logic equivalent for the conversion and data output control circuitry. A logic low is required on all three inputs to start a conversion and once the conversion is in progress, it cannot be re-started. BUSY remains low during the entire conversion cycle.

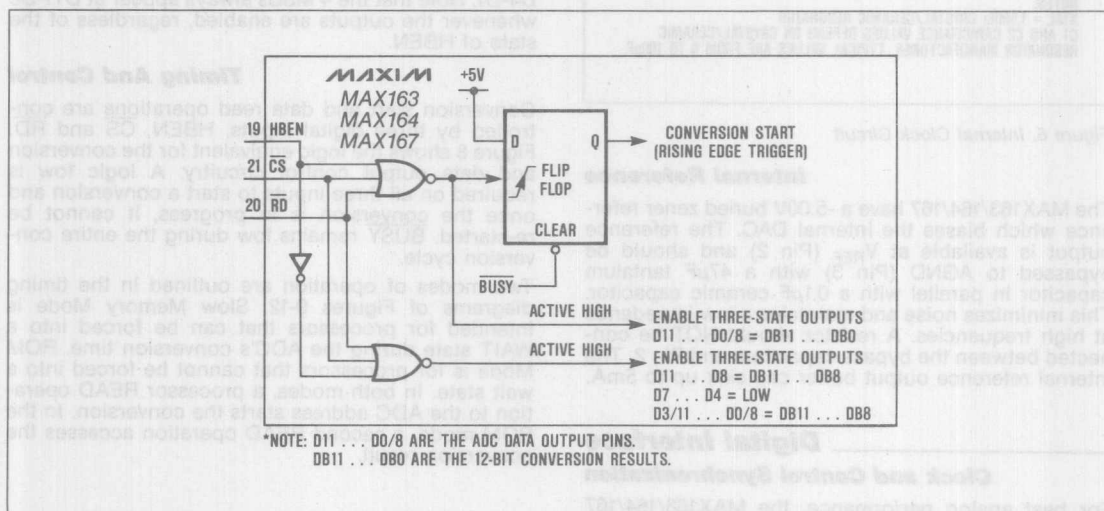
Two modes of operation are outlined in the timing diagrams of Figures 9-12. Slow Memory Mode is intended for processors that can be forced into a WAIT state during the ADC's conversion time. ROM Mode is for processors that cannot be forced into a wait state. In both modes, a processor READ operation to the ADC address starts the conversion. In the ROM mode, a second READ operation accesses the conversion result.

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Figure 7. $\overline{\text{RD}}$ and CLK IN for Synchronous OperationTable 1. Data Bus Output, $\overline{\text{CS}}$ & $\overline{\text{RD}} = \text{LOW}$

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Note: *D11 ... D0/8 are the ADC data output pins.
DB11 ... DB0 are the 12-bit conversion results, DB11 is the MSB.

Figure 8. Logic Equivalent for $\overline{\text{RD}}$, $\overline{\text{CS}}$ and HBEN Inputs

CMOS 12-Bit A/D Converters With Track-and-Hold

MAX163/164/167

Slow Memory Mode, Parallel Read (HBEN = LOW)

See Figure 9 and Table 2. Taking \overline{CS} and \overline{RD} low starts the conversion. $BUSY$ remains low while the conversion is in progress. The PREVIOUS (old) result appears at the digital outputs until the end of the conversion when $BUSY$ returns high. The output latches are then updated with the newest result on D11-D0/8.

Slow Memory Mode, Two Byte Read

See Figure 10 and Table 3. Outputs D7-D0/8 are used for a two byte read. The start and read operations for the 8 LSBs are identical to the Slow Memory Mode, Parallel Read. A second read operation with $HBEN$ high places the 4 MSBs, with 4 leading zeros, on data outputs D7-D0/8. This second read operation does not start another conversion since $HBEN$ is high.

ROM Mode, Parallel Read (HBEN = LOW)

See Figure 11 and Table 4. ROM Mode avoids using processor wait states. A conversion starts with a read operation and the 12 data bits from the PREVIOUS conversion appear at D11-D0/8. The data from the first read in a sequence is often disregarded when this interface mode is used. A second read accesses the results of the first conversion and also starts a new conversion. The time between successive READS must be longer than the MAX163/164/167 conversion times.

ROM Mode, Two Byte Read

See Figure 12 and Table 5. As in the Slow Memory Mode, only D7-D0/8 are used for two byte reads. A conversion starts with a read operation with $HBEN$ low. At this point the data outputs contain the 8 LSBs from the PREVIOUS conversion. Two more read operations are needed to access the conversion result. The first occurs with $HBEN$ high, where the 4 MSBs with 4 leading zeros are accessed. The second read, with $HBEN$ low, outputs the 8 LSBs and also starts a new conversion.

Application Hints

Initialization After Power Up

In some applications it may be desirable to remove power from the ADC during periods of inactivity. This is increasingly common in battery powered systems. To initialize the MAX163/164/167 at power up, perform a read operation with $HBEN$ low and ignore the data outputs.

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, errors can be caused by coupling from the data pins to the ADC comparator. Using the Slow Memory Mode avoids this problem by placing the processor in a wait state during the conversion. In the ROM Mode, if the data bus is going to be active during the conversion, the bus should be isolated from the ADC using three-state drivers.

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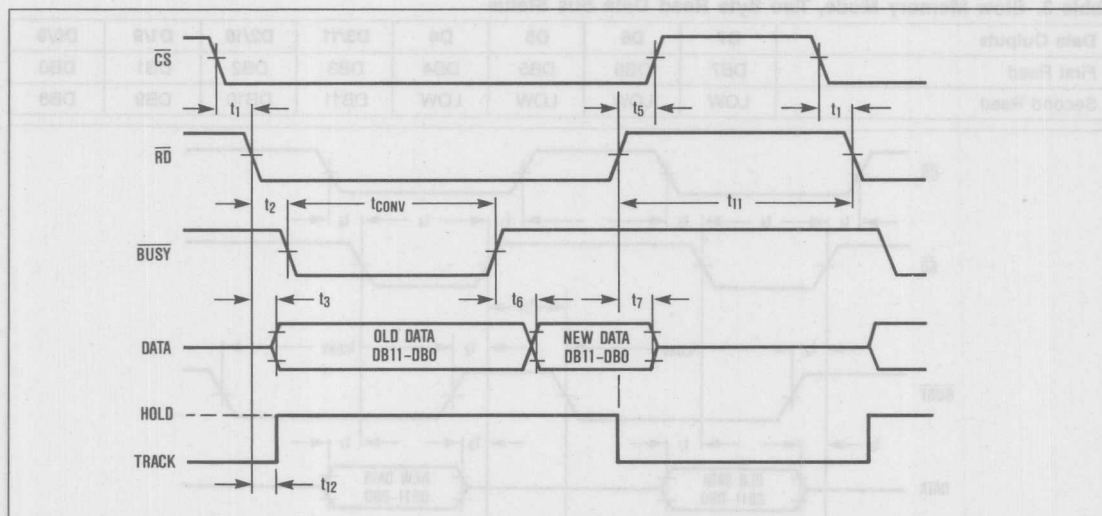


Figure 9. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

CMOS 12-Bit A/D Converters With Track-and-Hold

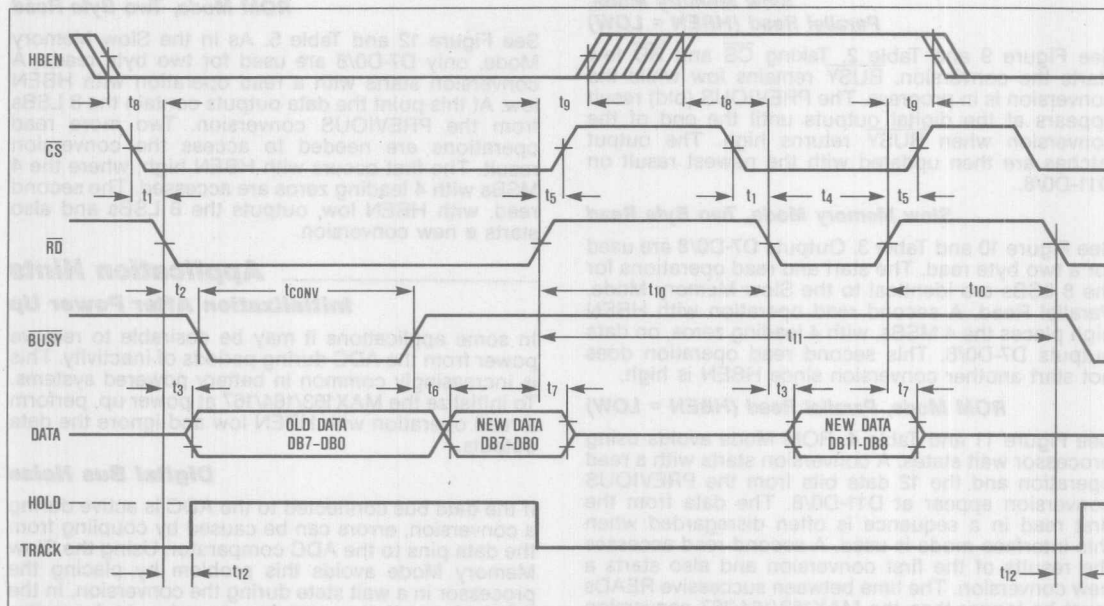


Figure 10. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

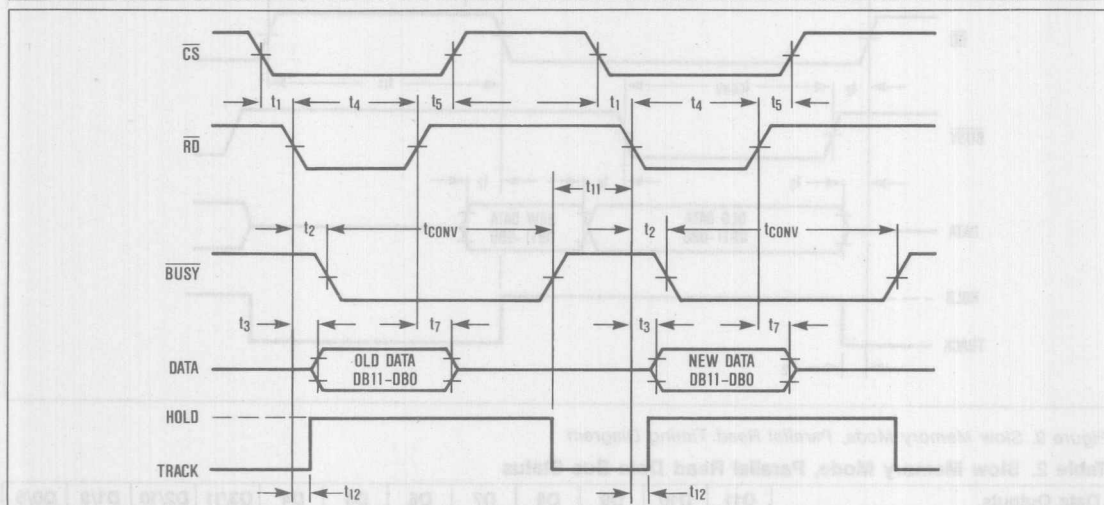


Figure 11. ROM Mode, Parallel Read Timing Diagram

CMOS 12-Bit A/D Converters With Track-and-Hold

MAX163/164/167

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Table 4. ROM Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

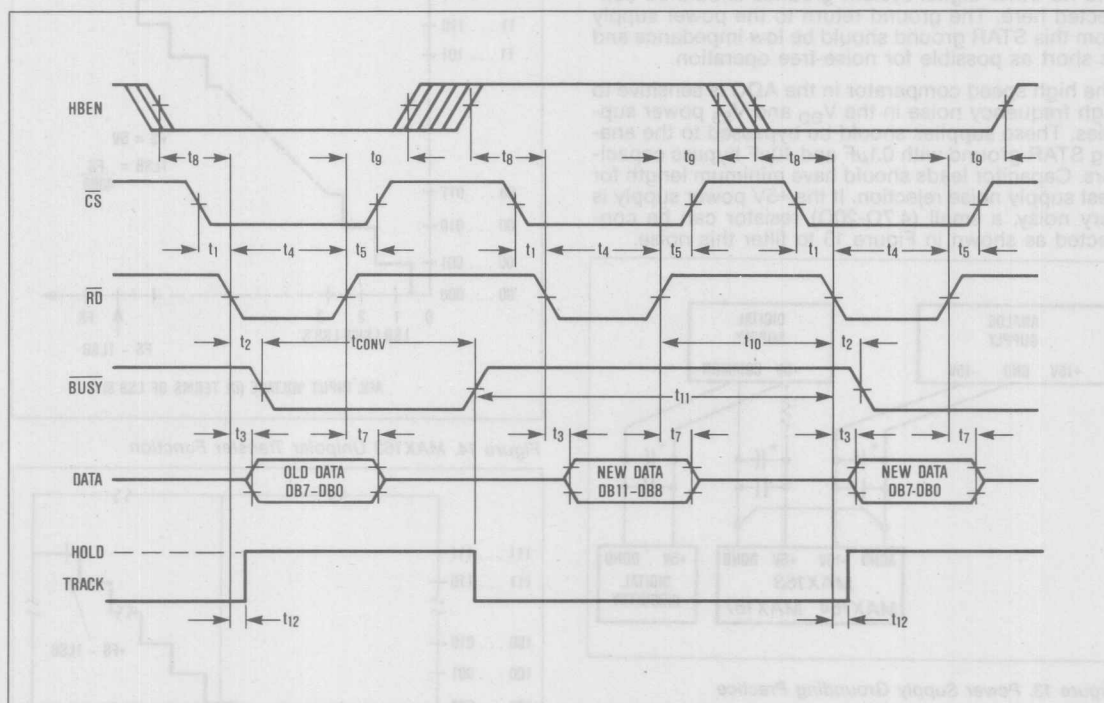


Figure 12. ROM Mode, Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

In ROM Mode, considerable digital noise is generated in the ADC when RD or CS go high and the output data drivers are disabled after a conversion is started. This noise can affect the ADC comparator and cause large errors if it coincides with the time the SAR is latching a comparator decision. To avoid this problem, RD and CS should be active for less than one clock cycle. If this is not possible, RD or CS must go high at a rising edge of CLK IN, since the comparator output is always latched at falling edges of CLK IN.

Layout, Grounding, Bypassing

For best system performance printed circuit boards should be used. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package.

CMOS 12-Bit A/D Converters With Track-and-Hold

Figure 13 shows the recommended system ground connections. A single point analog STAR ground should be established at Pin 3 (AGND) separate from the logic ground. All other analog grounds and Pin 12 (DGND) should be connected to this STAR ground and no other digital system grounds should be connected here. The ground return to the power supply from this STAR ground should be low impedance and as short as possible for noise-free operation.

The high speed comparator in the ADC is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be bypassed to the analog STAR ground with $0.1\mu\text{F}$ and $10\mu\text{F}$ bypass capacitors. Capacitor leads should have minimum length for best supply noise rejection. If the +5V power supply is very noisy, a small (4.7Ω - 20Ω) resistor can be connected as shown in Figure 13 to filter this noise.

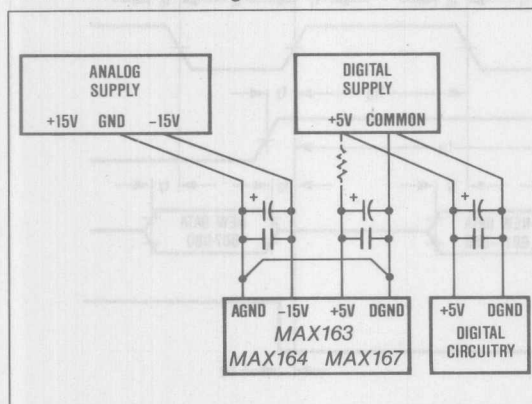


Figure 13. Power Supply Grounding Practice

Gain and Offset Adjustment

The plot in Figure 14 graphs the nominal unipolar input/output transfer function of the MAX163. Code transitions occur half way between successive integer LSB values. Output coding is natural binary with 1 LSB = 1.22mV ($5\text{V}/4096$). Figure 15 shows the bipolar input transfer function for the MAX164/167, where output coding is offset binary.

In applications where gain (full scale range) adjustment is required, the connection shown in Figure 16 provides $\pm 0.5\%$, or ± 20 LSBs, of adjustment range. If both offset and full scale range need adjustment, the circuit in Figure 17 is recommended. Offset should be adjusted before gain. For the MAX163 (0V to +5V input range), apply $+1/2$ LSB (0.61mV) to the analog input and adjust R12 so the digital output code changes between 0000 0000 0000 and 0000 0000 0001. To adjust full scale, apply $\text{FS} - 1/2$ LSB (4.99817V) and adjust R8 until the output code changes between 1111 1110 and 1111 1111 1111. There may be slight interaction between adjustments. If an input gain of two is acceptable, the connection in Figure 17 can be simplified by removing R5 and R6.

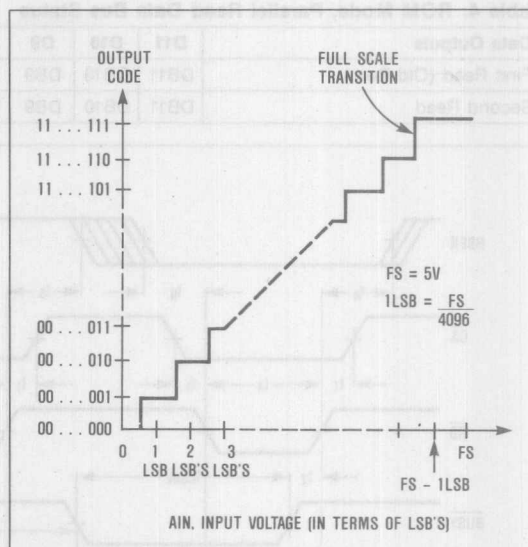


Figure 14. MAX163 Unipolar Transfer Function

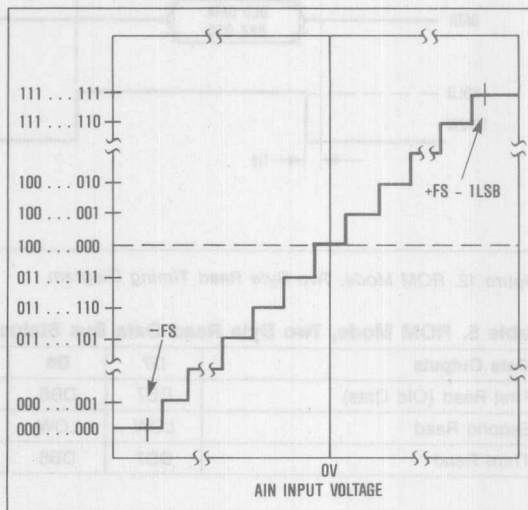


Figure 15. MAX164/167 Bipolar Transfer Function

To adjust bipolar offset (MAX164 $\pm 5\text{V}$, MAX167 $\pm 2.5\text{V}$), apply $+1/2$ LSB (1.22mV for MAX164, 0.61mV for MAX167) to the analog input and adjust R12 for output code flicker between 1000 0000 0000 and 1000 0000 0001. For full scale, apply $\text{FS} - 1/2$ LSB ($+4.99634\text{V}$ for the MAX164, 2.49817V for the MAX167) to the input and adjust R8 so the output code flickers between 1111 1111 1110 and 1111 1111 1111. There may be some interaction between these adjustments.

CMOS 12-Bit A/D Converters With Track-and-Hold

Signal-to-Noise Ratio and Effective Number of Bits

The ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the Signal-to-Noise Ratio (SNR). The output band is limited to frequencies above DC and below one half the A/D sample (conversion) rate. This usually (but not always) includes distortion as well as noise components. For this reason the ratio is sometimes referred to as "Signal-to-Noise + Distortion".

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the A/D's resolution: $SNR = (6.02N + 1.76)dB$, where N is the number of bits of resolution. A perfect 12-bit A/D can, therefore, do no better than 74dB. Figure 18 shows the result of sampling a pure 10kHz sinusoid at a 100kHz rate with the MAX167. An FFT plot of the output shows the output level in various spectral bands.

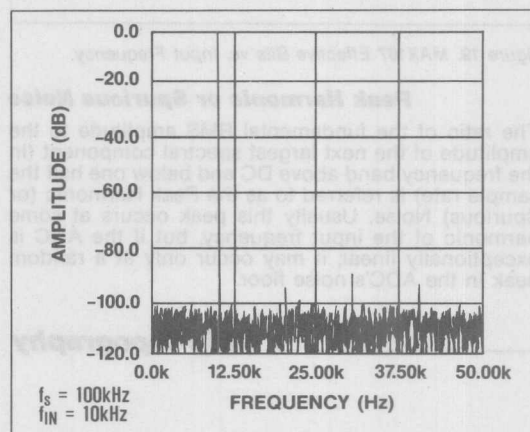


Figure 18. FFT Plot for the MAX167

By transposing the equation which converts resolution to SNR, we can, from the measured SNR, determine the effective resolution or the "Effective Number of Bits" that the A/D provides: $N = (SNR - 1.76)/6.02$. Figure 19 shows the effective number of bits as a function of the input frequency for the MAX167.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one half the sample rate) to the fundamental itself is Total Harmonic Distortion (THD). This is expressed as:

$$THD = 20\text{Log}\left[\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + \dots + V_N^2)/V_1^2}\right]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

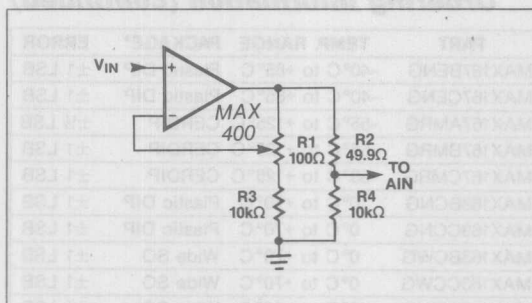


Figure 16. Trim Circuit for Gain Only ($\pm 0.5\%$)

Dynamic Performance

High speed sampling capability and 100kHz throughput make the MAX163/164/167 ideal for wideband signal processing. To support these and other related applications, FFT (Fast Fourier Transform) test techniques are used to guarantee the A/D's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm which determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency.

A-to-D converters have traditionally been evaluated by specifications such as Zero and Full Scale Error, Integral Non-linearity (INL), and Differential Non-linearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals but are less useful in signal processing applications where the A/D's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

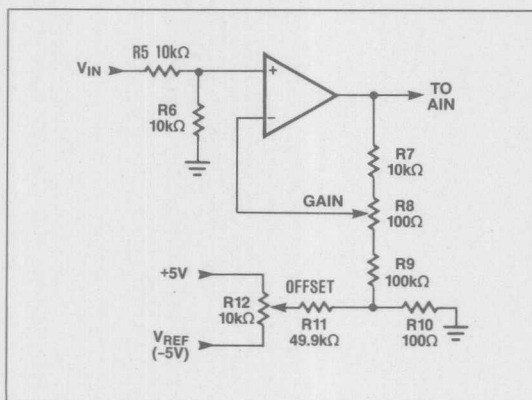


Figure 17. Offset ($\pm 20mV$) and Gain ($\pm 0.5\%$) Trim Circuit

CMOS 12-Bit A/D Converters With Track-and-Hold

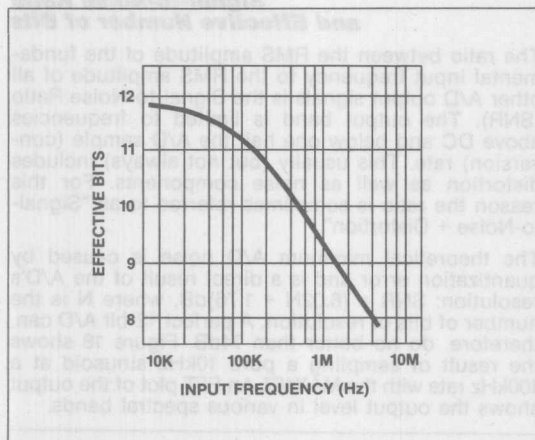
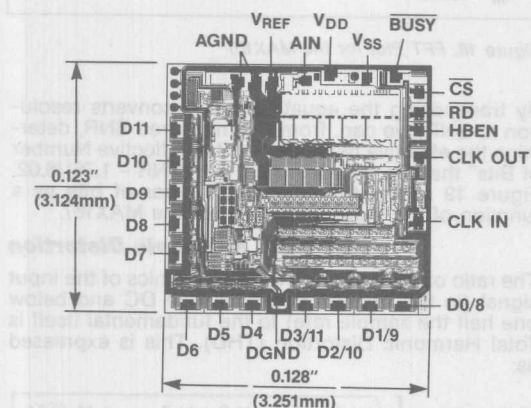


Figure 19. MAX167 Effective Bits vs. Input Frequency

Peak Harmonic or Spurious Noise

The ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one half the sample rate) is referred to as the Peak Harmonic (or Spurious) Noise. Usually this peak occurs at some harmonic of the input frequency, but if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Chip Topography



Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX167BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX167CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX167AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX167BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX167CMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX163BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX163CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX163BCWG	0°C to +70°C	Wide SO	±1 LSB
MAX163CCWG	0°C to +70°C	Wide SO	±1 LSB
MAX163BEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX163CEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX163CC/D	0°C to +70°C	Dice**	±1 LSB
MAX163BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX163CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX163BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX163CMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX164BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX164CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX164BCWG	0°C to +70°C	Wide SO	±1 LSB
MAX164CCWG	0°C to +70°C	Wide SO	±1 LSB
MAX164BEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX164CEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX164CC/D	0°C to +70°C	Dice**	±1 LSB
MAX164BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX164CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX164BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX164CMRG	-55°C to +125°C	CERDIP	±1 LSB

* All devices—24 lead packages

**Consult factory for dice specifications

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MAXIM

CMOS μ P Compatible 5 μ s, 8-Bit A/D Converters

MAX165/MAX166

1

General Description

The MAX165/MAX166 are high-speed (5 μ s) microprocessor (μ P) compatible 8-bit ADCs with Track-and-Hold (T/H). The T/H function allows full-scale signals up to 50kHz (386mV/ μ s slew rate) to be acquired and digitized accurately. Both ADCs use a successive approximation technique to achieve their fast conversions and low-power dissipation. The MAX165/MAX166 operate with a +5V supply, an internal or external +1.23V reference, and accept single-ended (MAX165) or differential (MAX166) voltages ranging from 0V to 2VREF.

The MAX165/MAX166 are easily interfaced to all popular 8-bit μ Ps through standard CS and RD control signals. These signals control the start of conversions and data access. A BUSY signal indicates the beginning and end of conversions. Since all the data outputs are latched and three-state buffered, the MAX165/MAX166 can be directly tied to a μ P data bus or system I/O port.

The MAX165 is a plug-in replacement, with an internal 1.23V reference, for the AD7575. For applications that require a differential analog input and an internal reference, the MAX166 is recommended.

Applications

- Digital Signal Processing
- High-Speed Data Acquisition
- Telecommunications
- Audio Systems
- High-Speed Servo Loops
- Low-Power Data Loggers

Features

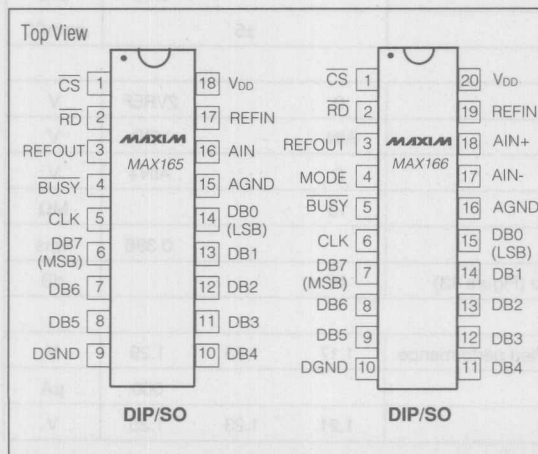
- ◆ 5 μ s Conversion Time
- ◆ Built-in (T/H) Function
- ◆ ± 1 LSB Max Total Unadjusted Error
- ◆ 50kHz Signal Bandwidth
- ◆ Internal 1.23V Bandgap Reference and Buffer
- ◆ Single +5V Supply Operation
- ◆ 8-Bit μ P Interface
- ◆ 100ns Data Access Time
- ◆ 15mW Typ Power Consumption
- ◆ Small Footprint Packages
- ◆ Plug-In Upgrade to the AD7575 (MAX165)

Ordering Information

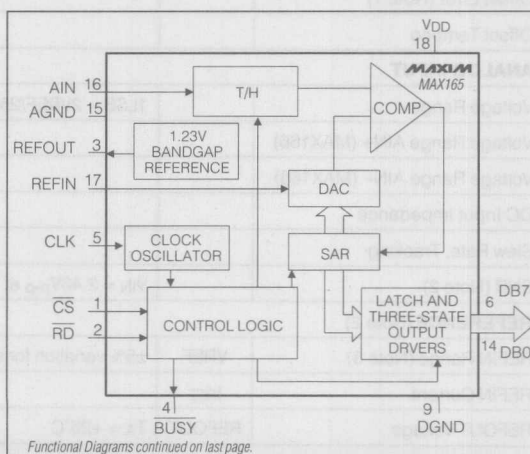
PART	TEMP. RANGE	PIN-PACKAGE	ERROR
MAX165ACPN	0°C to +70°C	18 Plastic DIP	1/2 LSB
MAX165BCPN	0°C to +70°C	18 Plastic DIP	1 LSB
MAX165ACWN	0°C to +70°C	18 Wide SO	1/2 LSB
MAX165BCWN	0°C to +70°C	18 Wide SO	1 LSB
MAX165AEPN	-40°C to +85°C	18 Plastic DIP	1/2 LSB
MAX165BEPN	-40°C to +85°C	18 Plastic DIP	1 LSB
MAX165AEPN	-40°C to +85°C	18 Wide SO	1/2 LSB
MAX165BEPN	-40°C to +85°C	18 Wide SO	1 LSB
MAX165AMJN	-55°C to +125°C	18 CERDIP	1/2 LSB
MAX165BMJN	-55°C to +125°C	18 CERDIP	1 LSB

Ordering Information continued on last page.

Pin Configurations



Functional Diagrams



Functional Diagrams continued on last page.

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CMOS μ P Compatible 5 μ s, 8-Bit A/D Converters

MAX165/MAX166

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND -0.3V, +7V
V_{DD} to DGND -0.3V, +7V
AGND to DGND -0.3V, $V_{DD} + 0.3V$
Digital Input Voltage to DGND	
(MAX165 Pins 1, 2) -0.3V, $V_{DD} + 0.3V$
(MAX166 Pins 1, 2, 4) -0.3V, $V_{DD} + 0.3V$
Digital Output Voltage to DGND	
(MAX165 Pins 4, 6-8, 10-14) -0.3V, $V_{DD} + 0.3V$
(MAX166 Pins 5, 7-9, 11-15) -0.3V, $V_{DD} + 0.3V$
CLK Input Voltage (MAX165 Pin 5) to DGND -0.3V, $V_{DD} + 0.3V$
CLK Input Voltage (MAX166 Pin 6) to DGND -0.3V, $V_{DD} + 0.3V$

REFIN, REFOUT to AGND -0.3V, $V_{DD} + 0.3V$
MAX165 AIN to AGND -0.3V, $V_{DD} + 0.3V$
MAX166 AIN+, AIN- to AGND -0.3V, $V_{DD} + 0.3V$
Power Dissipation (any package) to +75°C 450mW
Derates Above 75°C by 6mW/°C
Operating Temperature Range	
MAX165_C_, MAX166_C_ 0°C to +70°C
MAX165_E_, MAX166_E_ -40°C to +85°C
MAX165_M_, MAX166_M_ -55°C to +125°C
Storage Temperature Range -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = +5V$; REFIN = +1.23V; AGND = DGND = 0V; AIN- = 0V (MAX166); $f_{CLK} = 4MHz$ external;

$T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			8			Bits
Total Unadjusted Error		MAX165A MAX165B MAX166A/C MAX166B/D			± 1 ± 2 ± 1 ± 2	LSB
Relative Accuracy		MAX165A MAX165B MAX166A/C MAX166B/D			$\pm 1/2$ ± 1 $\pm 1/2$ ± 1	LSB
No Missing Codes Resolution			8			Bits
Full-Scale Error					± 1	LSB
Full-Scale Tempco				± 5		ppm/°C
Offset Error (Note 1)					$\pm 1/2$	LSB
Offset Tempco				± 5		ppm/°C
ANALOG INPUT						
Voltage Range		1LSB = $2V_{REF}/256$	0		$2V_{REF}$	V
Voltage Range AIN+ (MAX166)			AIN-		V_{DD}	V
Voltage Range AIN- (MAX166)			0		AIN+	V
DC Input Impedance			10			M Ω
Slew Rate, Tracking					0.386	V/ μ s
SNR (Note 2)		$V_{IN} = 2.46V_{p-p}$ at 10kHz (Figure 13)	45			dB
REFERENCE (Note 2)						
REFIN Range (Note 3)	V_{REF}	$\pm 5\%$ variation for specified performance	1.17	1.23	1.29	V
REFIN Current	I_{REF}				500	μ A
REFOUT Voltage	REFOUT	$T_A = +25^\circ C$	1.21	1.23	1.25	V

CMOS μ P Compatible 5 μ s, 8-Bit A/D Converters

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V; REFIN = +1.23V; AGND = DGND = 0V; AIN⁻ = 0V (MAX166); f_{CLK} = 4MHz external;
T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFOUT Load Regulation		T _A = +25°C, I _L = 0 to 1.5mA				3	mV
REFOUT Supply Sensitivity		V _{DD} ±5%				±1.5	mV
Temperature Drift			MAX165AC/AE/BC/BE MAX165AM/BM MAX166AC/AE/BC/BE MAX166AM/BM		40 60 40 60	70 100 70 100	ppm/°C
External Capacitive Load Requirement				4.7			μF
LOGIC INPUTS							
CS, RD, MODE (MAX166)							
Input Low Voltage	V _{INL}					0.8	V
Input High Voltage	V _{INH}			2.4			V
Input Current	I _{IN}	V _{IN} = 0 or V _{DD}	T _A = +25°C T _A = T _{MIN} to T _{MAX}			±1 ±10	μA
Input Capacitance (Note 3)	C _{IN}					10	pF
CLOCK							
Input Low Voltage	V _{INL}					0.8	V
Input High Voltage	V _{INH}			2.4			V
Input Low Current	I _{INL}	V _{IN} = 0V	MAX16__C/E MAX16__M			700 800	μA
Input High Current	I _{INH}	V _{IN} = V _{DD}	MAX16__C/E MAX16__M			700 800	μA
LOGIC OUTPUTS							
BUSY, DB0 to DB7							
Output Low Voltage	V _{OL}	I _{SINK} = 1.6mA				0.4	V
Output High Voltage	V _{OH}	I _{SOURCE} = 40μA		4.0			V
DB0 to DB7							
Floating-State Leakage Current		V _{OUT} = 0 to V _{DD}	MAX16__C/E MAX16__M			±1 ±10	μA
Floating-State Output Capacitance (Note 3)						10	pF
CONVERSION TIME (Note 4)							
With External Clock		f _{CLK} = 4MHz			5		μs
With Internal Clock		Using recommended clock components R _{CLK} = 100kΩ, C _{CLK} = 100pF, T _A = +25°C		5		15	μs
POWER REQUIREMENTS (Note 5)							
Supply Voltage	V _{DD}	±5% for specified performance			5		V
Supply Current	I _{DD}		MAX16__C/E MAX16__M		3 3	6 7	mA
Power Dissipation					15		mW
Power-Supply Rejection		4.75V < V _{DD} < 5.25V				±1/4	LSB

Note 1: Offset Error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

Note 2: REFOUT is not available for use in MAX166C/MAX166D. These parts must be used with an external reference.

Note 3: Guaranteed by design, not tested.

Note 4: Accuracy may degrade at conversion times other than those specified.

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TIMING CHARACTERISTICS (Note 6)

($V_{DD} = +5V$; $REF_{IN} = +1.23V$; $AGND = DGND = 0V$)

PARAMETER	SYMBOL	CONDITIONS	TA = 25°C		TA = Tmin to Tmax				UNITS
			All		MAX16XC/E		MAX16XM		
			MIN	MAX	MIN	MAX	MIN	MAX	
CS to RD Setup Time	t1		0		0		0		ns
RD to BUSY Propagation Time	t2			100		100		120	ns
Data Access Time after RD	t3	(Note 7)		100		100		120	ns
RD Pulse Width	t4		100		100		120		ns
CS to RD Hold Time	t5		0		0		0		ns
Data Access Time after BUSY	t6	(Note 7)		80		80		100	ns
Data Hold Time after RD	t7	(Note 8)	10	80	10	80	10	100	ns
BUSY to CS Delay	t8		0		0		0		ns

Note 5: Power-supply current is measured when MAX165/MAX166 are inactive i.e.,

For MAX165 $\overline{CS} = \overline{RD} = \overline{BUSY} = \text{High}$;

For MAX166 $\overline{CS} = \overline{RD} = \overline{BUSY} = \text{MODE} = \text{High}$.

Note 6: Timing Specifications are sample tested at $+25^\circ C$ to ensure compliance. All input control signals are specified with $t_r = t_f = 20\text{ns}$ (10% to 90% of $+5V$) and timed from a voltage level of 1.6V.

Note 7: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 8: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2. Specifications subject to change without notice.

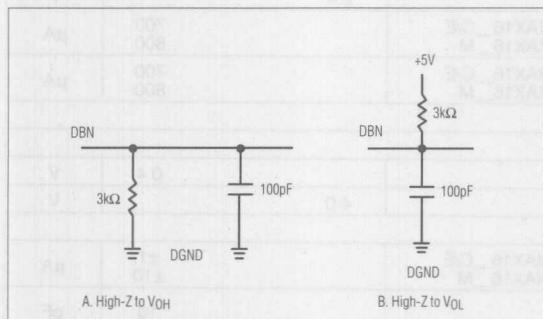


Figure 1. Load Circuits for Data Access Time Test

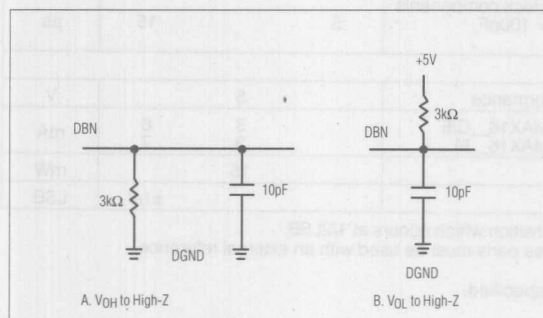


Figure 2. Load Circuits for Data Hold Time Test

Detailed Description

Converter Operation

The MAX165/MAX166 use the successive approximation technique to convert an unknown analog input voltage to an 8-bit digital output code (see Functional Diagrams). The MAX165/MAX166 sample the input voltage on an internal capacitor once at the beginning of the conversion, (see Track-and-Hold/Analog Input section). The DAC is initially set to half scale, and the comparator determines whether the input signal is larger than or smaller than half scale. If the input is larger than half scale, the DAC Most Significant Bit (MSB) is kept. But if it is smaller, the MSB is dropped. At the end of each comparison phase, the Successive Approximation Register (SAR) stores the results of the previous decisions and determines the next trial bit. This information is then loaded into the DAC after each decision. As the conversion proceeds, the analog input is approximated more closely by comparing it to the combination of the previous DAC bits and a new DAC trial bit. After 8 comparison cycles, the 8 bits stored in the SAR are latched into the output latches. At the end of the conversion, the \overline{BUSY} signal goes high, and the data in the output latches is ready for microprocessor access. Furthermore, the DAC is reset to half scale in preparation for the next conversion.

μ P Interface

The \overline{CS} and \overline{RD} logic inputs are used to initiate conversions and to access data from the devices. The MAX165/MAX166 have two common interface modes that will be

CMOS μ P Compatible 5 μ s, 8-Bit A/D Converters

Pin Description

MAX165 PIN #	MAX166 PIN #	NAME	FUNCTION
1	1	\overline{CS}	CHIP SELECT input. \overline{CS} must be low for the device to be selected, or to recognize the RD input.
2	2	\overline{RD}	READ input. \overline{RD} must be low to access data. RD is also used to start conversions. See the Digital Interface Section.
3	3	REFOUT	Output of the internal 1.23V bandgap reference.
N/A	4	MODE	MODE (MAX166). Mode = LOW puts the ADC into its Asynchronous Conversion Mode. MODE has to be tied HIGH for the Synchronous Conversion Mode and the ROM Interface Mode.
4	5	\overline{BUSY}	BUSY output. \overline{BUSY} going low indicates the start of a conversion. \overline{BUSY} going high indicates the end of a conversion.
5	6	CLK	External clock input/Internal oscillator pin for frequency setting RC components.
6	7	DB7	Three-state data output, bit 7 (MSB)

MAX165 PIN #	MAX166 PIN #	NAME	FUNCTION
7	8	DB6	Three-state data output, bit 6
8	9	DB5	Three-state data output, bit 5
9	10	DGND	Digital Ground
10	11	DB4	Three-state, data output, bit 4
11	12	DB3	Three-state, data output, bit 3
12	13	DB2	Three-state, data output, bit 2
13	14	DB1	Three-state, data output, bit 1
14	15	DB0	Three-state, data output, bit 0 (LSB)
15	16	AGND	Analog Ground
16	N/A	AIN	AIN (MAX165). Analog input (Single-Ended with respect to AGND) 0V to 2V _{REF} input range.
N/A	17	AIN-	AIN- (MAX166). Negative analog input (differential).
N/A	18	AIN+	AIN+ (MAX166). Positive analog input (differential).
17	19	REFIN	Reference input. +1.23V nominal.
18	20	V _{DD}	Power supply voltage. +5V nominal.

referred to as the Slow Memory Interface mode and the ROM Interface mode. In addition, the MAX166 has an Asynchronous Conversion mode (MODE Pin = low) where continuous conversions are performed. In the Slow Memory Interface mode, \overline{CS} and \overline{RD} are taken low to start a conversion and remain low until the end of the conversion, at which time data is updated. This mode is designed for processors that can be forced into a wait state. In the ROM Interface mode, however, the processor is not forced into a wait state. A conversion is started by taking \overline{CS} and \overline{RD} low, and data from the previous conversion is read. At the end of the most recent conversion, the processor executes a READ instruction and starts another conversion.

Slow Memory Mode

Figure 3 shows the timing diagram for the Slow Memory Interface mode. This is used with μ Ps that have a wait state capability of at least 5 μ s (such as the 8085A), where a READ instruction is extended to accommodate slow memory devices. A conversion is started by executing a memory READ to the device (taking \overline{CS} and \overline{RD} low). The \overline{BUSY} signal (which is connected to the processor

READY input) then goes low and forces the processor into a wait state. The Track-and-Hold, which had been tracking the analog input signal, holds the signal on the third falling clock edge after \overline{RD} goes low (Figure 12). At the end of the conversion, \overline{BUSY} returns high, the output latches and buffers are updated with the new conversion results, and the processor completes the memory READ by acquiring this new data.

The fast conversion time of the MAX165/MAX166 ensures that the processor is not forced into a wait state for an

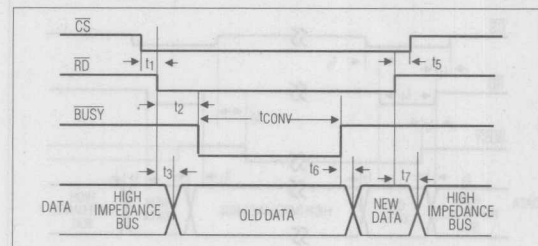


Figure 3. Slow Memory Interface Timing Diagram (MAX165/MAX166)

CMOS μ P Compatible 5 μ s, 8-Bit A/D Converters

excessive amount of time. Faster versions of many processors, including the 8085A-2, test the status of the READY input right after the start of an instruction cycle. Therefore, if the MAX165/MAX166 are to be effective in placing the processor in a wait state, its BUSY output should go low very early in the cycle. When using the 8085A-2, the earliest possible indication of an upcoming READ operation is provided by the S0 status signal. Thus, S0 which is low for a READ cycle should be connected to the RD input of the MAX165/MAX166. Figure 4 shows the connection diagram for the 8085A-2 to the MAX165/MAX166 in the Slow Memory Interface mode.

ROM Interface Mode

Figure 5 shows the timing diagram for the ROM Interface mode. In this mode, the processor does not need to be placed in a wait state. A conversion is started with a READ instruction (RD and CS go low), and old data is accessed. The BUSY signal then goes low to indicate the start of a conversion. As before, the T/H acquires the signal on the third falling clock edge after RD goes low. At the end of conversion (BUSY going high), another READ instruction always accesses the new data and normally starts a second conversion. However, if RD and CS go low within one external clock period of BUSY going high, the second conversion is not started. Furthermore,

for correct operation in this mode, \overline{RD} and \overline{CS} should not go low before BUSY returns high.

Figures 6 and 7 show the connection diagrams for interfacing the MAX165/MAX166 in the ROM Interface mode. Figure 6 shows the connection diagram to the 6502/6809 μ Ps, and Figure 7 shows the interfacing to the Z-80.

Due to their fast interface timing, the MAX165/MAX166 will interface to the TMS32010 running at up to 18MHz. Figure 8 shows the connection diagram to the TMS32010. In this interface the MAX165/MAX166 are mapped as a port address. A conversion is initiated by using an IN A and a PA instruction, and the conversion result is placed in the TMS32010 accumulator.

Asynchronous Conversion Mode (MAX166)

Tying the MODE pin low places the MAX166 into a continuous conversion mode. The RD and CS inputs are only used for reading data from the converter. Figure 9 shows the timing diagram for this mode of operation, and Figure 10 shows the connection diagram of the converter to the 8085A. In this mode, the MAX166 appears like a ROM to the μ P, in that data can be accessed independently of the clock. The output latches are normally updated on the rising edge of BUSY. But, if CS and RD

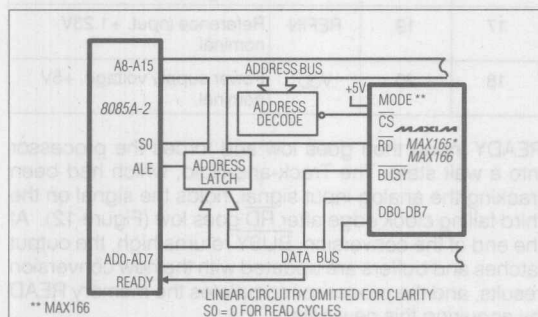


Figure 4. MAX165/MAX166 to 8085A-2 Slow Memory Interface

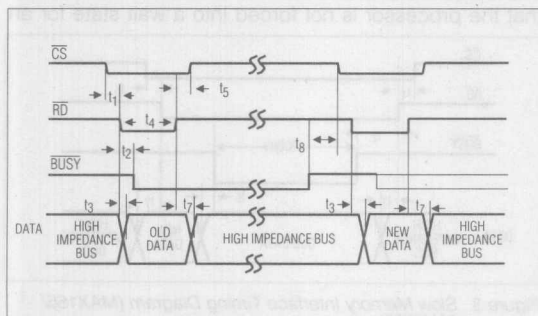


Figure 5. ROM Interface Timing Diagram

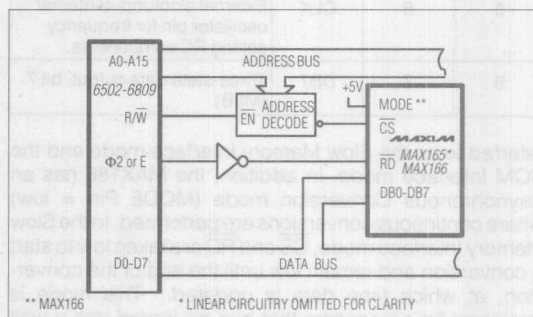


Figure 6. MAX165/MAX166 to 6502/6809 ROM Interface

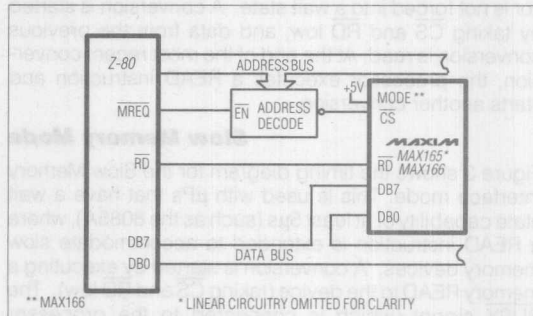


Figure 7. MAX165/MAX166 to Z-80 ROM Interface

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MAX165/MAX166

are low when $\overline{\text{BUSY}}$ goes high, the data latches are not updated until either one of these inputs returns high. Additionally, the MAX166 stops converting and $\overline{\text{BUSY}}$ stays high until $\overline{\text{RD}}$ or $\overline{\text{CS}}$ goes high. This mode of operation allows a simple interface to the μ P.

μ P Interface For Signal Acquisition

In many applications, it is necessary to sample the input signal at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In order to achieve this objective with the previously discussed interfaces, the user must match software delays or count the number of elapsed clock cycles. This becomes difficult in interrupt driven systems where the uncertainty in interrupt servicing delays is another complicating factor.

The solution is to use a real time clock to control the start of a conversion. This should be synchronous with the clock input to the ADC (both should be derived from the same source) because the sampling instants occur three clock cycles after $\overline{\text{CS}}$ and $\overline{\text{RD}}$ go low. Therefore, the sampling instants occur at exactly equal intervals if the conversions are started at equal intervals. In this scheme, the output data is fed into a FIFO latch, which allows the processor to access data at its own rate. This guarantees that data is not read from the ADC in the middle of a conversion. If data is read from the ADC during a conversion, the conversion in progress may be disturbed, but the accessed data which belonged to the previous conversion will be correct.

The T/H starts holding the input on the third falling edge of the clock after $\overline{\text{CS}}$ and $\overline{\text{RD}}$ go low. If $\overline{\text{CS}}$ and $\overline{\text{RD}}$ go low within 20ns of a falling clock edge, the ADC may or may not consider this falling edge as the first of the three edges that determine the sampling instant. Therefore, the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ should not be allowed to go low within this period when sampling accuracy is required.

Track-and-Hold (T/H)

The T/H consists of a sampling capacitor and a switch to capture the input signal. The simplified diagram of this block is shown in Figure 11. At the beginning of the conversion, switch S1 is closed, and the input signal is tracked. The input signal is held (switch S1 opens) on the third falling edge of clock after $\overline{\text{CS}}$ and $\overline{\text{RD}}$ go low (Figure 12). This allows a minimum of two clock cycles for the input capacitor to be charged to the input voltage through the switch resistance. The time that is required for the hold capacitor to settle to $\pm 1/4\text{LSB}$ is typically 7ns. Therefore, the input signal is allowed ample time to settle before it is acquired by the T/H. When a conversion ends, switch S1 closes, and the input signal is tracked.

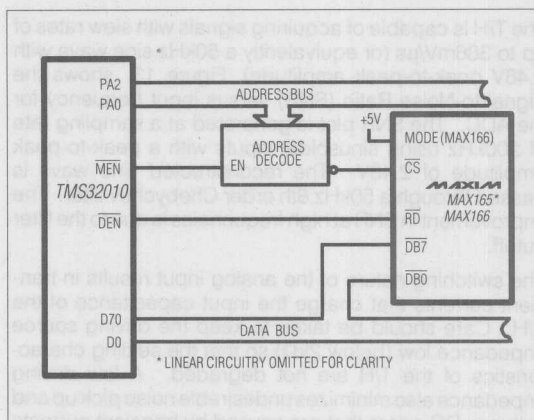


Figure 8. MAX165/MAX166 to TMS32010 ROM Interface

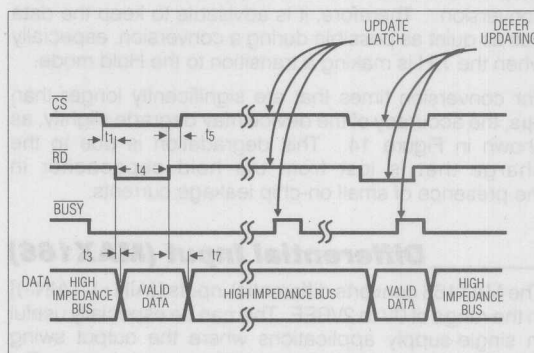


Figure 9. MAX166 Asynchronous Conversion Mode Timing Diagram

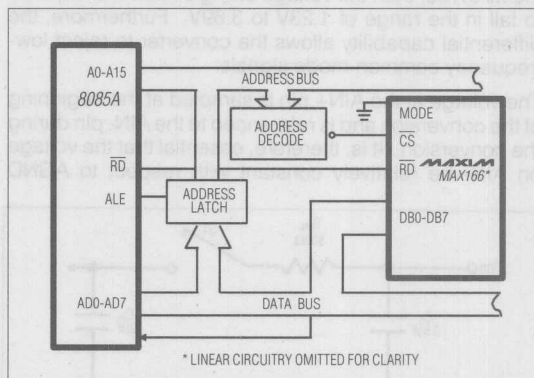


Figure 10. MAX166 to 8085A Asynchronous Conversion Mode Interface

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The T/H is capable of acquiring signals with slew rates of up to 386mV/ μ s (or equivalently a 50kHz sine wave with 2.46V peak-to-peak amplitude). Figure 13 shows the Signal-to-Noise Ratio (SNR) versus input frequency for the ADC. The SNR plot is generated at a sampling rate of 200kHz using sinusoidal inputs with a peak-to-peak amplitude of 2.46V. The reconstructed sine wave is passed through a 50kHz 8th order Chebychev filter. The improvement in SNR at high frequencies is due to the filter cutoff.

The switching nature of the analog input results in transient currents that charge the input capacitance of the T/H. Care should be taken to keep the driving source impedance low (below 2k Ω) so that the settling characteristics of the T/H are not degraded. A low driving impedance also minimizes undesirable noise pick up and reduces DC errors that are caused by transient currents at the analog input. As with any ADC, it is important to keep external sources of noise to a minimum during a conversion. Therefore, it is advisable to keep the data bus as quiet as possible during a conversion, especially when the T/H is making a transition to the Hold mode.

For conversion times that are significantly longer than 5 μ s, the accuracy of the device may degrade slightly, as shown in Figure 14. This degradation is due to the charge that is lost from the hold capacitor in the presence of small on-chip leakage currents.

Differential Input (MAX166)

The MAX166 converts differential inputs [(AIN+) - (AIN-)] in the range of 0V to 2VREF. This can be especially useful in single-supply applications where the output swing requirements on the input amplifier are reduced. For example, if the AIN- pin is tied to the reference output of the MAX166, then the voltage swing on AIN+ is required to fall in the range of 1.23V to 3.69V. Furthermore, the differential capability allows the converter to reject low-frequency common-mode signals.

The voltage at the AIN+ pin is sampled at the beginning of the conversion and is referenced to the AIN- pin during the conversion. It is, therefore, essential that the voltage on AIN- be relatively constant with respect to AGND

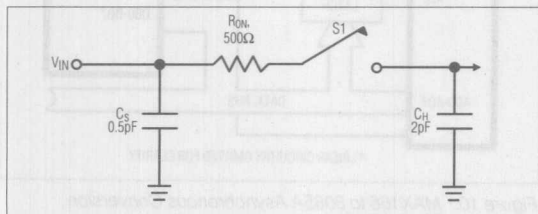


Figure 11. MAX165/MAX166 Equivalent Input Circuit

during the conversion; otherwise, conversion errors will result. If the AIN- input changes by a small voltage during the conversion, then the conversion result can be off by the same amount. For example, if the input has a 60Hz common-mode component of 0.5V with respect to AGND, an error of less than 0.1LSB is incurred during the 5 μ s conversion. The conversion errors increase with higher frequency or higher amplitude common-mode signals.

Reference Input

The high speed of this ADC can be partially attributed to the "inverted voltage output" topology of the DAC that it uses. This topology provides low offset and gain errors and fast settling times. The input current to the DAC, however, is not constant. During a conversion, as different DAC codes are tried, the DC impedance of the DAC can vary between 6k Ω and 18k Ω . Furthermore, when the DAC codes change, small amounts of transient current are drawn from the reference input. These characteristics require a low DC and AC driving impedance for the reference circuitry to minimize conversion errors.

Figure 15 shows the recommended external reference circuitry to be used for driving the reference input of the

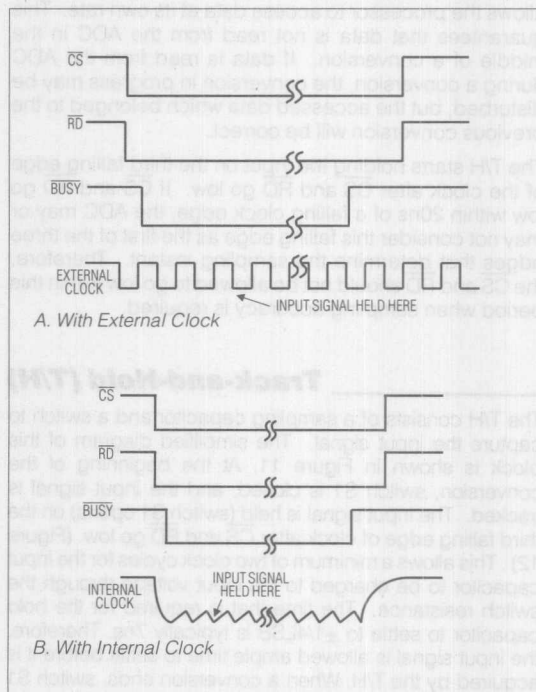


Figure 12. MAX165/MAX166 T/H (Slow Memory Interface) Timing Diagrams

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MAX165/MAX166

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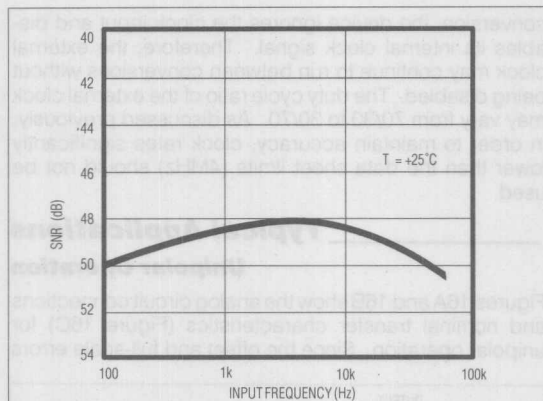


Figure 13. MAX165/MAX166 SNR vs. Input Frequency

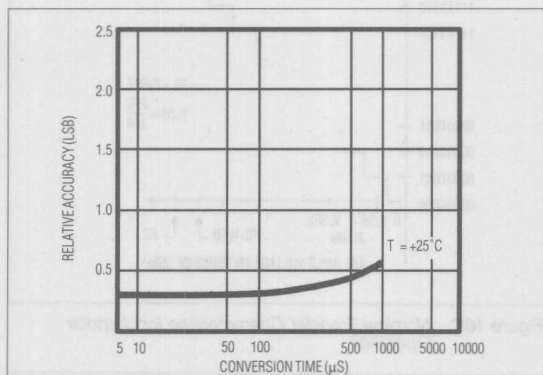


Figure 14. MAX165A/MAX166A Accuracy vs. Conversion Time

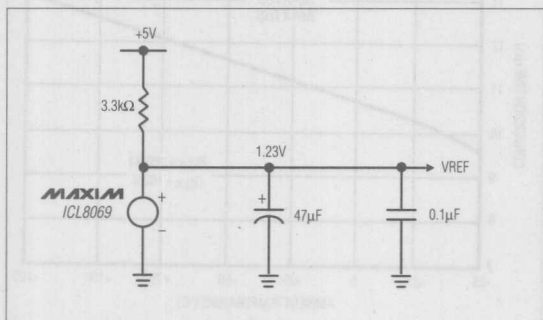


Figure 15. External Reference Circuit

MAX165/MAX166. The decoupling capacitors are necessary in order to provide a low-AC source impedance.

Internal Reference

The MAX165/MAX166 have an internal 1.23V bandgap reference and buffer suitable for driving the reference input of the ADC. As discussed before, the reference input requires a low DC and AC driving impedance.

The reference buffer requires a 4.7 μ F low ESR capacitor (tantalum or aluminum with additional 0.1 μ F ceramic) for compensation and to achieve low-AC impedance. If this capacitor is omitted, oscillations can occur on the REFOUT pin. If the user chooses to use an external reference, the REFOUT pin can be tied to V_{DD} to disable the internal reference.

Internal/External Clock

The MAX165/MAX166 can be run either with an externally applied clock or with their internal clock. In either case, the signal appearing at the clock pin is internally divided by two to provide an internal clock signal that is relatively insensitive to the input clock duty cycle. Therefore, a single conversion takes 20 input clock cycles which corresponds to 10 internal clock cycles.

Internal Clock

The internal oscillator frequency is set by an external capacitor, C_{CLK} , and an external resistor, R_{CLK} , which are connected as shown in Figure 16A. During a conversion, a sawtooth waveform is generated on the CLK pin by charging C_{CLK} through R_{CLK} and discharging it through an internal switch. At the end of a conversion, the internal oscillator is shut down by clamping the CLK pin to V_{DD} through an internal switch. The circuit for the internal oscillator can be easily overdriven with an external clock source.

The internal oscillator provides a convenient clock source for the MAX165/MAX166. Typical conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination are shown in Figure 17. Due to process variations, the oscillation frequency for this R_{CLK} , C_{CLK} combination may vary by as much as $\pm 50\%$ from the nominal value shown in Figure 17. Therefore, an external clock should be used in the following situations:

1. Applications which require the conversion time to be within 50% of the minimum conversion time for the specified accuracy (5 μ s).
2. Applications in which time related software constraints cannot accommodate conversion time differences which may occur from unit to unit or over temperature for a given device.

CMOS μ P Compatible 5 μ s, 8-Bit A/D Converters

External Clock

The CLK input of the MAX165/MAX166 may be driven directly by a 74HC or 4000B series buffer (e.g., 4049) or an LS TTL with a 5.6k Ω pullup resistor. At the end of a

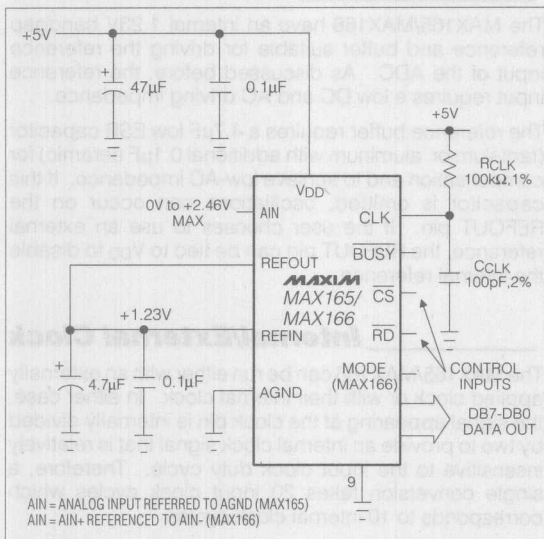


Figure 16A. MAX165/MAX166 Unipolar Configuration (Internal Reference)

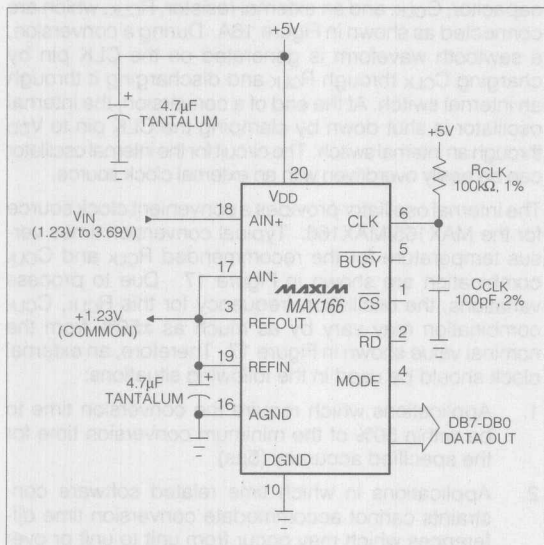


Figure 16B. MAX166 Unipolar Configuration

conversion, the device ignores the clock input and disables its internal clock signal. Therefore, the external clock may continue to run between conversions without being disabled. The duty cycle ratio of the external clock may vary from 70/30 to 30/70. As discussed previously, in order to maintain accuracy, clock rates significantly lower than the data sheet limits (4MHz) should not be used.

Typical Applications

Unipolar Operation

Figures 16A and 16B show the analog circuit connections and nominal transfer characteristics (Figure 16C) for unipolar operation. Since the offset and full-scale errors

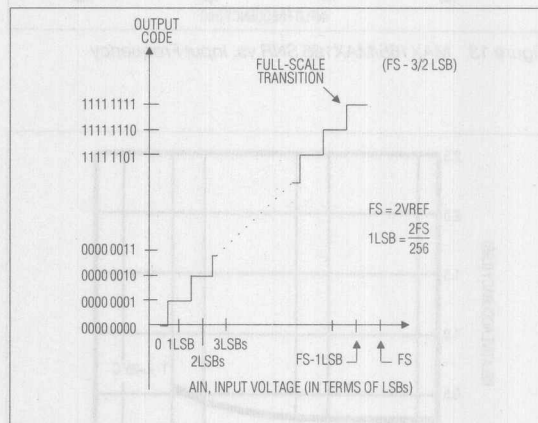


Figure 16C. Nominal Transfer Characteristic for Unipolar Operation

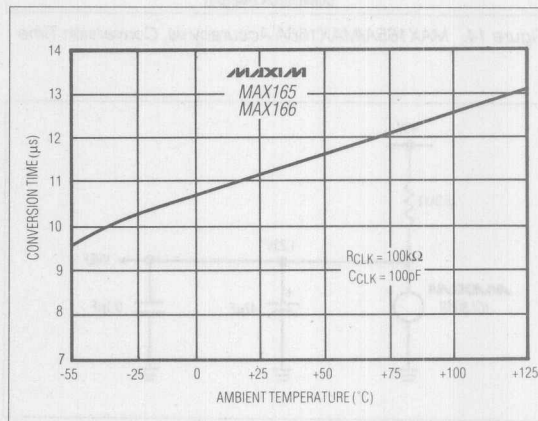


Figure 17. Typical Conversion Times vs. Temperature Using Internal Clock

CMOS μ P Compatible 5 μ s, 8-Bit A/D Converters

MAX165/MAX166

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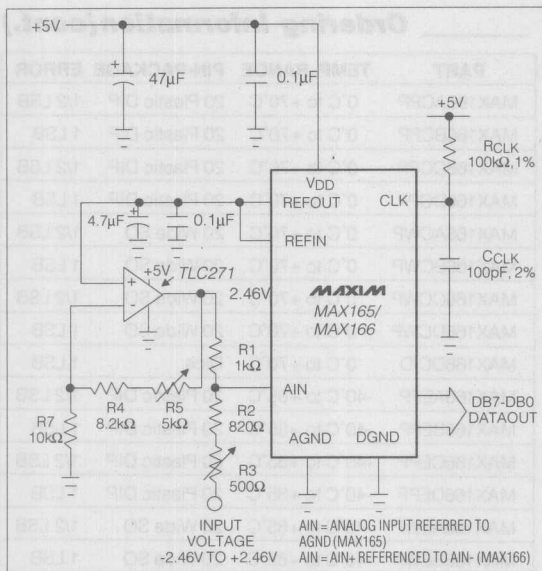


Figure 18A. MAX165/MAX166 Bipolar Configuration (Internal Reference)

of the MAX165/MAX166 are very small, it is not necessary to null these errors in most cases. If calibration is required, the following procedures can be followed.

Offset Adjust

The offset error can be easily adjusted by using the offset trim capability of an op amp when it is used as a voltage follower to drive the analog input AIN. The op amp that is used should have a common-mode input range that includes 0V. The op amp input is initially set to +4.8mV (+1/2LSB), while its offset is varied until the ADC output code flickers between 0000 0000 and 0000 0001.

Full-Scale Adjustment

The full-scale adjustment is made by forcing the analog input, AIN, to +2.445V (FS - 3/2LSB). The reference input voltage is then varied until the ADC output code flickers between 1111 1110 and 1111 1111.

Bipolar Operation

Figure 18A shows an example of the circuit connections for bipolar operation and its nominal transfer characteristics (Figure 18B). The output code provided by the MAX165/MAX166 is offset binary. The analog input range for this circuit is ± 2.46 V (1LSB = 19.22mV), even though the voltage appearing at the AIN pin is in the range of 0V to +2.46V. In most cases, the accuracy of the MAX165/MAX166 is high enough that calibration will not

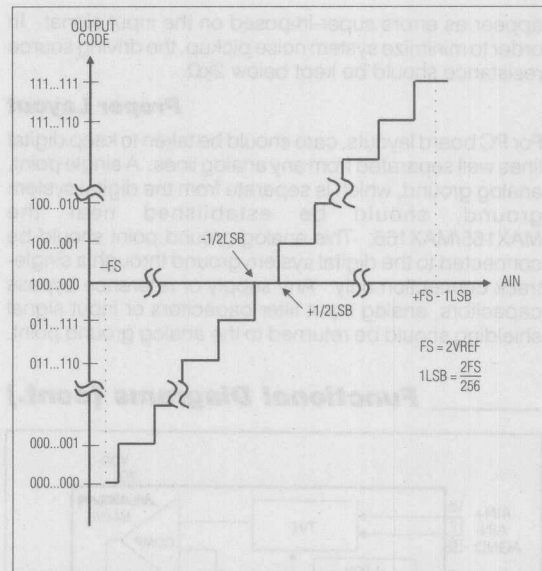


Figure 18B. Nominal Transfer Characteristic for Bipolar Operation

be necessary. If calibration is not needed, resistors R1 through R7 should have a 0.1% tolerance, with R4 and R5 replaced by one 10kΩ resistor, and R2 and R3 with one 1kΩ resistor. If calibration is required, then the procedure is as follows:

Offset Adjust

The offset error can be adjusted by applying an analog input voltage of +2.43V (FS - 3/2LSB). Resistor R5 is then adjusted until the output code flickers between 1111 1110 and 1111 1111.

Full-Scale Adjust

The full-scale errors are nulled by applying an analog input voltage of -2.45V (FS + 1/2LSB). Resistor R3 is then adjusted until the output code flickers between 0000 0000 and 0000 0001.

Application Hints

Noise

In order to minimize noise coupling, both the input signal lead to AIN and the signal return lead from AGND should be kept as short as possible. If this is not possible, a shielded cable or a twisted pair transmission line is recommended. Additionally, potential differences between the ADC ground and the signal source ground should be minimized since these voltage differences

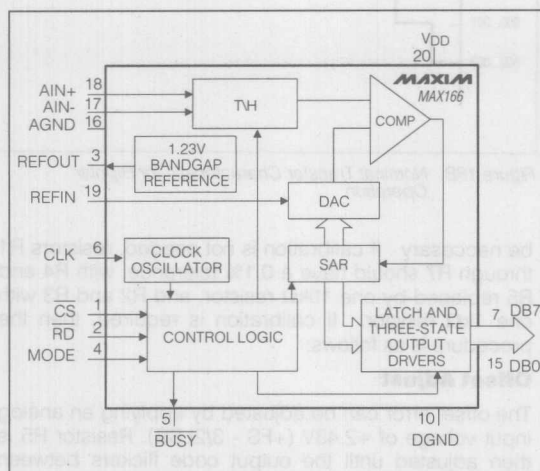
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appear as errors super-imposed on the input signal. In order to minimize system noise pickup, the driving source resistance should be kept below 2k Ω .

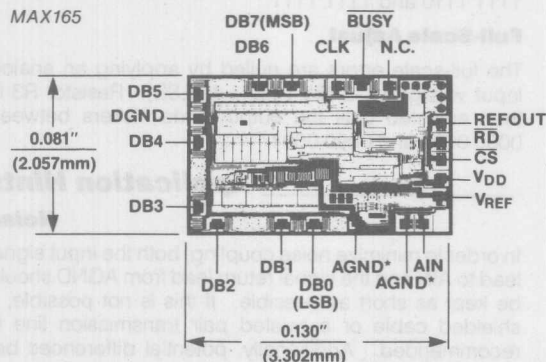
Proper Layout

For PC board layouts, care should be taken to keep digital lines well separated from any analog lines. A single point, analog ground, which is separate from the digital system ground, should be established near the MAX165/MAX166. This analog ground point should be connected to the digital system ground through a single-track connection only. Any supply or reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

Functional Diagrams (cont.)



MAX165



*The two AGND pads must both be used (bonded together).

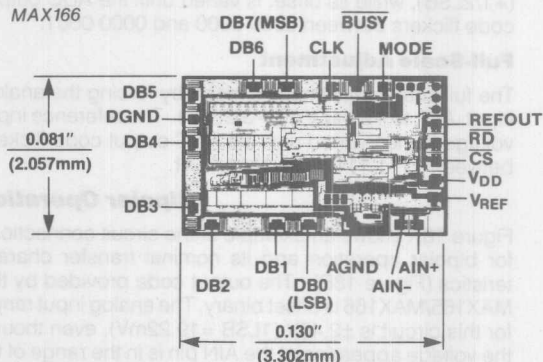
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Ordering Information(cont.)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR
MAX166ACPP	0°C to +70°C	20 Plastic DIP	1/2 LSB
MAX166BCPP	0°C to +70°C	20 Plastic DIP	1 LSB
MAX166CCPP	0°C to +70°C	20 Plastic DIP	1/2 LSB
MAX166DCPP	0°C to +70°C	20 Plastic DIP	1 LSB
MAX166ACWP	0°C to +70°C	20 Wide SO	1/2 LSB
MAX166BCWP	0°C to +70°C	20 Wide SO	1 LSB
MAX166CCWP	0°C to +70°C	20 Wide SO	1/2 LSB
MAX166DCWP	0°C to +70°C	20 Wide SO	1 LSB
MAX166DC/D	0°C to +70°C	Dice	1 LSB
MAX166AEPP	-40°C to +85°C	20 Plastic DIP	1/2 LSB
MAX166BEPP	-40°C to +85°C	20 Plastic DIP	1 LSB
MAX166CEPP	-40°C to +85°C	20 Plastic DIP	1/2 LSB
MAX166DEPP	-40°C to +85°C	20 Plastic DIP	1 LSB
MAX166AEWP	-40°C to +85°C	20 Wide SO	1/2 LSB
MAX166BEWP	-40°C to +85°C	20 Wide SO	1 LSB
MAX166CEWP	-40°C to +85°C	20 Wide SO	1/2 LSB
MAX166DEWP	-40°C to +85°C	20 Wide SO	1 LSB
MAX166AMJP	-55°C to +125°C	20 Cerdip	1/2 LSB
MAX166BMJP	-55°C to +125°C	20 Cerdip	1 LSB
MAX166CMJP	-55°C to +125°C	20 Cerdip	1/2 LSB
MAX166DMJP	-55°C to +125°C	20 Cerdip	1 LSB

Chip Topographies

MAX166



Serial Output 5.6 μ s 12-Bit A/D Converter

General Description

The MAX170 is a complete CMOS 12-bit A/D converter that combines high speed and accurate performance with a cost and space saving serial interface in an 8-lead DIP or 16-lead surface mount SO package. It uses a high speed DAC and an accurate comparator in a successive approximation loop to achieve a 5.6 μ s conversion time. An on-chip buried-zener reference provides low-drift performance over the full temperature range.

External components are limited only to supply and reference decoupling capacitors. The CLOCK input can be driven from an external clock source such as a divided-down microprocessor clock. The MAX170 works with +5V and -12V to -15V supply voltages, typically dissipating 135mW.

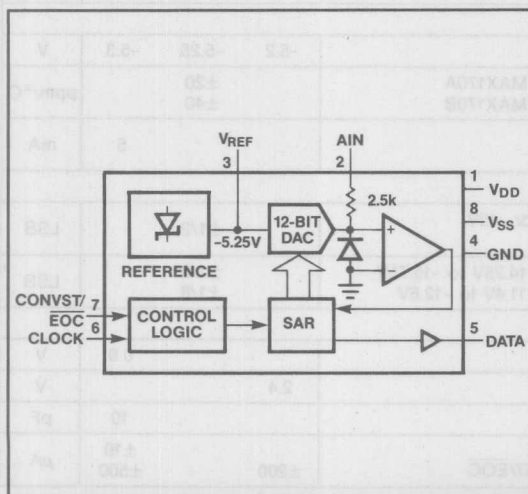
The MAX170 is designed to work with general purpose serial-to-parallel converters, such as the 74HC595. It can also be used with digital-signal-processors such as the TMS32020, TMS320C25, NEC μ PD7720 or the DSP56000. The MAX170 has a three-wire interface that serially outputs a leading one, followed by 12 data bits (MSB first).

When the MAX170 is used with an external sample-and-hold amplifier, a maximum sampling rate of 125kHz is possible.

Applications

Telecommunication
Digital Signal Processing (DSP)
Sonar/Radar Signal Processing
Isolated Industrial Data Acquisition

Functional Diagram



Features

- ◆ 12-Bit Resolution and Linearity
- ◆ 5.6 μ s Fast Conversion Time
- ◆ Serial Output
- ◆ Self-Start Mode
- ◆ Complete with On-Chip Reference
- ◆ Low Power (135mW)
- ◆ Easy to Opto- or Transformer-Isolate
- ◆ Small Footprint 8-Lead DIP, 16-Lead SO

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
MAX170ACPA	0°C to +70°C	Plastic DIP	$\pm 1/2$ LSB
MAX170BCPA	0°C to +70°C	Plastic DIP	± 1 LSB
MAX170ACWE	0°C to +70°C	Wide SO	$\pm 1/2$ LSB
MAX170BCWE	0°C to +70°C	Wide SO	± 1 LSB
MAX170BC/D	0°C to +70°C	Dice	± 1 LSB
MAX170AEPA	-40°C to +85°C	Plastic DIP	$\pm 1/2$ LSB
MAX170BEPA	-40°C to +85°C	Plastic DIP	± 1 LSB
MAX170AEWE	-40°C to +85°C	Wide SO	$\pm 1/2$ LSB
MAX170BEWE	-40°C to +85°C	Wide SO	± 1 LSB
MAX170AMJA	-55°C to +125°C	CERDIP	$\pm 1/2$ LSB
MAX170BMJA	-55°C to +125°C	CERDIP	± 1 LSB

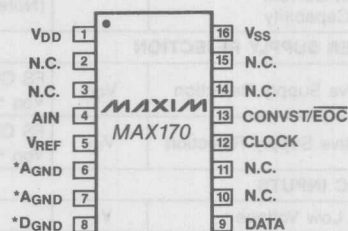
All DIP packages are 8 leads; all SO packages are 16 leads.

Pin Configurations

Top View



DIP



SO

*Leads 6, 7 and 8 must be connected together as close to the package as possible.

Serial Output 5.6 μ s 12-Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND -0.3 to +7V
V _{SS} to GND +0.3V to -17V
A _{IN} to AGND \pm 15V
Digital Input Voltage to GND -0.3V, V _{DD} +0.3V (Pins 6, 7, DIP)
Digital Output Voltage to GND -0.3V, V _{DD} +0.3V (Pin 5, DIP)

Operating Temperature Ranges

MAX170XC 0°C to +70°C
MAX170XE -40°C to +85°C
MAX170XM -55°C to +120°C
Storage Temperature Range -65°C to +160°C
Power Dissipation (any package) to +70°C 500mW
Derates Above +75°C by 6.25mW/°C
Lead Temperature (Soldering 10 seconds) +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V \pm 5%, V_{SS} = -11.4V to -15.75V; f_{CLK} = 2.5MHz; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
Integral Non-Linearity	INL	T _A = 25°C MAX170A MAX170AC/AE MAX170AM MAX170B			\pm 1/2 \pm 1/2 \pm 3/4 \pm 1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temperature			\pm 1	LSB
Offset Error (Note 1)		MAX170A MAX170B			\pm 3 \pm 5	LSB
Full Scale Error (Note 2)		T _A = 25°C			\pm 10	LSB
Full Scale Tempco (Notes 3, 4)		MAX170A MAX170B			\pm 25 \pm 45	ppm/°C
Conversion Time	t _{CONV}	14 Clock Cycles			5.6	μ s
ANALOG INPUT						
Input Voltage Range			0		+5	V
Input Current		A _{IN} = 0V to +5V			3.5	mA
INTERNAL REFERENCE						
V _{REF} Output Voltage		T _A = 25°C	-5.2	-5.25	-5.3	V
V _{REF} Output Tempco (Note 5)		MAX170A MAX170B		\pm 20 \pm 40		ppm/°C
Output Current Sink Capability		(Note 6)			5	mA
POWER SUPPLY REJECTION						
Positive Supply Rejection	V _{DD}	FS Change, V _{SS} = -15V or -12V, V _{DD} = 4.75V to 5.25V		\pm 1/2		LSB
Negative Supply Rejection	V _{SS}	FS Change, V _{DD} = +5V V _{SS} = -14.25V to -15.75V V _{SS} = -11.4V to -12.6V		\pm 1/8 \pm 1/8		LSB
LOGIC INPUTS						
Input Low Voltage	V _{IL}				0.8	V
Input High Voltage	V _{IH}		2.4			V
Input Capacitance (Note 7)	C _{IN}				10	pF
Input Current	I _{IN}	A _{IN} = 0 to V _{DD} CLOCK CONVST/EOC	\pm 200		\pm 10 \pm 500	μ A

Serial Output 5.6μs 12-Bit A/D Converter

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V; f_{CLK} = 2.5MHz; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUT						
Output Low Voltage	V _{OL}	DATA I _{SINK} = 1.6mA			0.4	V
		DATA I _{SINK} = 6.0mA		0.3	1.5	
Output High Voltage	V _{OH}	DATA I _{SOURCE} = 200μA	4			V
POWER REQUIREMENTS						
Positive Supply Voltage	V _{DD}	±5% for Specified Performance		5		V
Negative Supply Voltage (Note 8)	V _{SS}	±5% for Specified Performance	-15 to -12			V
Positive Supply Current	I _{DD}	CONVST/EOC = V _{DD} , AIN = 0V		5	8	mA
Negative Supply Current	I _{SS}	CONVST/EOC = V _{DD} , AIN = 0V		-6	-11	mA
Power Dissipation		V _{DD} = +5V, V _{SS} = -15V		115	205	mW
TIMING CHARACTERISTICS (Note 9)						
(V _{DD} = +5V, V _{SS} = -12V or -15V; T _A = T _{MIN} to T _{MAX})						
CLOCK Pulse Width	t _{CH}	CLOCK HIGH	40			ns
	t _{CL}	CLOCK LOW	60			
CONVST/EOC Pulse Width	t _{SH}	CONVST/EOC HIGH	40			ns
	t _{SL}	CONVST/EOC LOW	60			
CONVST/EOC to CLOCK Skew	t _{SC0} t _{SC1}	Leading CLOCK Leading CLOCK + 1	200		40	ns
CLOCK to DATA Delay	t _{PD}		25		80	ns

Note 1: Typical change over temp is ±1 LSB.

Note 2: FS = +5,000V. Ideal last code transition = FS - 3/2 LSB. Adjusted for offset error.

Note 3: Full Scale Tempco = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.

Note 4: Includes internal reference drift.

Note 5: V_{REF} Tempco = ΔV_{REF}/ΔT, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.

Note 6: Output current should not change during conversion.

Note 7: Guaranteed by design, not subject to test.

Note 8: Specified performance with -12V supply is guaranteed by testing offset and full scale errors.

Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Converter Operation

The MAX170 uses a successive approximation technique to convert an unknown analog input to a 12-bit digital output code. The digital interface requires only three digital lines. Most applications require only a few external passive components to perform the analog-to-digital function. Figure 1 shows the MAX170 in its simplest operational configuration.

Figure 2 shows the MAX170 analog equivalent circuit. The internal voltage output digital-to-analog converter (DAC) is controlled by a successive approximation register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 2.5kΩ resistor. The comparator is essentially a zero-crossing detector with its output feeding back to the SAR input.

Timing and Control

The MAX170 can be used in two different modes: Forced-Start Mode requires an external conversion start

signal to initiate the conversions. Self-Start Mode uses an internally generated conversion start signal and causes the MAX170 to convert continuously.

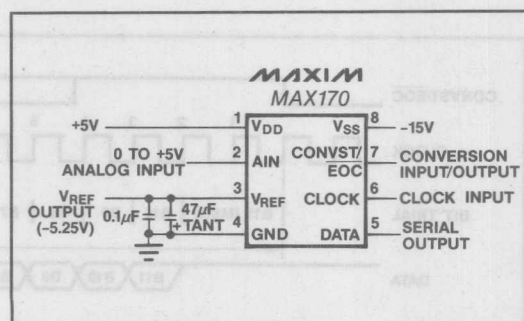


Figure 1. MAX170 Operational Diagram

Serial Output 5.6 μ s 12-Bit A/D Converter

Pin Description

PIN DIP	SO	NAME	FUNCTION
1	1	V _{DD}	Positive Supply, +5V
2	4	AIN	Analog Input, 0V to +5V Unipolar
3	5	V _{REF}	Reference Voltage Output, -5.25V
	6,7	AGND	Analog Ground. Must be tied to the GND pin.
4	8	GND	Ground
5	9	DATA	Serial Data Output
6	12	CLOCK	Clock Input, TTL/+5V CMOS compatible.
7	13	CONVST/EOC	Conversion Start Input for three-wire mode; End-of-Conversion output for two-wire mode.
8	16	V _{SS}	Negative Supply, -12V or -15V

Forced-Start Mode

A conversion cycle is initiated on the rising edge of the conversion start signal (CONVST/EOC) that is coincident with a falling edge of the CLOCK signal. Figure 3 shows a single conversion cycle with a continuous CLOCK. Once started, a conversion cannot be stopped and transitions at the CONVST/EOC input have no effect until the current conversion is completed (minimum of 14 clock cycles from the last rising edge of the conversion start signal).

The conversion start transition causes the SAR to set B11 (MSB) which drives the DAC output to half-scale. The analog input is compared to this value from the time of the conversion start transition until the second falling edge of CLOCK which latches the MSB result and sets the SAR to compare the next bit. The MSB result appears at the DATA output after a delay T_{PD} from the falling edge of CLOCK. Each subsequent bit conversion proceeds similarly until all 12 bits of the DAC have been tried. Conversion is completed at the falling edge of the 13th CLOCK cycle. The DATA output returns high at the falling edge of the 14th CLOCK cycle and remains so until the next conversion sends out its MSB result.

The next conversions can be started on the 14th CLOCK cycle of a previous conversion as shown in Figure 4. This results in the maximum throughput rate of one conversion per 14 CLOCK cycles.

Conversion start transitions must arrive within the setup limits t_{SC0} and t_{SC1} relative to the falling edges of the CLOCK signal to guarantee that the serial DATA output stream will start at the second CLOCK cycle, as shown in Figure 4. Limits t_{SC0} and t_{SC1} apply whether conversion is started directly after a previous cycle on the 14th CLOCK, or if idle CLOCK pulses exist between conversions. Note that bringing CONVST/EOC input high on the falling edge of CLOCK 14 allows the maximum time for the internal DAC to settle.

It is possible to operate the MAX170 at a higher or lower clock rate than specified. At higher than 2.5MHz clock rates, the INL will degrade as shown in Figure 5. But at lower speeds, there will be no degradation of the INL.

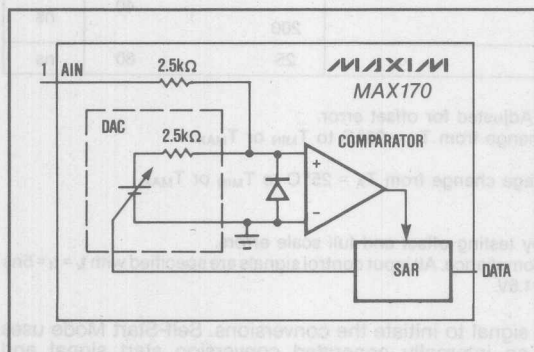


Figure 2. MAX170 Analog Equivalent Circuit

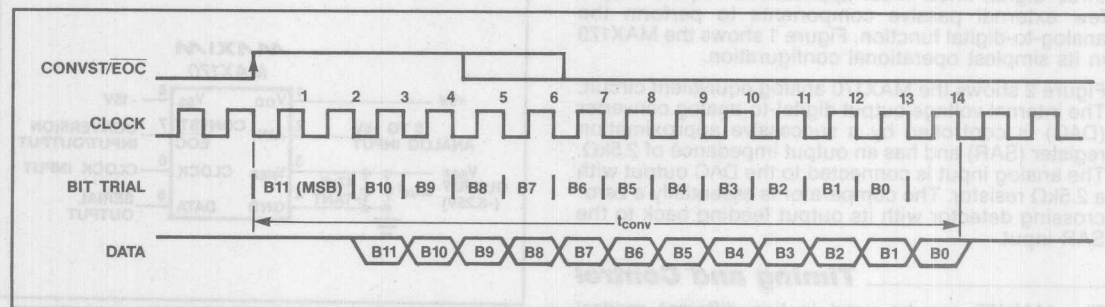


Figure 3. Forced-Start Mode Timing (14 Clocks Per Conversion Cycle)

Serial Output 5.6 μ s 12-Bit A/D Converter

MAX170

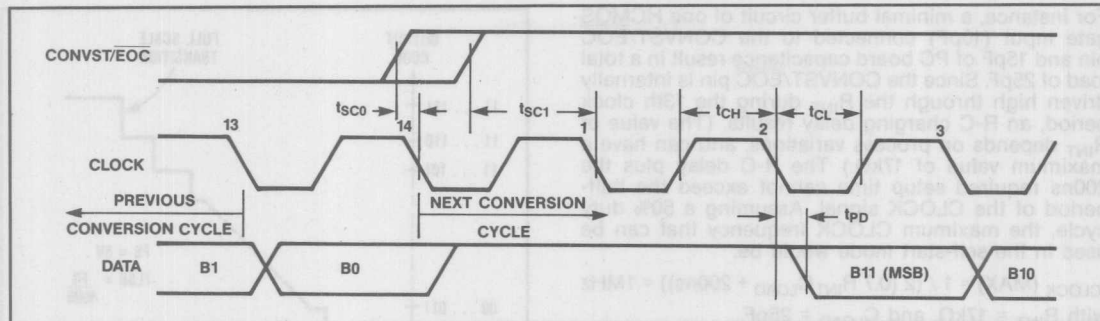


Figure 4. MAX170 Timing Diagram

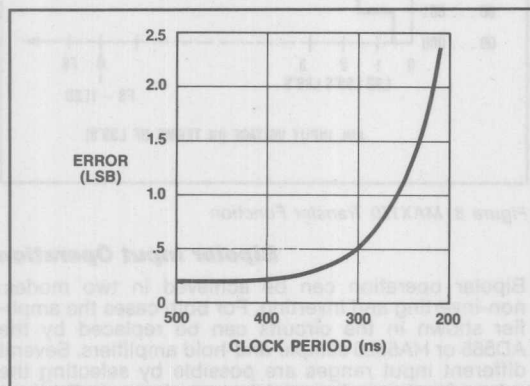


Figure 5. Typical INL vs Clock Rate for MAX170

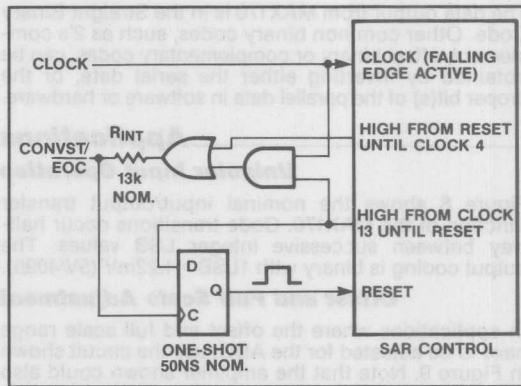


Figure 6. MAX170 Logic Equivalent for Start and Clock Inputs

Self-Start Mode

The CONVST/EOC pin is internally driven by a conversion complete signal through a 13k Ω (typical value) resistor, R_{INT} (Figure 6). By leaving this pin open-circuited, the MAX170 will generate its own conversion start input and run at a rate of one conversion for every 13 CLOCK cycles. The signal at the CONVST/EOC pin can be buffered and used as a framing signal to synchronize the serial data (Figure 7).

The CLOCK rate in the self-start mode will be limited by capacitive loading of the CONVST/EOC pin. Therefore, no more than one HCMOS logic input and a minimum of PC board capacitance should be connected to this pin when high speed conversions are desired. The maximum CLOCK rate for this mode will be limited by the requirement that the conversion start signal must cross the logic high threshold ($V_{IH} = 2.4V$) of this input at least 200ns before the falling edge of the first clock cycle (t_{SC1}).

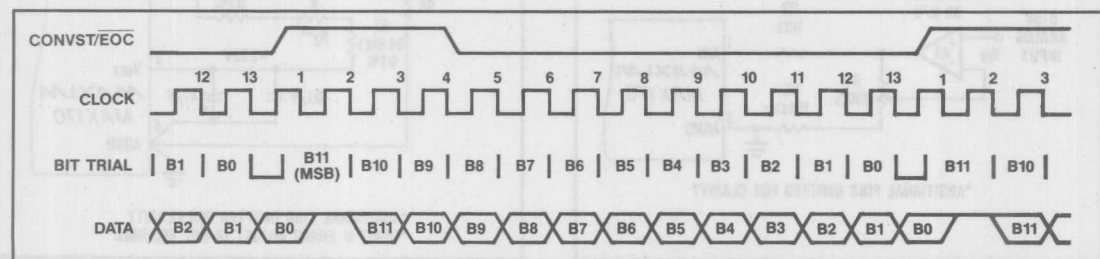


Figure 7. Self-Start Mode Timing (13 Clocks Per Conversion Cycle)

Serial Output 5.6 μ s 12-Bit A/D Converter

For instance, a minimal buffer circuit of one HCMOS gate input (10pF) connected to the CONVST/EOC pin and 15pF of PC board capacitance result in a total load of 25pF. Since the CONVST/EOC pin is internally driven high through the R_{INT} during the 13th clock period, an R-C charging delay results. (The value of R_{INT} depends on process variations, and can have a maximum value of 17k Ω .) The R-C delay plus the 200ns required setup time cannot exceed the half-period of the CLOCK signal. Assuming a 50% duty cycle, the maximum CLOCK frequency that can be used in the self-start mode would be:

$$f_{CLOCK} (MAX) = 1 / (2 (0.7 R_{INT} C_{LOAD} + 200ns)) = 1MHz$$

with $R_{INT} = 17k\Omega$, and $C_{LOAD} = 25pF$.

Output Coding

The data output from MAX170 is in the Straight Binary Code. Other common binary codes, such as 2's complement, offset binary or complementary codes, can be obtained by inverting either the serial data, or the proper bit(s) of the parallel data in software or hardware.

Applications

Unipolar Input Operation

Figure 8 shows the nominal input/output transfer function of the MAX170. Code transitions occur halfway between successive integer LSB values. The output coding is binary with 1LSB = 1.22mV (5V/4096).

Offset and Full Scale Adjustment

In applications where the offset and full scale range have to be adjusted for the ADC, use the circuit shown in Figure 9. Note that the amplifier shown could also have been a sample-and-hold. The offset should be adjusted first. Apply 1/2 LSB (0.61mV) at the analog input and adjust the offset of the amplifier until the digital output code changes between 0000 0000 0000 and 0000 0000 0001.

To adjust the full scale range, apply FS - 3/2LSB (4.9817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

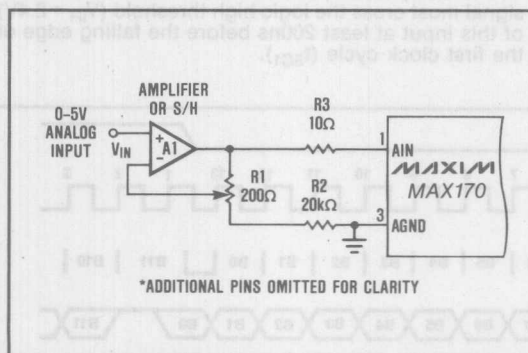


Figure 9. Full-Scale Adjustment

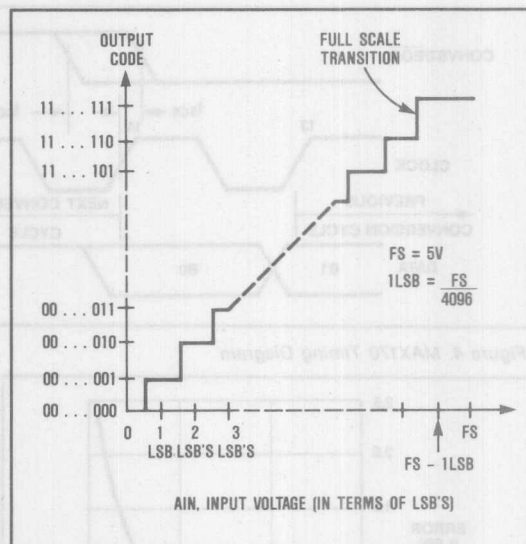


Figure 8. MAX170 Transfer Function

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 1 and 2.

Figure 10 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 11 shows the ideal transfer function for this mode.

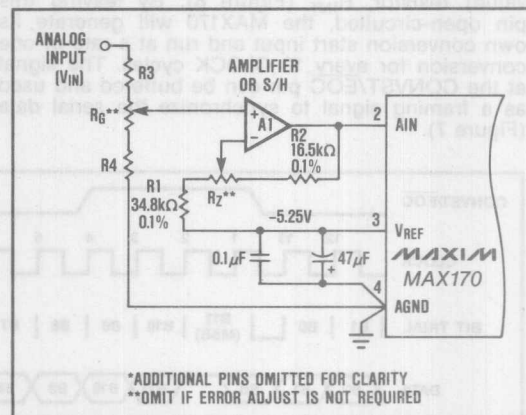


Figure 10. MAX170 Non-Inverting Bipolar Operation

Serial Output 5.6 μ s 12-Bit A/D Converter

Table 1. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 10

V _{IN} Range (Volts)	R3* (k Ω)	R4* (k Ω)	R _Z (Ω)	R _G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
± 2.5	3.83	8.25	500	500	0.61	2.49817
± 5.0	33.2	16.9	500	1000	1.22	4.99634
± 10.0	47.5	9.53	500	500	2.44	9.99268

*R3 and R4 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

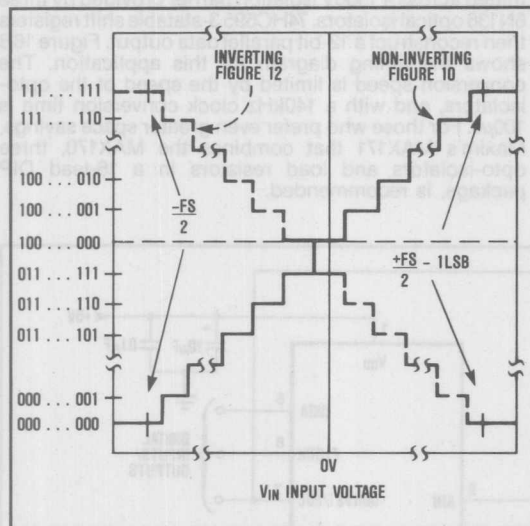


Figure 11. Ideal Input/Output Transfer Characteristics for the Bipolar Circuits Shown in Figures 10 and 12

Figure 12 shows the bipolar operation in the inverting mode where the output coding is complementary offset binary. Figure 11 shows the ideal transfer function for the circuit in Figure 12.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drift. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply $+1/2$ LSB to the analog input (see Tables 1 and 2) and adjust R_Z until the output code flickers between the following codes:

For Non-Inverting (Figure 10) 1000 0000 0000
1000 0000 0001

For inverting (Figure 12) 0111 1111 1111
0111 1111 1110

Apply FS - $3/2$ LSB (See Tables 1 and 2) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-inverting (Figure 10) 1111 1111 1110
1111 1111 1111

For inverting (Figure 12) 0000 0000 0001
0000 0000 0000

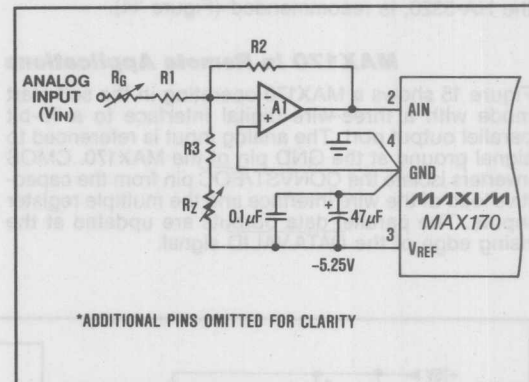


Figure 12. MAX170 Inverting Bipolar Operation

Table 2. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 12

V _{IN} Range (Volts)	R1* (k Ω)	R2* (k Ω)	R3* (k Ω)	R _Z (Ω)	R _G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
± 2.5	20	20.5	42.2	2000	1000	0.61	2.49817
± 5.0	20	10.2	21	1000	1000	1.22	4.99634
± 10.0	20	5.11	10.5	500	1000	2.44	9.99268

*R1, R2 and R3 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

MAX170 to Sample-and-Hold Interface

The analog input to the MAX170 must be stable to within $\pm 1/2$ LSB during the entire conversion for specified 12-bit accuracy. This limits the input signal bandwidth to a few Hz for sinusoidal inputs. For higher bandwidth signals, a sample-and-hold should be used.

The signal that starts the MAX170 conversions can be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. The MAX170's DAC is switched at approximately the same time as the sample-and-hold amplifier starts holding the signal. The sample-and-hold amplifier should switch to the HOLD mode before there are any disturbances on the input signal, otherwise code dependent errors will be observed. These can be avoided by starting the MAX170 slightly after the TRACK/HOLD signal by using a gate delay. For synchronous conversion start and CLOCK as described above, the maximum allowable hold settling time for the sample-and-hold is 600ns.

MAX170

The maximum sampling rate is 125kHz with a 2.5MHz clock and 64.5kHz with a 1MHz clock allowing for a 3 μ s sample-and-hold acquisition time. At the 2.5MHz clock rate a faster sample-and-hold amplifier, such as the HA-5320, is recommended (Figure 14).

Figure 15 shows a MAX170 operating in the self-start mode with a three-wire digital interface to a 12-bit parallel output port. The analog input is referenced to signal ground at the GND pin of the MAX170. CMOS inverters isolate the CONVST/EOC pin from the capacitive load of the wire interface and the multiple register inputs. The parallel data outputs are updated at the rising edge of the DATA VALID signal.

Serial interface simplifies opto-coupled or transformer-coupled A/D converter applications. For example, transducer outputs often require electrical isolation to separate the control electronics from hazardous electrical conditions, provide noise immunity or bridge large differences in ground potential. Isolation amplifiers that are typically used for accomplishing this cost up to \$100 per channel. The MAX170 provides a low cost alternative to isolation amplifiers, and it performs the A/D conversion as well (Figure 16A). The A/D converter results are transmitted across a 1500V isolation barrier provided by three 6N136 optical isolators. 74HC595 3-statable shift registers then reconstruct a 12-bit parallel data output. Figure 16B shows the timing diagram for this application. The conversion speed is limited by the speed of the opto-isolators, and with a 140kHz clock conversion time is 100 μ s. For those who prefer even greater space savings, Maxim's MAX171 that combines the MAX170, three opto-isolators and load resistors in a 16-lead DIP package, is recommended.



Serial Output 5.6 μ s 12-Bit A/D Converter

MAX170

1

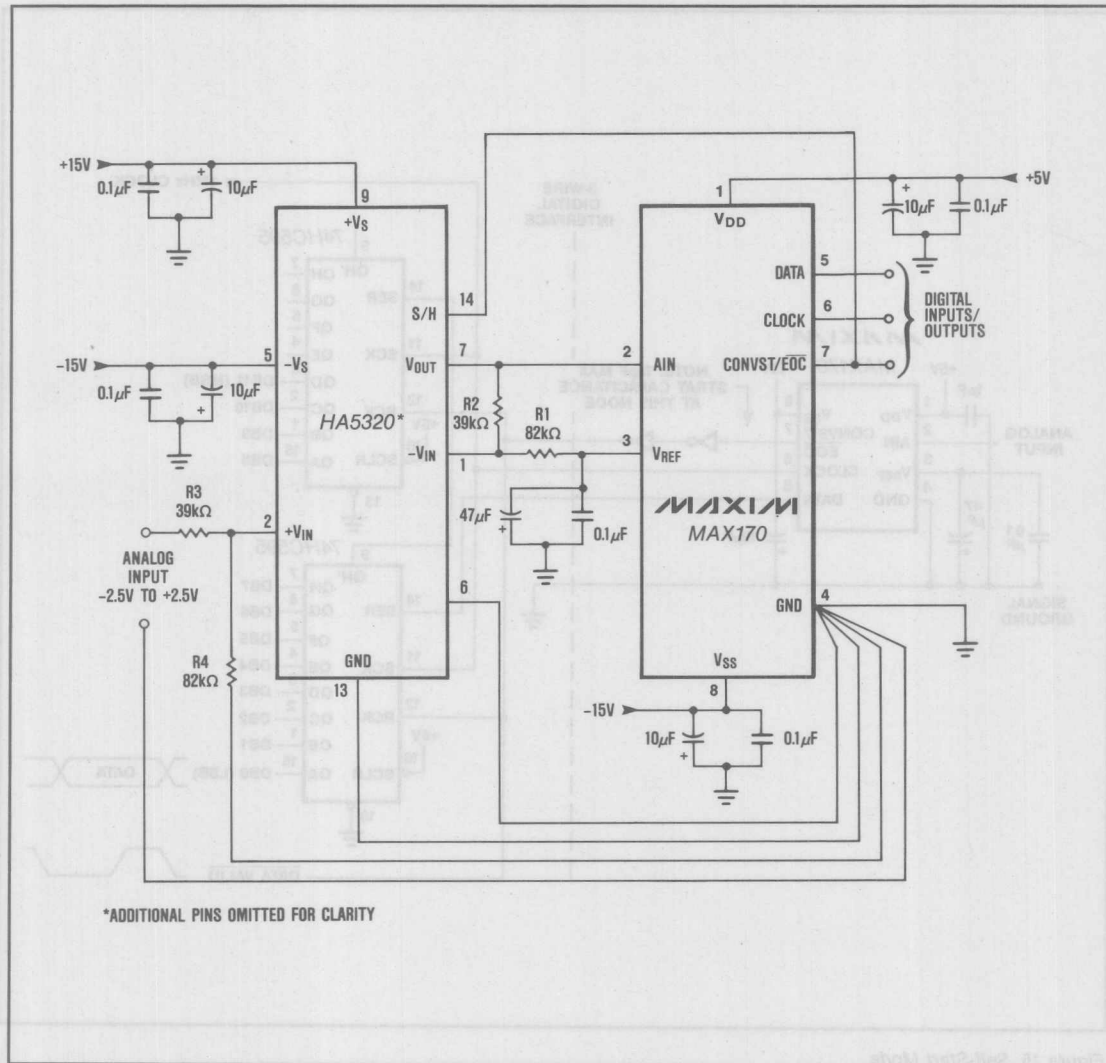


Figure 14. MAX170-HA5320 Sample-and-Hold Interface

Figure 17 shows the recommended system ground connections. A single-pointing STAR ground should be established at pin 4 (GND) of the MAX170. All grounds should be connected to this STAR ground. The ground return to the power supply from this STAR ground should be low impedance for noise-free operation of the MAX170.

Application Hints

Physical Layout

For best system performance printed circuit boards should be used for the MAX170. Where wire boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX170 package.

Serial Output 5.6 μ s 12-Bit A/D Converter

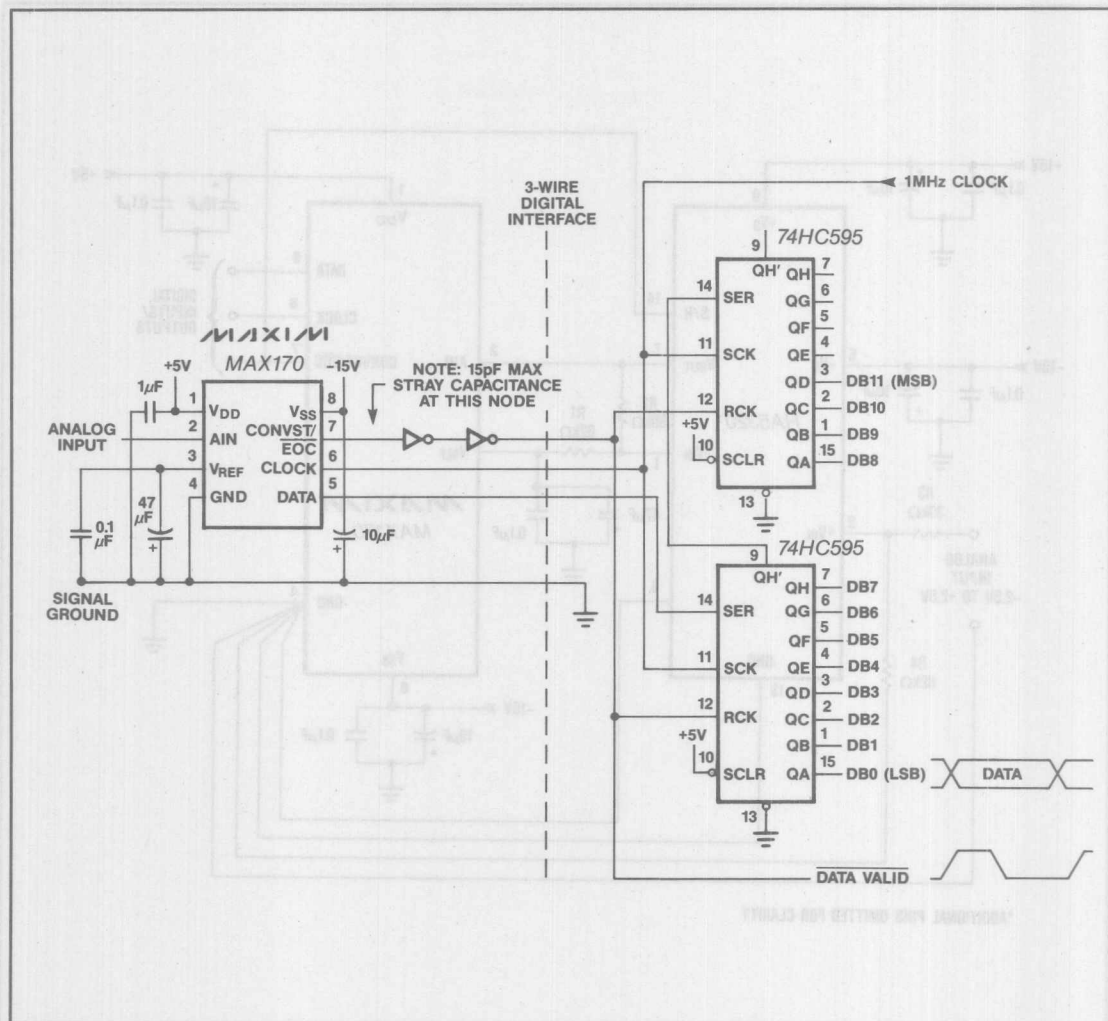


Figure 15. Self-Start Mode

Application Hints

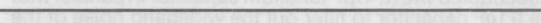
Physical Layout

For best system performance printed circuit boards should be used for the MAX170. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX170 package.

Grounding

Figure 17 shows the recommended system ground connections. A single point analog STAR ground should be established at pin 4 (GND) of the MAX170. All grounds should be connected to this STAR ground. The ground return to the power supply from this STAR ground should be low impedance for noise-free operation of the MAX170.

MAX170



Serial Output 5.6 μ s 12-Bit A/D Converter

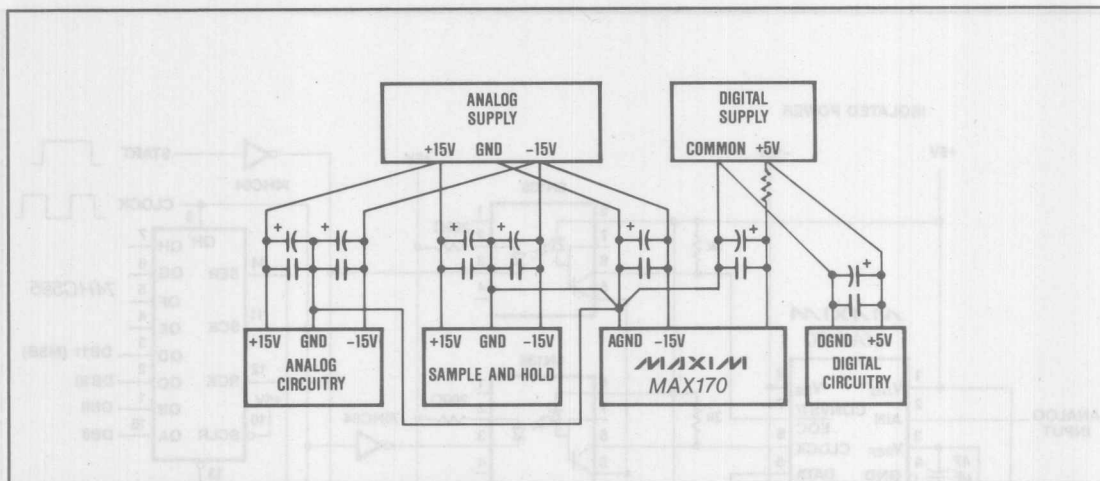


Figure 17. Power Supply Grounding

Power Supply Bypassing

The high speed comparator in the MAX170 is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be by-passed to the analog STAR ground with 0.1 μ F and 10 μ F by-pass capacitors with minimum lead length for supply noise rejection. If the +5V power supply is very noisy, a small resistor (10–20 Ω) can be connected as shown in Figure 17 to filter external noise.

Internal Reference

The MAX170 has an on-chip reference that is built with a buffered and temperature compensated buried zener diode, laser-trimmed to $-5.25V \pm 1\%$. Its output is connected to the V_{REF} pin and also drives the internal DAC. This output can be used as a reference voltage source for other components.

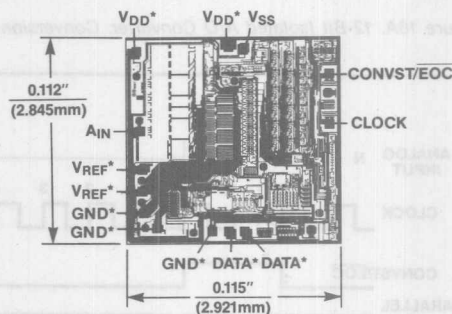
For minimal transition noise, the V_{REF} pin must be decoupled with a 47 μ F tantalum capacitor in parallel with a 0.1 μ F capacitor to filter out the wideband noise of the zener diode and to provide low impedance at high frequencies (Figure 1). This capacitor also creates the dominant pole of the reference buffer amplifier for stability. If this capacitor is not used, the reference will oscillate. Since the MAX170 buffer amplifier is designed to be stable with this capacitor, no series resistance should be used between the V_{REF} pin and the capacitor. This capacitor must not be less than 4.7 μ F.

Driving the Analog Input

The input signal leads to AIN and GND should be as short as possible to minimize noise pick-up. If the leads must be long, use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5k Ω . The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion. The output impedance of the driving amplifier is reduced by the loop gain at the frequency of interest. With a maximum clock rate of 2.5MHz, it is possible to drive the MAX170 with amplifiers like the OP-42, AD711, or OP-27. At 1MHz clock rate a MAX400 or OP-07 can also be used.

Chip Topography



* Pads with the same name must be bonded together.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

General Description

The MAX171 is a complete 5.8 μ s, 12-bit analog-to-digital converter (ADC) that provides over 1,500V_{RMS} electrical isolation between its analog input and the digital interface pins. It combines a serial output 12-bit ADC, three opto-couplers, and a low-drift buried-zener voltage reference in a standard 16-lead plastic DIP package (0.3").

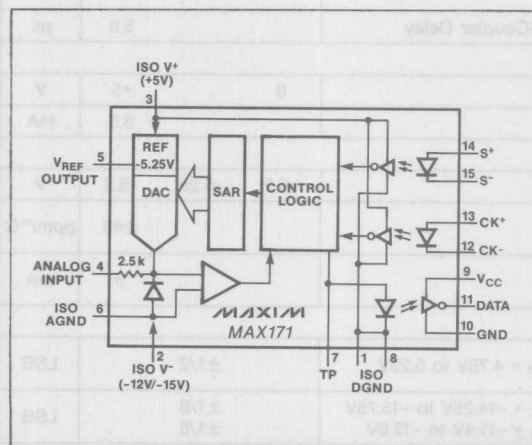
Required external components are limited to supply and reference decoupling capacitors and three resistors. The 2.5MHz clock input can be driven from an external clock source such as a divided microprocessor clock. The MAX171 works with +5V and -12V to -15V supply voltages and typically dissipates 265mW.

The MAX171 is useful in applications where an analog signal must be electrically isolated from control electronics to avoid hazardous electrical conditions, provide noise immunity, or bridge large differences in ground potential. These situations have traditionally required an instrumentation or isolation amplifier with suitably high common mode rejection. If the analog signal must be digitized at some point in the signal chain, the MAX171 can replace these isolating amplifiers while providing high performance and lower cost.

Applications

Ground-Loop Interruption
Process Control
Isolated Industrial Data Acquisition
Electro-Mechanical Systems
Robotics
Automatic Test Equipment

Functional Diagram



Features

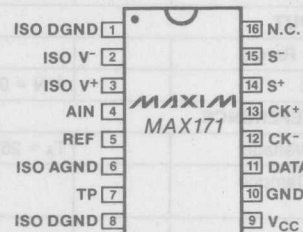
- ◆ Optical Isolation to Over 1,500V_{RMS}
- ◆ UL Recognized in File E118032 to UL1577
- ◆ 12-Bit Resolution and Linearity
- ◆ 5.8 μ s Conversion Time
- ◆ No Missing Codes Over Temperature
- ◆ Serial Output
- ◆ Complete with On-Chip Reference
- ◆ Standard 16-Lead Plastic DIP Package

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
MAX171ACPE	0°C to +70°C	Plastic DIP	$\pm 1/2$ LSB
MAX171BCPE	0°C to +70°C	Plastic DIP	± 1 LSB
MAX171AEPE	-40°C to +85°C	Plastic DIP	$\pm 1/2$ LSB
MAX171BEPE	-40°C to +85°C	Plastic DIP	± 1 LSB

Pin Configuration

TOP VIEW



Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS

$V_{ISO} V^+$ to ISO GND	-0.3V to +7V
$V_{ISO} V^-$ to ISO GND	+0.3V to -17V
AIN to ISO GND	$\pm 15V$
V_{CC} to GND	-0.3V to +7V
DATA Output Current	60mA
DATA Output Voltage	5.5V
Digital Inputs: S^+ to S^- and CK^+ to CK^- :	
LED Current	15mA
LED Reverse Voltage	5V

Isolation Voltage	
1 second	1,500 V_{RMS}
1 minute	1,200 V_{RMS}
Continuous	130 V_{RMS}
Operating Temperature Ranges	
MAX171XC	0°C to +70°C
MAX171XE	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Power Dissipation to +75°C	1000mW
Derates Above +75°C by	10mW/°C
Lead Temperature (Soldering 10 sec)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V \pm 5\%$, $V_{ISO} V^+ = +5V \pm 5\%$, $V_{ISO} V^- = -11.4V$ to $-15.75V$; $f_{CLK} = 2.5MHz$; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION ($T_A = +25^\circ C$, Note 1)						
Test Voltage	V_{ISO}	1 second withstand 1 minute withstand (Note 2)	1500 1200			V_{RMS} V_{RMS}
Leakage Current	I_{ISO}	$V_{ISO} = 130V_{RMS}$, 60Hz		2	50	μA_{RMS}
Resistance	R_{ISO}	$V_{ISO} = 500VDC$		10^{10}		Ω
Capacitance	C_{ISO}			5		pF
ACCURACY						
Resolution			12			Bits
Integral Non-Linearity	INL	MAX171AC MAX171AE MAX171B			$\pm 1/2$ $\pm 3/4$ ± 1	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Specified Temperature Range			± 1	LSB
Offset Error (Note 3)		MAX171A MAX171B			± 3 ± 5	LSB
Full Scale Error (Note 4)		$T_A = 25^\circ C$			± 10	LSB
Full Scale Tempco (Notes 5, 6)					± 45	ppm/°C
Conversion Time	t_{CONV}	14 Clock Cycles + Opto-Coupler Delay			5.8	μs
ANALOG INPUT						
Input Voltage Range			0		+5	V
Input Current		AIN = 0V to +5V			3.5	mA
INTERNAL REFERENCE						
V_{REF} Output Voltage		$T_A = 25^\circ C$	-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 7)					± 40	ppm/°C
Output Current Sink Capability		(Note 8)			5	mA
POWER SUPPLY REJECTION						
Positive Supply Rejection	V_{DD}	FS Change, $V_{SS} = -15V$ or $-12V$	$V_{DD} = 4.75V$ to $5.25V$	$\pm 1/2$		LSB
Negative Supply Rejection	V_{SS}	FS Change, $V_{DD} = +5V$	$V_{SS} = -14.25V$ to $-15.75V$ $V_{SS} = -11.4V$ to $-12.6V$	$\pm 1/8$ $\pm 1/8$		LSB

Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

MAX171

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +5V \pm 5\%$, $V_{ISO} V^+ = +5V \pm 5\%$, $V_{ISO} V^- = -11.4V$ to $-15.75V$; $f_{CLK} = 2.5MHz$; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (S^+ to S^- and CK^+ to CK^-)						
LED Operating Current	I_{IJN}		8	10	15	mA
LED Forward Operating Voltage	V_{IJN}	$I_{IJN} = 10mA$		1.55	1.75	V
LED Capacitance (Note 9)	C_{IJN}			60		pF
LOGIC OUTPUT (DATA)						
Output Low Voltage	V_{OL} V_{OL}	$I_{SINK} = 1.6mA$ $I_{SINK} = 13mA$	0.25		0.4 0.6	V
Output High Current	I_{OH}	$V_{DATA} = 5.5V$		0.02	250	μA
POWER REQUIREMENTS						
Analog Positive Supply Voltage	$V_{ISO} V^+$	$\pm 5\%$ for Specified Performance	4.75		5.25	V
Analog Negative Supply Voltage (Note 10)	$V_{ISO} V^-$	$\pm 5\%$ for Specified Performance	-15.75		-11.4	V
Analog Positive Supply Current	$I_{ISO} V^+$	START = V_{DD} , AIN = 0V		25	44	mA
Analog Negative Supply Current	$I_{ISO} V^-$	START = V_{DD} , AIN = 0V		-6	-12	mA
Digital Positive Supply Voltage	V_{CC}		4.75		5.25	V
Digital Positive Supply Current	I_{CC}			10	18	mA
Power Dissipation		$V_{ISO} V^+ = +5V$, $V_{ISO} V^- = -15V$, $V_{CC} = +5V$		265	495	mW
TIMING CHARACTERISTICS (Note 11)						
CLOCK Pulse Width	t_{CH} t_{CL}	CLOCK HIGH CLOCK LOW	60 80			ns
START Pulse Width	t_{SH} t_{SL}	START HIGH START LOW	60 80			ns
START to CLOCK Skew	t_{SC0} t_{SC1}	Leading CLOCK Leading CLOCK + 1	250		100	ns
CLOCK to DATA Delay	t_{PD}	$T_A = 25^\circ C$		175	250	ns

Note 1: Isolation voltage is measured between pins 1 to 8 connected together and pins 9 to 16 connected together.

Note 2: Guaranteed by the "2 second withstand test voltage," which is 100% production tested.

Note 3: Typical change over temp is ± 1 LSB.

Note 4: $V_{ISO} V^+ = +5V$, $V_{ISO} V^- = -15V$, FS = +5.000V or +2.500V. Ideal last code transition = FS - 3/2LSB

Note 5: Full Scale Tempco = $\Delta FS / \Delta T$, where ΔFS is full scale change from $T_A = 25^\circ C$ to T_{MIN} or T_{MAX} .

Note 6: Includes internal reference drift.

Note 7: V_{REF} Tempco = $\Delta V_{REF} / \Delta T$, where ΔV_{REF} is reference voltage change from $T_A = 25^\circ C$ to T_{MIN} or T_{MAX} .

Note 8: Output current should not change during conversion.

Note 9: Guaranteed by design, not subject to test.

Note 10: Specified performance with -12V supply is guaranteed by testing offset and full scale errors.

Note 11: Timing specifications are sample tested to LTPD = 10 at $25^\circ C$ to ensure compliance. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

Pin Description

PIN DIP	NAME	FUNCTION
1	ISO DGND	Isolated Digital Ground
2	ISO V ⁻	Analog Negative Supply, -12V or -15V
3	ISO V ⁺	Analog Positive Supply, +5V
4	AIN	Analog Input, 0V to +5V Unipolar
5	REF	Reference Voltage Output, -5.25V
6	ISO AGND	Isolated Analog Ground. Normally tied to ISO DGND
7	TP	Test Pin. Leave unconnected
8	ISO DGND	Isolated Digital Ground
ELECTRICAL ISOLATION BARRIER		
9	V _{CC}	Digital Positive Supply, +5V
10	GND	Digital Ground
11	DATA	Serial Data Output
12	CK ⁻	Clock ⁻ Input
13	CK ⁺	Clock ⁺ Input
14	S ⁺	Conversion Start ⁺ Input
15	S ⁻	Conversion Start ⁻ Input
16	N.C.	No Connect

Converter Operation A/D Converter

The MAX171 combines a successive approximation A/D converter and three opto-couplers to convert an unknown analog input to an electrically isolated 12-bit serial output code. The opto-coupled digital interface works with three interface signals: Conversion Start Input (S⁺, S⁻), Clock Input (CK⁺, CK⁻), and the Serial Data Output (DATA). Most applications require only a few external passive components to perform the analog-to-digital function. Figure 1 shows the MAX171 in its simplest operational configuration.

Figure 2 shows the MAX171 analog equivalent circuit. The internal digital-to-analog converter (DAC) is controlled by a successive approximation register (SAR) and has an output impedance of 2.5k Ω . The analog input is connected to the DAC output with a 2.5k Ω resistor. The comparator is essentially a zero-crossing detector with its output feeding back to the SAR input.

Opto-Couplers

The Start (S⁺, S⁻) and Clock (CK⁺, CK⁻) inputs to the MAX171 are unbuffered LEDs and require a series resistor of typically 470 Ω to a TTL or 5V-CMOS gate to set the drive current. The preferred connection is to tie the resistor from +5V to the LED anode and then connect logic LED cathode as shown in Figure 1. Alternatively, logic drive current may be sourced to a grounded LED, but this requires opposite logic polarity from Figure 1 for both the Start and Clock signals.

The serial data output is an open-collector NPN bipolar transistor, and normally requires a 470 Ω pull-up resistor to a +5V supply. The external stray capacitance at the DATA output pin should be kept below 10pF for operation at the maximum clock rate. A low signal at the DATA output represents a logical "1" in the output word.

Power Supplies

The MAX171 requires three power supplies: +5V and -12V to -15V is required on the isolated analog side of the package (ISO V⁺, ISO V⁻). A separate +5V voltage source (V_{CC}) is required on the digital side of the isolation barrier for the DATA output transmitter.

Digital Interface

Clock — Data Skew

While the opto-isolators used in the MAX171 are fast enough for the specified conversion speed of 5.8 μ s, they do add a time delay that impacts high speed operation. The A/D cannot begin processing a clock edge before it crosses the isolation barrier. Therefore, the digital I/O signals at the A/D lag/lead the digital signals at the input/output pins. For example, as each successive approximation decision is sent out, it appears at the DATA pin following a delay induced by the opto-coupler. At low conversion rates (below 1MHz clock) these delays are negligible and Clock and Start signals may be applied simultaneously to the MAX171 and to the output register. At clock speeds above 1MHz, these delays become a significant portion of the clock cycle and must be compensated for best performance. Figure 3 illustrates using delay lines in the start and clock signals applied to the output register.

Timing and Control

A conversion cycle is initiated on the rising edge of the conversion start signal that is coincident with a falling edge of the Clock signal. Figure 4 shows a single conversion cycle with a continuous Clock. Once started, a conversion cannot be stopped and transitions at the Start input have no effect until the CURRENT conversion is completed (minimum of 14 clock cycles from the last rising edge of the conversion start signal).

Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

MAX171

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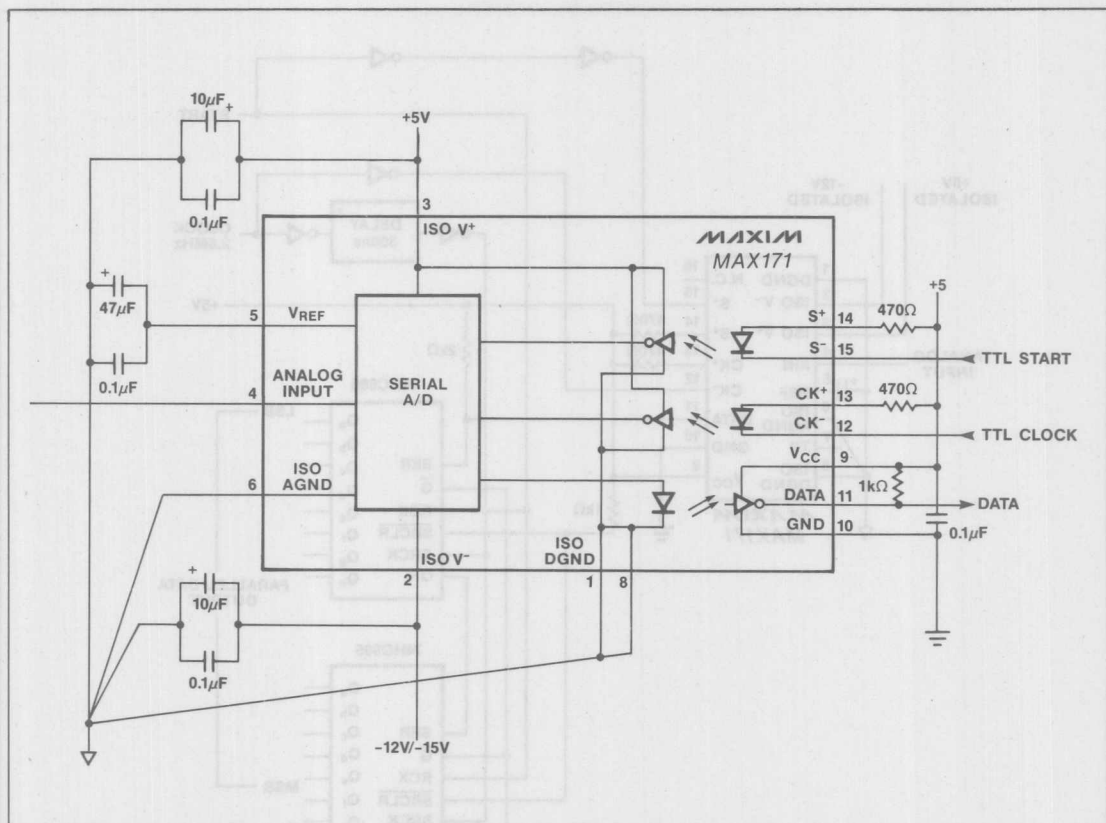


Figure 1. MAX171 Operating Circuit

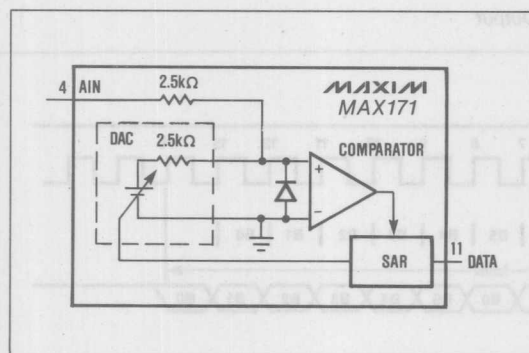


Figure 2. MAX171 Analog Equivalent Circuit

The Conversion Start transition causes the SAR to set B11 (MSB), driving the DAC output to half-scale. The analog input is compared to this value from the time of the conversion start transition until the second falling Clock edge which latches the MSB result and sets the SAR to compare the next bit. The MSB result appears at the DATA output after a delay, t_{PD} from the falling edge of Clock. Each subsequent bit conversion proceeds similarly until all 12 bits of the DAC have been tried. The conversion is completed at the falling edge of the 13th Clock cycle. The DATA output returns high at the falling edge of the 14th Clock cycle and remains so until the next conversion sends out its MSB result.

The next conversion can be started on the 14th Clock cycle of a previous conversion as shown in Figure 4. This allows the maximum throughput rate, one conversion per 14 Clock cycles.

Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

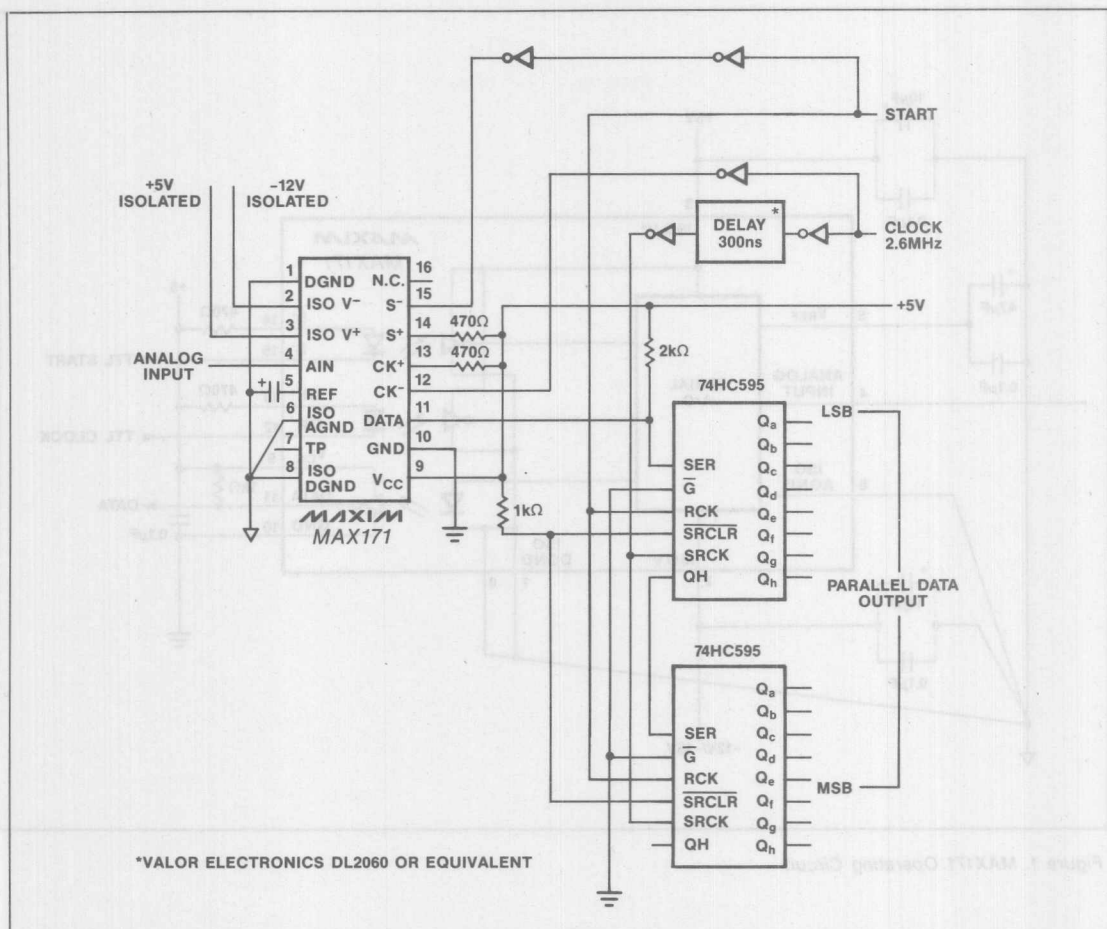


Figure 3. MAX171 Opto-Isolated Conversion with Parallel Data Output

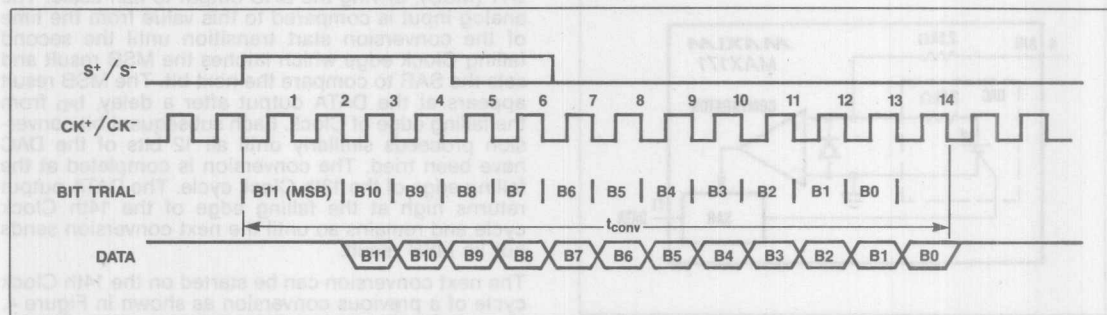


Figure 4. MAX171 Conversion Cycle Timing

MAX771



Conversion Start Timing

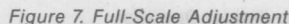
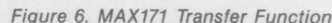
Output Coding

Applications

Unipolar Input Operation

Offset and Full Scale Adjustment

To adjust the full scale range, apply FS - 3/2LSB (4.9817V) at the analog input and adjust R1 until the output code changes between 1111 1111 1110 and 1111 1111 1111.



Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

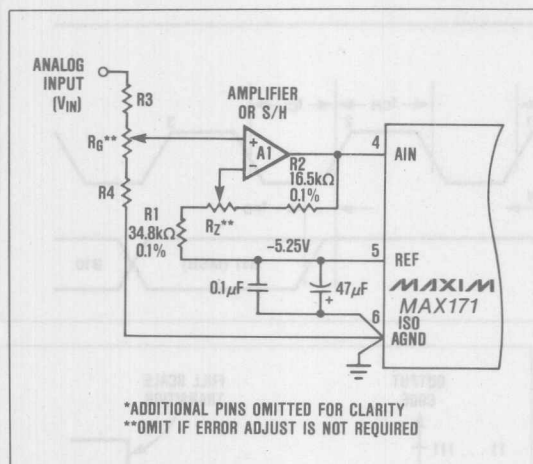


Figure 8. MAX171 Non-Inverting Bipolar Operation

Table 1. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 8

V _{IN} Range (Volts)	R3* (kΩ)	R4* (kΩ)	R _Z (Ω)	R _G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	3.83	8.25	500	500	0.61	2.49817
±5.0	33.2	16.9	500	1000	1.22	4.99634
±10.0	47.5	9.53	500	500	2.44	9.99268

*R3 and R4 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

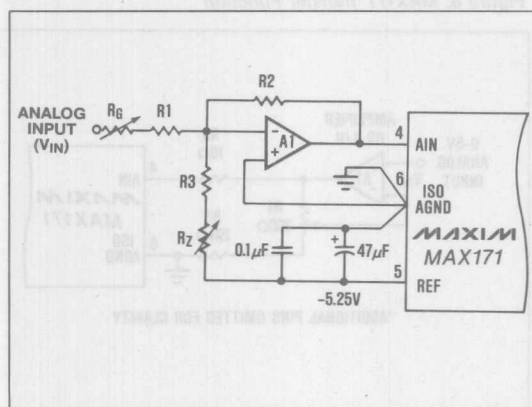


Figure 9. MAX171 Inverting Bipolar Operation

Table 2. Resistor and Potentiometer Values Required for Offset and Gain Adjustment of Figure 9

V _{IN} Range (Volts)	R1* (kΩ)	R2* (kΩ)	R3* (kΩ)	R _Z (Ω)	R _G (Ω)	1/2LSB (mV)	FS/2-3/2LSBs (Volts)
±2.5	20	20.5	42.2	2000	1000	0.61	2.49817
±5.0	20	10.2	21	1000	1000	1.22	4.99634
±10.0	20	5.11	10.5	500	1000	2.44	9.99268

*R1, R2 and R3 have a 0.1% tolerance. All resistors are standard EIA/MIL decade values.

Bipolar Input Operation

Bipolar operation can be achieved in two modes: non-inverting and inverting. For both cases, the amplifier shown in the circuits can be replaced by the AD585 or HA5320 sample-and-hold amplifiers. Several different input ranges are possible by selecting the values for the scaling resistors as shown in Tables 1 and 2.

Figure 8 shows the bipolar operation in the non-inverting mode, where the output coding is offset binary. Figure 10 shows the ideal transfer function for this mode.

Figure 9 shows the bipolar operation in the inverting mode where the output coding is complementary offset binary. Figure 10 shows the ideal transfer function for the circuit in Figure 9.

The resistors used in bipolar applications should be of the same type and from the same manufacturer to obtain low temperature drift. 0.1% resistors are recommended for applications where offset and full scale adjustments must be made in bipolar circuits. If high tolerances are used, larger value potentiometers must be used and this results in poor sensitivity and higher temperature drifts.

Offset and Full Scale Adjustment

Offset should always be adjusted before full scale. For both circuits apply +1/2LSB to the analog input (see Tables 1 and 2) and adjust R_Z until the output code flickers between the following codes:

For Non-Inverting (Figure 8) 1000 0000 0000
1000 0000 0001

For Inverting (Figure 9) 0111 1111 1111
0111 1111 1110

Apply FS - 3/2LSB (See Tables 1 and 2) to the input and adjust R_G until the ADC output code flickers between the following codes:

For Non-Inverting (Figure 8) 1111 1111 1110
1111 1111 1111

For Inverting (Figure 9) 0000 0000 0001
0000 0000 0000

Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

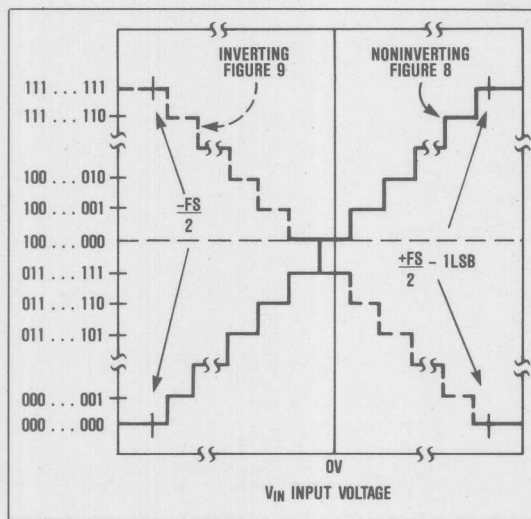


Figure 10. Ideal Input/Output Transfer Characteristics for the Bipolar Circuits in Figures 8 and 9

MAX171 to Sample-and-Hold Interface

The analog input to the MAX171 must be stable to within $\pm 1/2$ LSB during the entire conversion for specified 12-bit accuracy. This limits the input signal bandwidth to a few Hertz for sinusoidal inputs. For higher bandwidth signals a sample-and-hold should be used.

The signal that starts a conversion can be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. Note that this signal is not available on the isolated side of the barrier and must be separately coupled. The MAX171's DAC is switched at approximately the same time as the sample-and-hold amplifier starts holding the signal. The sample-and-hold amplifier should switch to the HOLD mode before there are any disturbances on the input signal, otherwise code dependent errors will be observed. These can be avoided by starting the MAX171 slightly after the TRACK/HOLD signal by using a gate delay. For synchronous conversion start and CK^+ , CK^- as described above, the maximum allowable hold settling time for the sample-and-hold is 600ns.

Circuit Layout

For best system performance printed circuit boards should be used for the MAX171. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX171 package.

The pin configuration of the MAX171 is designed to provide optimum electrical isolation in printed circuit layouts. To maintain this capability, connections from

the analog side (Pins 1-8) of the A/D should be separated from the digital side (Pins 9-16) and should not reach or run underneath the package. In some cases it may be best to "notch" or cut out the circuit board material to form an air gap between the pin rows.

Grounding

No special precautions are necessary for the ground connection on the digital side of the MAX171. Connect GND (Pin 10) near the ground of the device that will receive the data. The isolated analog ground (ISO AGND, Pin 6) must be connected to the isolated digital ground pins (ISO DGND, Pins 1 and 8), and together they should be tied to the ground of the analog signal. No connection is needed between GND (Pin 10) and the isolated grounds.

Power-Supply Bypassing

The comparator in the MAX171 is sensitive to high frequency noise in the analog power supplies (ISO V^+ , ISO V^-). These supplies should be bypassed close to the device with 0.1 μ F and 10 μ F capacitors with minimum lead length. If ISO V^+ is very noisy, a small resistor (10 Ω to 20 Ω) or inductor can be connected in series to form a low-pass filter with the by-pass capacitors. The digital +5V supply (V_{CC}) should be bypassed to GND with 0.1 μ F for best performance.

Internal Reference

The MAX171's on-chip reference is laser-trimmed to $-5.25V \pm 1\%$. The reference output is available at REF (Pin 5) as a reference source for other components and also drives the internal DAC.

For minimum noise, REF must be bypassed with a 47 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor to maintain a low impedance at high frequencies (Figure 1). This capacitance also stabilizes the internal reference buffer amplifier preventing oscillations. No series resistance should be used between REF and the bypass capacitors.

Driving the Analog Input

The input signal leads to AIN and GND should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2.5k Ω . The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion. The output impedance of the driving amplifier is reduced by the loop gain at the frequency of interest. With a maximum clock rate of 2.5MHz, amplifiers like the OP-42, AD711, or OP-27 are recommended. At a 1MHz clock rate, a MAX400 or OP-07 can be used.

LH17 Module Product Reliability

For reliability data on Maxim's Module Product Line, consult factory for Reliability Report RR-4A.

Opto-Isolated Serial Output 5.8 μ s 12-Bit A/D Converter

the analog side (Pins 1-5) of the A/D should be separated from the digital side (Pins 6-10) and should not reach or run underneath the package in some cases it may be best to "notch" or cut out the circuit board material to form an air gap between the pin rows.

Grounding

No special precautions are necessary for the ground connection on the digital side of the MAX171. Connect GND (Pin 10) near the ground of the device that will receive the data. The isolated analog ground (AGND, Pin 6) must be connected to the isolated digital ground pins (ISO GND, Pins 1 and 8), and together they should be tied to the ground of the analog signal. No connection is needed between GND (Pin 10) and the isolated ground.

Power-Supply Bypassing

The comparator in the MAX171 is sensitive to high frequency noise in the analog power supplies (ISO V₊, ISO V₋). These supplies should be bypassed close to the device with 0.1 μ F and 10 μ F capacitors with minimum lead length. If ISO V₋ is very noisy a small resistor (10 Ω to 50 Ω) or inductor can be connected in series to form a low-pass filter with the bypass capacitor. The digital +5V supply (V_{CC}) should be bypassed to GND with 0.1 μ F for best performance.

Internal Reference

The MAX171's on-chip reference is laser-trimmed to $\pm 25V \pm 1\%$. The reference output is available at REF (Pin 5) as a reference source for other components and also drives the internal DAC.

For minimum noise, REF must be bypassed with a 0.1 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor to maintain a low impedance at high frequencies (Figure 1). This capacitor also stabilizes the internal reference buffer amplifier preventing oscillations. No series resistance should be used between REF and the bypass capacitor.

Driving the Analog Input

The input signal leads to AIN and GND should be as short as possible to minimize noise pick-up. If the leads must be long use shielded cables to minimize noise pick-up.

The input impedance at the AIN pin is typically 2k Ω . The amplifier driving AIN must have low enough DC output impedance for low gain error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during a conversion. The output impedance of the driving amplifier is reduced by the loop gain at the frequency of interest. With a maximum clock rate of 2.5MHz, amplifiers like the OP-42, AD711, or OP-27 are recommended. At a 1MHz clock rate, a MAX400 or OP-07 can be used.

MAX171 Module Product Reliability

For reliability data on Maxim's Module Product Line.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

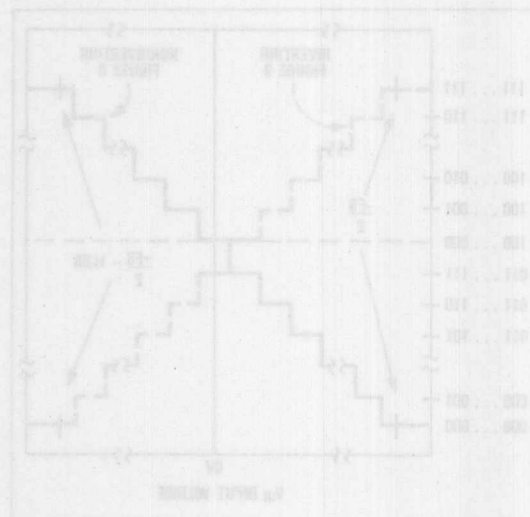


Figure 10: Ideal Input/Output Transfer Characteristics for the Block Circuit in Figures 5 and 6

MAX171 to Sample-and-Hold Interface

The analog input to the MAX171 must be stable to within $\pm 0.25V$ during the entire conversion for specified 12-bit accuracy. The input signal must have a bandwidth of a few MHz for sinusoidal inputs. For higher bandwidth signals a sample-and-hold should be used.

The signal that starts a conversion can be used to provide the TRACK/HOLD signal to the sample-and-hold amplifier. Note that this signal is not available on the isolated side of the barrier and must be separately coupled. The MAX171's DAC is switched at approximately the same time as the sample-and-hold amplifier starts holding the signal. The sample-and-hold amplifier should switch to the HOLD mode before there are any disturbances on the input signal. Otherwise, large errors will be observed. These errors can be avoided by starting the MAX171 slightly after the TRACK/HOLD signal by using a gate delay. For asynchronous conversion start and CK, CK' as described above, the maximum allowable hold setting time for the sample-and-hold is 800ns.

Circuit Layout

For best system performance printed circuit boards should be used for the MAX171. Wire-wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or right lines underneath the MAX171 package.

The pin configuration of the MAX171 is designed to

Complete 10 μ s CMOS 12-Bit ADC

General Description

The MAX172 is a complete 12-Bit analog-to-digital converter (ADC) that combines high speed, low power consumption, and an on-chip voltage reference. The conversion time is 10 μ s. The buried zener reference provides low drift and low noise performance.

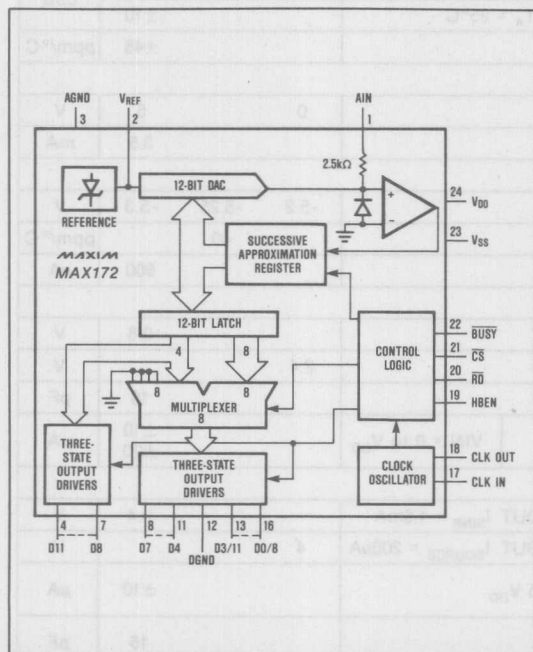
External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, can be used with a crystal.

The MAX172 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90 and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)
High Accuracy Process Control
High Speed Data Acquisition
Electro-Mechanical Systems

Functional Diagram



Features

- ◆ 12-Bit Resolution and Linearity
- ◆ 10 μ s Conversion Time
- ◆ No Missing Codes
- ◆ On-Chip Voltage Reference
- ◆ 90ns Access Time
- ◆ 215mW Max Power Consumption
- ◆ 24-Lead Narrow DIP Package
- ◆ Pin-for-Pin AD7572 Replacement

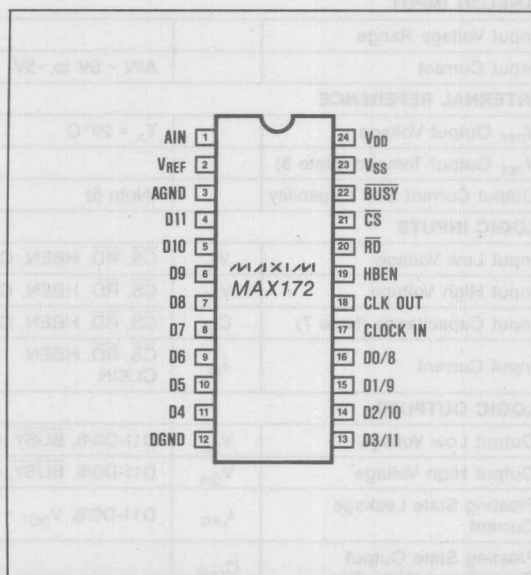
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX172ACNG	0°C to +70°C	Plastic DIP	$\pm 1/2$ LSB
MAX172BCNG	0°C to +70°C	Plastic DIP	± 1 LSB
MAX172ACWG	0°C to +70°C	Wide S.O.	$\pm 1/2$ LSB
MAX172BCWG	0°C to +70°C	Wide S.O.	± 1 LSB
MAX172CC/D	0°C to +70°C	Dice**	± 1 LSB
MAX172AING	-25°C to +85°C	Plastic DIP	$\pm 1/2$ LSB
MAX172BING	-25°C to +85°C	Plastic DIP	± 1 LSB
MAX172AMRG	-55°C to +125°C	CERDIP	$\pm 1/2$ LSB
MAX172BMRG	-55°C to +125°C	CERDIP	± 1 LSB

* All devices — 24 lead packages

** Consult factory for dice specifications

Pin Configuration



Complete 10 μ s CMOS 12-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND	-0.3V to +7V
V_{SS} to DGND	+0.3V to -17V
AGND to DGND	-0.3V, $V_{DD} + 0.3V$
AIN to AGND	-15V to +15V
Digital Input Voltage to DGND (Pins 17, 19-21)	-0.3V, $V_{DD} + 0.3V$
Digital Output Voltage to DGND (pins 4-11, 13-16, 18, 22)	-0.3V, $V_{DD} + 0.3V$

Operating Temperature Ranges

MAX172XC	0°C to +70°C
MAX172XI	-25°C to +85°C
MAX172XM	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Power Dissipation (any Package) to +75°C	1000mW
Derates Above +75°C by	10mW/°C
Lead Temperature (Soldering 10 seconds)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = +5V \pm 5\%$, $V_{SS} = -12V$ or $-15V \pm 5\%$; Slow Memory Mode; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted, $f_{CLK} = 1.25MHz$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral NonLinearity	INL	MAX172A	$T_A = 25^{\circ}\text{C}$			$\pm 1/2$	LSB
		MAX172AC/AI				$\pm 1/2$	
		MAX172AM				$\pm 3/4$	
		MAX172B				± 1	
Differential NonLinearity	DNL	Guaranteed Monotonic Over Temp.				± 1	LSB
Offset Error (Note 1)		MAX172B	$T_A = 25^{\circ}\text{C}$ $T_A = T_{\text{MIN}}$ to T_{MAX}			± 4 ± 6	LSB
		MAX172A	$T_A = 25^{\circ}\text{C}$ $T_A = T_{\text{MIN}}$ to T_{MAX}			± 3 ± 4	
Full Scale Error (Note 2)		MAX172B	$T_A = 25^{\circ}\text{C}$			± 15	LSB
		MAX172A	$T_A = 25^{\circ}\text{C}$			± 10	
Full Scale Tempco (Notes 3, 4)						± 45	ppm/ $^{\circ}\text{C}$
ANALOG INPUT							
Input Voltage Range				0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V _{REF} Output Voltage		T _A = 25°C		-5.2	-5.25	-5.3	V
V _{REF} Output Tempco (Note 5)					40		ppm/ $^{\circ}\text{C}$
Output Current Sink Capability		(Note 6)				500	μA
LOGIC INPUTS							
Input Low Voltage	V _{IL}	CS, RD, HBEN, CLKIN				0.8	V
Input High Voltage	V _{IH}	CS, RD, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C _{IN}	CS, RD, HBEN, CLKIN				10	pF
Input Current	I _{IN}	CS, RD, HBEN CLKIN	VIN = 0 to V _{DD}			± 10 ± 20	μA
LOGIC OUTPUTS							
Output Low Voltage	V _{OL}	D11-D0/8, BUSY, CLKOUT I _{SINK} = 1.6mA				0.4	V
Output High Voltage	V _{OH}	D11-D0/8, BUSY, CLKOUT I _{SOURCE} = 200μA		4			V
Floating State Leakage Current	I _{LKG}	D11-D0/8, V _{OUT} = 0V to V _{DD}				± 10	μA
Floating State Output Capacitance (Note 7)	C _{OUT}					15	pF

Complete 10 μ s CMOS 12-Bit ADC

MAX172

ELECTRICAL CHARACTERISTICS (Continued)

(V_{DD} = +5V \pm 5%, V_{SS} = -12V or -15V \pm 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 1.25MHz.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION TIME						
MAX172	t _{CONV}	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	9.6		10 10.4	μ s
POWER SUPPLY REJECTION						
V _{DD} Only		FS Change, V _{SS} = -15V, V _{DD} = 4.75V to 5.25V		\pm 1/2		LSB
V _{SS} Only		FS Change, V _{DD} = 5V, V _{SS} = -5% to +5%		\pm 1/8		LSB
POWER REQUIREMENTS						
V _{DD}		\pm 5% for Specified Performance		5		V
V _{SS} (Note 8)		\pm 5% for Specified Performance		-12 or -15		V
I _{DD}		$\overline{\text{CS}} = \overline{\text{RD}} = \text{V}_{\text{DD}}$, AIN = 5V		5	7	mA
I _{SS}		$\overline{\text{CS}} = \overline{\text{RD}} = \text{V}_{\text{DD}}$, AIN = 5V		8	12	mA
Power Dissipation		V _{DD} = +5V, V _{SS} = -15V		145	215	mW

Note 1: Typical change over temp is \pm 1 LSB.

Note 2: V_{DD} = +5V, V_{SS} = -15V, FS = +5,000V, Ideal last code transition = FS - 3/2LSB.

Note 3: Full Scale TC = $\Delta\text{FS}/\Delta\text{T}$, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.

Note 4: Includes internal reference drift.

Note 5: V_{REF} TC = $\Delta\text{V}_{\text{REF}}/\Delta\text{T}$, where $\Delta\text{V}_{\text{REF}}$ is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.

Note 6: Output current should not change during conversion.

Note 7: Guaranteed by design, not subject to test.

Note 8: Functional operation at V_{SS} = -12V \pm 5% is guaranteed by testing offset error and full scale error.

TIMING CHARACTERISTICS (Note 9)

(V_{DD} = +5V, V_{SS} = -12V or -15V; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T _A = 25°C			MAX172C/I		MAX172M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time	t ₁		0			0		0		ns
$\overline{\text{RD}}$ to BUSY Delay	t ₂	C _L = 50pF		90	190		230		270	ns
Data Access Time (Note 10)	t ₃	C _L = 20pF C _L = 100pF		60 70	90 125		110 150		120 170	ns
$\overline{\text{RD}}$ Pulse Width	t ₄		t ₃			t ₃		t ₃		
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time	t ₅		0			0		0		ns
Data Setup Time After $\overline{\text{BUSY}}$ Note (10)	t ₆			70		90		100		ns
Bus Relinquish Time (Note 11)	t ₇		20		75	20	85	20	90	ns
HBEN to $\overline{\text{RD}}$ Setup Time	t ₈		0			0		0		ns
HBEN to $\overline{\text{RD}}$ Hold Time	t ₉		0			0		0		ns
Delay Between Read Operations	t ₁₀		200			200		200		ns

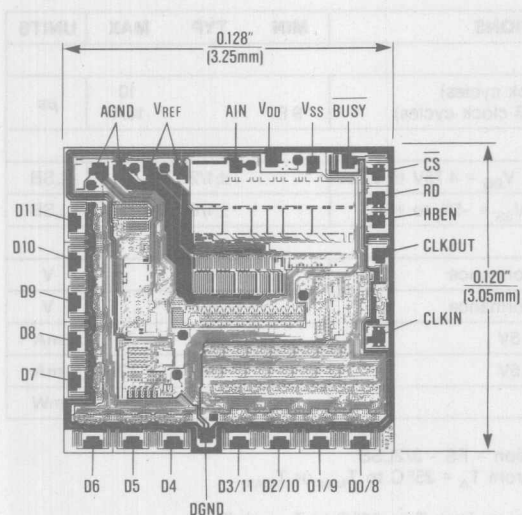
Note 9: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 10: t₃ and t₆ are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 11: t₇ is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

For additional information on using the MAX172 please refer to MAX162 data sheet.

Chip Topography



PARAMETER	SYMBOL	CONDITIONS	T _A = 25°C		MAXIMUM	UNIT
			MIN	TYP	MAX	
CS to RD Setup Time	t _{CS-RD}		0		0	ns
RD to BUSY Delay	t _{RD-BUSY}	C _L = 50pF	20	180	230	ns
Data Access Time (Note 10)	t _{DA}	C _L = 100pF C _L = 100pF	60 70	90 125	110 130	ns
RD Pulse Width	t _{RD}		t _{RD}		t _{RD}	ns
CS to RD Hold Time	t _{CS-RD}		0		0	ns
Data Setup Time After BUSY (Note 10)	t _{DS}		10		90	ns
Data Retention Time (Note 11)	t _{DR}		20	75	20	ns
HBEN to RD Setup Time	t _{HBEN-RD}		0		0	ns
HBEN to RD Hold Time	t _{HBEN-RD}		0		0	ns
Bus Retention Read Conditions	t _{BR}		200		200	ns

Note 1: Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with $V_{DD} = 5V$ and $V_{SS} = 0V$ (GND) and V_{REF} is a voltage level of 1.6V.

Note 10: t_{DA} and t_{DS} are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 50% of V_{DD} or 50% of V_{SS} .

Note 11: t_{DR} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 2.

For additional information on using the MAX172 please refer to MAX182 data sheet.

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Complete 5 μ s CMOS 10-Bit A/D Converter

General Description

The MAX173 is a complete, 10-bit linear analog-to-digital converter (ADC) that combines high speed, low power consumption, and an on-chip voltage reference. The conversion time is 5 μ s. The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, from a crystal.

The MAX173 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90ns and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Features

- ◆ 12-Bit Resolution and 10-Bit Linearity
- ◆ 5 μ s Conversion Time
- ◆ On-Chip ± 40 ppm/ $^{\circ}$ C Voltage Reference
- ◆ 90ns Access Time
- ◆ 215mW (Max) Power Consumption
- ◆ 24-Lead Narrow DIP and Wide SO Packages

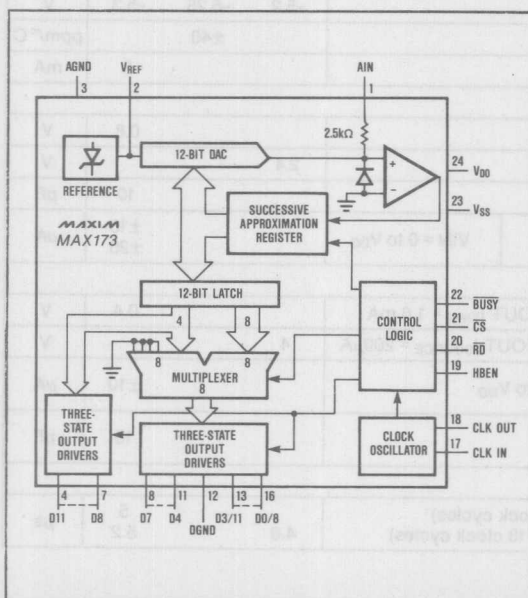
Ordering Information

PART	TEMP. RANGE	PACKAGE*
MAX173CNG	0 $^{\circ}$ C to +70 $^{\circ}$ C	Plastic DIP
MAX173CWG	0 $^{\circ}$ C to +70 $^{\circ}$ C	Wide SO
MAX173C/D	0 $^{\circ}$ C to +70 $^{\circ}$ C	Dice**
MAX173ENG	-40 $^{\circ}$ C to +85 $^{\circ}$ C	Plastic DIP
MAX173EWG	-40 $^{\circ}$ C to +85 $^{\circ}$ C	Wide SO
MAX173MRG	-55 $^{\circ}$ C to +125 $^{\circ}$ C	CERDIP

* All devices — 24 lead packages

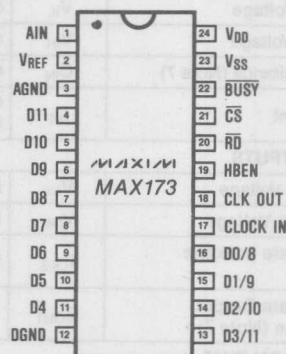
** Consult factory for dice specifications.

Functional Diagram



Pin Configurations

Top View



Complete 5 μ s CMOS 10-Bit A/D Converter

ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND	-0.3V to +7V
V _{SS} to DGND	+0.3V to -17V
AGND to DGND	-0.3V, V _{DD} + 0.3V
AIN to AGND	-15V to +15V
Digital Input Voltage to DGND (Pins 17, 19-21)	-0.3V, V _{DD} + 0.3V
Digital Output Voltage to DGND (Pins 4-11, 13-16, 18, 22)	-0.3V, V _{DD} + 0.3V

Operating Temperature Ranges

MAX173XC	0°C to +70°C
MAX173XE	-40°C to +85°C
MAX173XM	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Power Dissipation (any Package) to +75°C	1000mW
Derates Above +75°C by	10mW/°C
Lead Temperature (Soldering 10 seconds)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V \pm 5%, V_{SS} = -12V or -15V \pm 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 2.5MHz.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
No Missing Code Resolution			10			Bits
Integral Non-Linearity	INL				± 0.05	%FSR
Offset Error (Note 1)					± 5	mV
Full Scale Error (Note 2)					± 0.4	%
Full Scale Tempco (Notes 3, 4)					± 45	ppm/°C
ANALOG INPUT						
Input Voltage Range			0		5	V
Input Current		AIN = 0V to +5V			3.5	mA
INTERNAL REFERENCE						
V _{REF} Output Voltage		T _A = 25°C	-5.2	-5.25	-5.3	V
V _{REF} Output Tempco (Note 5)				± 40		ppm/°C
Output Current Sink Capability		(Note 6)			5	mA
LOGIC INPUTS						
Input Low Voltage	V _{IL}	CS, RD, HBEN, CLKIN			0.8	V
Input High Voltage	V _{IH}	CS, RD, HBEN, CLKIN	2.4			V
Input Capacitance (Note 7)	C _{IN}	CS, RD, HBEN, CLKIN			10	pF
Input Current	I _{IN}	CS, RD, HBEN CLKIN			± 10 ± 20	μ A
LOGIC OUTPUTS						
Output Low Voltage	V _{OL}	D11-D0/8, BUSY, CLKOUT I _{SINK} = 1.6 mA			0.4	V
Output High Voltage	V _{OH}	D11-D0/8, BUSY, CLKOUT I _{SOURCE} = 200 μ A	4			V
Floating State Leakage Current	I _{LKG}	D11-D0/8, V _{OUT} = 0V to V _{DD}			± 10	μ A
Floating State Output Capacitance (Note 7)	C _{OUT}				15	pF
CONVERSION TIME						
MAX173	t _{CONV}	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)	4.8		5 5.2	μ s

Complete 5 μ s CMOS 10-Bit A/D Converter

MAX173

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +5V \pm 5\%$, $V_{SS} = -12V$ or $-15V \pm 5\%$; Slow Memory Mode; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted, $f_{CLK} = 2.5MHz$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REJECTION						
V_{DD} Only		FS Change, $V_{SS} = -15V$, $V_{DD} = 4.75V$ to $5.25V$		± 0.01		%
V_{SS} Only		FS Change, $V_{DD} = 5V$, $V_{SS} = -5\%$ to $+5\%$		± 0.01		%
POWER REQUIREMENTS						
V_{DD}		$\pm 5\%$ for Specified Performance		5		V
V_{SS} (Note 8)		$\pm 5\%$ for Specified Performance		-12 or -15		V
I_{DD}		$CS = RD = V_{DD}$, $A_{IN} = 5V$		5	7	mA
I_{SS}		$CS = RD = V_{DD}$, $A_{IN} = 5V$		8	12	mA
Power Dissipation		$V_{DD} = +5V$, $V_{SS} = -15V$		145	215	mW

Note 1: Typical change over temp is $\pm 1.2mV$.

Note 2: $V_{DD} = +5V$, $V_{SS} = -15V$, $FS = +5.000V$. Ideal last code transition = $FS - 1.8mV$.

Note 3: Full Scale $TC = \Delta FS / \Delta T$, where ΔFS is full scale change from $T_A = 25^\circ C$ to T_{MIN} or T_{MAX} .

Note 4: Includes internal reference drift.

Note 5: $V_{REF} TC = \Delta V_{REF} / \Delta T$, where ΔV_{REF} is reference voltage change from $T_A = 25^\circ C$ to T_{MIN} or T_{MAX} .

Note 6: Output current should not change during conversion.

Note 7: Guaranteed by design, not subject to test.

Note 8: Functional operation at $V_{SS} = -12V \pm 5\%$ is guaranteed by testing offset error and full scale error.

1

TIMING CHARACTERISTICS (Note 9) (See MAX162 data sheet for t_1 - t_{10} description)

($V_{DD} = +5V$, $V_{SS} = -12V$ or $-15V$; $T_A = T_{MIN}$ to T_{MAX} , specifications in bold type are 100% tested, others are guaranteed by design, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	$T_A = 25^\circ C$			MAX173C/E		MAX173M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CS to RD Setup Time	t_1		0			0		0		ns
RD to BUSY Delay (Note 12)	t_2	$C_L = 50pF$		90	190		230		270	ns
Data Access Time (Note 10)	t_3	$C_L = 20pF$		60	90		110		120	ns
Data Access Time (Notes 10, 12)	t_3	$C_L = 100pF$		70	125		150		170	ns
RD Pulse Width	t_4			t_3			t_3		t_3	
CS to RD Hold Time	t_5		0			0		0		ns
Data Setup Time After BUSY (Notes 10, 12)	t_6				80		105		120	ns
Bus Relinquish Time (Notes 11, 12)	t_7				75		85		90	ns
HBEN to RD Setup Time	t_8		0			0		0		ns
HBEN to RD Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 (see MAX162 data sheet) and defined as the time required for an output to cross 0.8V or 2.4V.

Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2 (see MAX162 data sheet).

Note 12: This specification is 100% production tested.

For additional information on using the MAX173 please refer to MAX162 data sheet.

MAX173

Figure 1 is a pin configuration diagram of the AD9225. It shows a square package with pins numbered 06 to 11 on the left and 00/8 to 03/11 on the bottom. Power pins at the top are AGND, VREF, AIN, VDD, VSS, and BUSY. Signal pins on the right are CS, RD, HBEN, CLKOUT, and CLKIN. Dimensions are 0.128 inches (3.25mm) for the width and 0.120 inches (3.05mm) for the height.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

Industry Standard Complete 12-Bit A/D Converters

MAX174/MX574A/MX674A

1

General Description

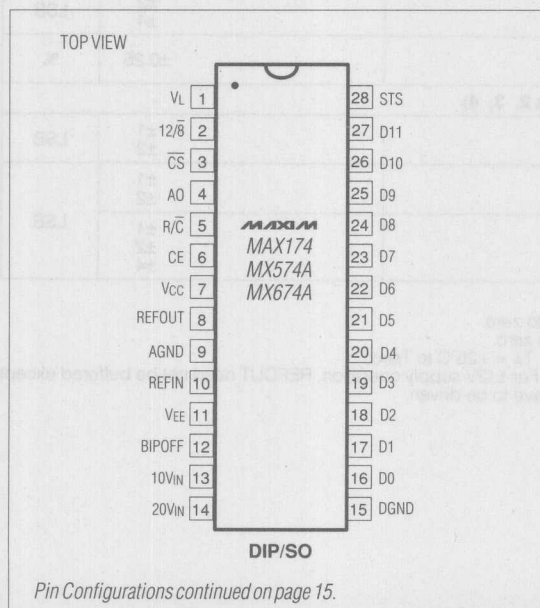
The MAX174 and the MX574A/MX674A are complete 12-bit analog-to-digital converters (ADCs) that combine high speed, low-power consumption, and on-chip clock and voltage reference. The maximum conversion times are 8 μ s (MAX174), 15 μ s (MX674A) and 25 μ s (MX574A). Maxim's BiCMOS construction reduces power dissipation 3 times (150mW) over comparable devices. The internal buried zener reference provides low-drift and low-noise performance. External component requirements are limited to only decoupling capacitors and fixed resistors. The versatile analog input structure allows for 0V to +10V or 0V to +20V unipolar or \pm 5V or \pm 10V bipolar input ranges with pin strapping.

The MAX174/MX574A/MX674A use standard microprocessor interface architectures and can be interfaced to 8-, 12- and 16-bit wide buses. Three-state data outputs are controlled by CS, CE and R/C logic inputs.

Applications

Digital Signal Processing
High-Accuracy Process Control
High-Speed Data Acquisition
Electro-Mechanical Systems

Pin Configurations



Features

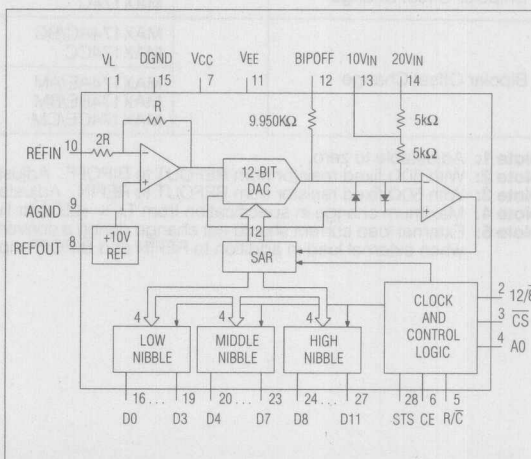
- ◆ Complete ADC with Reference and Clock
- ◆ 12-Bit Resolution and Linearity
- ◆ No Missing Codes Over Temperature
- ◆ 150mW Power Dissipation
- ◆ 8 μ s (MAX174), 15 μ s (MX674A) and 25 μ s (MX574A) Max Conversion Times
- ◆ Precision Low TC Reference: 10ppm/ $^{\circ}$ C
- ◆ Monolithic BiCMOS Construction
- ◆ 150ns Maximum Data Access Time

Ordering Information

PART	PIN-PACKAGE	LINEARITY (LSBs)	TEMPCO (ppm/ $^{\circ}$ C)
8 μ s Maximum Conversion Time			
TEMP. RANGE: 0 $^{\circ}$ C to +70 $^{\circ}$ C			
MAX174ACPI	28 Plastic DIP	1/2	10
MAX174BCPI	28 Plastic DIP	1/2	27
MAX174CCPI	28 Plastic DIP	1	50
MAX174ACWI	28 Wide SO	1/2	10
MAX174BCWI	28 Wide SO	1/2	27
MAX174CCWI	28 Wide SO	1	50
MAX174BC/D	Dice*	1/2	--

*Consult factory for dice specifications.
Ordering information continued on page 1-116.

Functional Diagram



MAXIM

Maxim Integrated Products 1-103

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Industry Standard Complete 12-Bit A/D Converters

ABSOLUTE MAXIMUM RATINGS

V _{CC} to DGND	0V to +16.5V
V _{EE} to DGND	0V to -16.5V
V _L to DGND	0V to +7V
DGND to AGND	±1V
Control Inputs to DGND (CE, CS, A0, 12/8, R/C)	-0.3V to V _{CC} + 0.3V
Digital Output Voltage to DGND (DB11-DB0, STS)	-0.3V, V _L + 0.3V
Analog Inputs to AGND (REFIN, BIPOFF, 10V _{IN})	±16.5V

20V _{IN} to AGND	±24V
REFOUT	Indefinite short to V _{CC} or AGND
Power Dissipation (any package) to +75°C	1000mW
Derates Above +75°C by	10mW/°C
Operating Temperature Ranges:	
MAX174_C, MX_74AJ/K/L	0°C to +70°C
MAX174_E, MX_74AJE/KE/LE	-40°C to +85°C
MAX174_M, MX_74AS/T/U	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX174

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	RES		12			Bits
Integral Nonlinearity	INL	T _A = +25°C MAX174A/B MAX174C			±1/2 ±1	LSB
		T _A = T _{MIN} to T _{MAX} MAX174AC/BC MAX174AE/BE/AM/BM MAX174C			±1/2 ±3/4 ±1	
Differential Nonlinearity	DNL	12 bits, no missing codes over temp			±1	LSB
Unipolar Offset Error (Note 1)		MAX174A/B MAX174C			±1 ±2	LSB
Bipolar Offset Error (Notes 2, 3)		MAX174A MAX174B/C			±2 ±4	LSB
Full-Scale Calibration Error (Note 3)					±0.25	%
TEMPERATURE COEFFICIENTS (Using Internal Reference, Notes 2, 3, 4)						
Unipolar Offset Change		MAX174A/B MAX174C			±1 ±2	LSB
Bipolar Offset Change		MAX174AC/BC MAX174CC			±1 ±2	LSB
		MAX174AE/AM MAX174BE/BM MAX174CE/CM			±1 ±2 ±4	

Note 1: Adjustable to zero.

Note 2: With 50Ω fixed resistor from REFOUT to BIPOFF. Adjustable to zero.

Note 3: With 50Ω fixed resistor from REFOUT to REFIN. Adjustable to zero.

Note 4: Maximum change in specification from T_A = +25°C to T_{MIN} or T_A = +25°C to T_{MAX}.

Note 5: External load current should not change during a conversion. For ±12V supply operation, REFOUT need not be buffered except when external load in addition to REFIN and BIPOFF inputs have to be driven.



Industry Standard Complete 12-Bit A/D Converters

MAX174/MX574A/MX674A

1

ELECTRICAL CHARACTERISTICS – MAX174 (continued)

($V_L = +5V$, $V_{CC} = +15V$ or $+12V$, $V_{EE} = -15V$ or $-12V$; $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full-Scale Calibration Change		MAX174AC				±2 (10)	LSB (ppm/°C)
		MAX174BC				±5 (27)	
		MAX174CC				±9 (50)	
		MAX174AE				±5 (19)	
		MAX174BE				±10 (38)	
		MAX174CE				±20 (75)	
		MAX174AM				±5 (12)	
		MAX174BM				±10 (25)	
		MAX174CM				±20 (50)	
INTERNAL REFERENCE							
Output Voltage		No Load	MAX174A MAX174B/C	9.98 9.97	10.00 10.00	10.02 10.03	V
Output Current (Note 5)		Available for external loads, in addition to REFIN and BIPOFF load				2	mA

ELECTRICAL CHARACTERISTICS – MX574A, MX674A

($V_L = +5V$, $V_{CC} = +15V$ or $+12V$, $V_{EE} = -15V$ or $-12V$; $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	RES		12			Bits
Integral Nonlinearity	INL	$T_A = +25^\circ C$ MX574AK/L/T/U, MX674AK/L/T/U, MX574AJ/S, MX674AJ/S			$\pm 1/2$ ± 1	LSB
		$T_A = T_{MIN}$ to T_{MAX} MX574AK/L, MX674AK/L, MX574AT/U/KE/LE, MX674AT/U/KE/LE, MX574AJ/S, MX674AJ/S			$\pm 1/2$ $\pm 3/4$ $\pm 3/4$ ± 1	
Differential Nonlinearity	DNL	12 bits, no missing codes over temp			± 1	LSB

Industry Standard Complete 12-Bit A/D Converters

ELECTRICAL CHARACTERISTICS – MX574A, MX674A (continued)

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Unipolar Offset Error (Note 1)		MX574AK/L/T/U, MX674AK/L/T/U MX574AJ/S, MX674AJ/S			±1 ±2	LSB
Bipolar Offset Error (Notes 2, 3)		MX574AL/U, MX674AL/U MX574AJ/K/S/T, MX674AJ/K/S/T			±2 ±4	LSB
Full-Scale Calibration Error (Note 3)		MX574AL/U MX574AJ/K/S/T, MX674A			±0.125 ±0.25	%
TEMPERATURE COEFFICIENTS (Using Internal Reference, Notes 2, 3, 4)						
Unipolar Offset Change		MX574AK/L/T/U, MX674AK/L/T/U MX574AJ/S, MX674AJ/S			±1 ±2	LSB
Bipolar Offset Change		MX574AK/L, MX674AK/L MX574AJ, MX674AJ			±1 ±2	LSB
		MX574AU/LE, MX674AU/LE MX574AT/KE, MX674AT/KE MX574AS/JE, MX674AS/JE			±1 ±2 ±4	
Full-Scale Calibration Change		MX574AL, MX674AL			±2 (10)	LSB (ppm/°C)
		MX574AK, MX674AK			±5 (27)	
		MX574AJ, MX674AJ			±9 (50)	
		MX574ALE, MX674ALE			±5 (19)	
		MX574AKE, MX674AKE			±10 (38)	
		MX574AJE, MX674AJE			±20 (75)	
		MX574AU, MX674AU			±5 (12)	
		MX574AT, MX674AT			±10 (25)	
		MX574AS, MX674AS			±20 (50)	
INTERNAL REFERENCE						
Output Voltage		No Load MX574AL/U MX574AJ/K/S/T, MX674AL/U MX674AJ/K/S/T	9.99 9.98 9.97	10.00 10.00 10.00	10.01 10.02 10.03	V
Output Current (Note 5)		Available for external loads, in addition to REFIN and BIPOFF load			2	mA

Note 1: Adjustable to zero.

Note 2: With 50Ω fixed resistor from REFOUT to BIPOFF. Adjustable to zero.

Note 3: With 50Ω fixed resistor from REFOUT to REFIN. Adjustable to zero.

Note 4: Maximum change in specification from T_A = +25°C to T_{MIN} or T_A = +25°C to T_{MAX}.

Note 5: External load current should not change during a conversion. For ±12V supply operation, REFOUT need not be buffered except when external load in addition to REFIN and BIPOFF inputs have to be driven.

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MAX174/MX574A/MX674A

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ELECTRICAL CHARACTERISTICS – MAX174/MX574A/MX674A

($V_L = +5V$, $V_{CC} = +15V$ or $+12V$, $V_{EE} = -15V$ or $-12V$; $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Bipolar Input Range		Using 10V Input				±5	V
		Using 20V Input				±10	
Unipolar Input Range		Using 10V Input		0		+10	V
		Using 20V Input		0		+20	
Input Impedance		10V Input		3	5	7	kΩ
		20V Input		6	10	14	
POWER-SUPPLY REJECTION (Max change in Full-Scale Calibration)							
VCC Only		+15V ±1.5V or +12V ±0.6V	MAX174A/B, MX_74AK/L/TU MAX174C, MX_74AJ/S	±1/8		±1	LSB
VEE Only		-15V ±1.5V or -12V ±0.6V			±1/8	±1/2	
VL Only		+5V ±0.5V			±1/8	±1/2	
LOGIC INPUTS							
Input Low Voltage	VIL	CS, CE, R/C, A0, 12/8				0.8	V
Input High Voltage	VIH	CS, CE, R/C, A0, 12/8			2.0		V
Input Current	IIN	CS, CE, R/C, A0, 12/8, VIN = 0 to VL				±5	μA
Input Capacitance	CIN	CS, CE, R/C, A0, 12/8				7	pF
LOGIC OUTPUTS							
Output Low Voltage	VOL	DB11-DB0, STS	ISINK = 1.6mA			0.4	V
Output High Voltage	VOH	DB11-DB0, STS	ISOURCE = 500μA	4			V
Floating State Leakage Current	ILKG	DB11-DB0, STS	VOUT = 0 to VL			±10	μA
Floating State Output Capacitance	COUT	DB11-DB0			8		pF
CONVERSION TIME							
12-Bit Cycle	tCONV	MX574A		15	20	25	μs
		MX674A		9	12	15	
		MAX174		6	7	8	
8-Bit Cycle	tCONV	MX574A		10	14	18	μs
		MX674A		6	8	11	
		MAX174		4	5	6	
POWER REQUIREMENTS							
VCC Operating Range				11.4		16.5	V
VL Operating Range				4.5		5.5	V
VEE Operating Range				-11.4		-16.5	V
VCC Supply Current (Note 5)	ICC				3	5	mA
VL Supply Current (Note 5)	IL				3	8	mA
VEE Supply Current (Note 5)	IEE				6	10	mA
Power Dissipation (Note 5)	PD	VCC = +15V and VEE = -15V			150	265	mW

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TIMING CHARACTERISTICS – MAX174/MX574A/MX674A (Note 6)

(V_L = +5V, V_{CC} = +15V or +12V, V_{EE} = -15V or -12V)

PARAMETER	SYMBOL	CONDITIONS	T _A = +25°C			T _A = -40°C to +85°C T _A = 0°C to +70°C		T _A = -55°C to +125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CONVERT START TIMING – FULL CONTROL MODE										
STS Delay from CE	tDSC	C _L = 50pF		100	200		250		320	ns
CE Pulse Width	tHEC		50	15		50		50		ns
CS to CE Setup	tSSC		50			50		50		ns
CS Low During CE High	tHSC		50			50		50		ns
R/C to CE Setup	tSRC		50			50		50		ns
R/C Low During CE High	tHRC		50			50		50		ns
A0 to CE Setup	tSAC		0			0		0		ns
A0 Valid During CE High	tHAC		50			50		50		ns
READ TIMING – FULL CONTROL MODE										
Access Time (from CE)	tDD	C _L = 100pF		60	120		150		200	ns
Data Valid after CE Low	tHD		25	40		20		15		ns
Output Float Delay	tHL				75		100		120	ns
C _S to CE Setup	tSSR		50			50		50		ns
R/C to CE Setup	tSRR		0			0		0		ns
A0 to CE Setup	tSAR		50			50		50		ns
C _S Valid After CE Low	tHSR		0			0		0		ns
R/C High After CE Low	tHRR		0			0		0		ns
A0 Valid After CE Low	tHAR		0			0		0		ns
STAND-ALONE MODE										
Low R/C Pulse Width	tHRL		50	15		50		50		ns
STS Delay from R/C	tDS			115	200		250		320	ns
Data Valid After R/C Low	tHDR		25	40		20		15		ns
STS Delay After Data Valid	tHS	MX574A	300	600	1000	300	1000	300	1000	ns
		MX674A	30	320	600	30	600	30	600	
		MAX174	30	140	300	30	300	30	400	
High R/C Pulse Width	tHRH		150			150		200		ns
Data Access Time	tDDR	C _L = 100pF		60	120		150		200	ns

Note 6: Timing specifications guaranteed by design. All input control signals specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. See loading circuits in Figures 1 and 2.

Industry Standard Complete 12-Bit A/D Converters

MAX174/MX574A/MX674A

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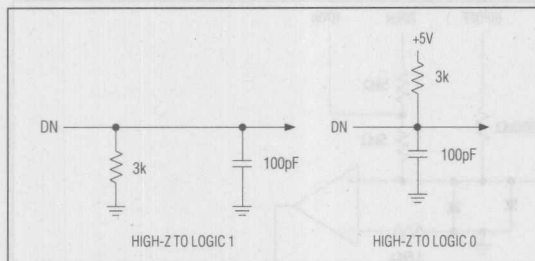


Figure 1. Load Circuit for Access Time Test

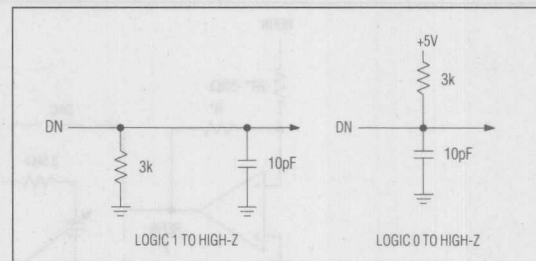


Figure 2. Load Circuit for Output Float Delay Test

Pin Description

PIN #	NAME	FUNCTION
1	V _L	Logic Supply, +5V
2	12/8	Data Mode Select Input
3	CS	Chip-Select Input. Must be low to select device.
4	A0	Byte Address/Short Cycle Input. When starting a conversion, controls number of bits converted (low = 12 bits, high = 8 bits). When reading data, if 12/8 = low, enables low byte (A0 = high) or high byte (A0 = low).
5	R/C	Read/Convert Input. When high, the device will be in the data-read mode. When low, the device will be in the conversion start mode.
6	CE	Chip-Enable Input. Must be high to select device.
7	V _{CC}	+12V or +15V Supply
8	REFOUT	+10V Reference Output
9	AGND	Analog Ground
10	REFIN	Reference Input
11	V _{EE}	-12V or -15V Supply
12	BIPOFF	Bipolar Offset Input. Connect to REFOUT for bipolar input range.
13	10V _{IN}	10V Span Input
14	20V _{IN}	20V Span Input
15	DGND	Digital Ground
16-27	D0-D11	Three-State Data Outputs
28	STS	Status Output

Converter Operation

The MAX174/MX574A/MX674A use a successive approximation technique to convert an unknown analog input to a 12-bit digital output code. The control logic provides easy interface to most microprocessors. Most applications require only a few external passive components to perform the analog-to-digital (A/D) function.

The internal voltage output DAC is controlled by a Successive Approximation Register (SAR) and has an output impedance of 2.5kΩ. The analog input is connected to the DAC output with a 5kΩ resistor for the 10V input and 10kΩ resistor for the 20V input. The comparator is essentially a zero crossing detector, and its output is fed back to the SAR input.

The SAR is set to half scale as soon as a conversion starts. The analog input is compared to 1/2 of the full-scale voltage. The bit is kept if the analog input is greater than half scale or dropped if smaller. The next bit, bit 10, is then set with the DAC output either at 1/4 scale, if the Most Significant Bit (MSB) is dropped, or 3/4 scale if the MSB is kept. The conversion continues in this manner until the Least Significant Bit (LSB) is tried. At the end of the conversion, the SAR output is latched into the output buffers.

Digital Interface

CE, CS, and R/C control the operation of the MAX174/MX574A/MX674A. While both CE and CS are asserted, the state of R/C selects whether a conversion (R/C = 0) or a data read (R/C = 1) is in progress. The register control inputs, 12/8 and A0, select the data format and conversion length. A0 is usually tied to the LSB of the address bus. To perform a full 12-bit conversion, set A0 low during a convert start. For a shorter 8-bit conversion, A0 must be high during a convert start.

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Table 2. MAX174/MX574A/MX674A Data Format for 8-Bit Bus

	D7	D6	D5	D4	D3	D2	D1	D0
High Byte (A0 = 0)	MSB	D10	D9	D8	D7	D6	D5	D4
Low Byte (A0 = 1)	D3	D2	D1	D0	0	0	0	0

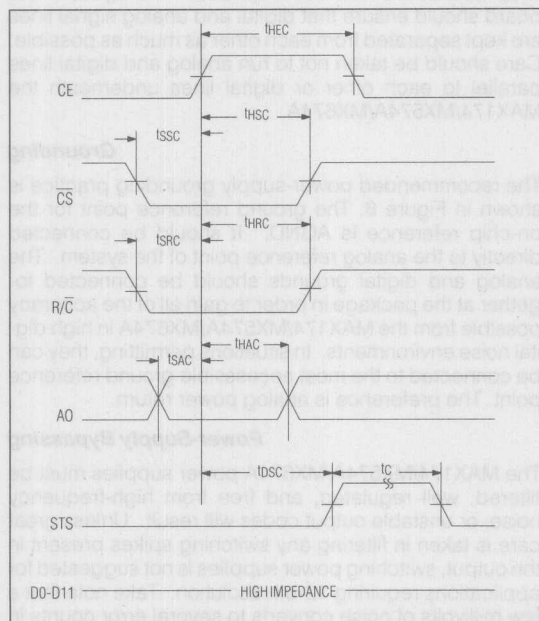
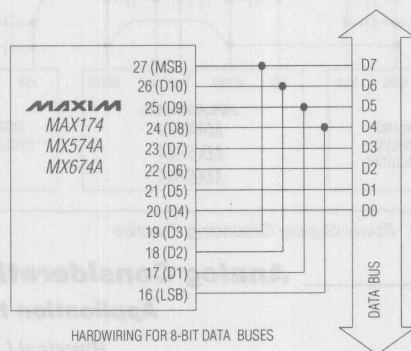


Figure 4. Convert Start Timing

Timing and Control Convert Start Timing - Full Control Mode

R/\overline{C} must be low before asserting both CE and \overline{CS} . If it is high, a brief read operation occurs possibly resulting in system bus contention. To initiate a conversion, use either CE or \overline{CS} . CE is recommended since it is shorter by one propagation delay than \overline{CS} and is the faster input of the two. CE is used to begin the conversion in Figure 4.

Once STS goes high, signaling that a conversion has started, all convert start commands will have no effect until the conversion is finished. Also, the output data buffers cannot be enabled during a conversion.

Read Timing - Full Control Mode

Figure 5 illustrates the read-cycle timing. While reading data, access time is measured from when CE and R/\overline{C} are both high. Access time is extended 10ns if \overline{CS} is used to initiate a read.

Stand-Alone Operation

For systems which do not use or require full bus interfacing, the MAX174/MX574A/MX674A can be operated in a stand-alone mode directly linked through dedicated input ports.

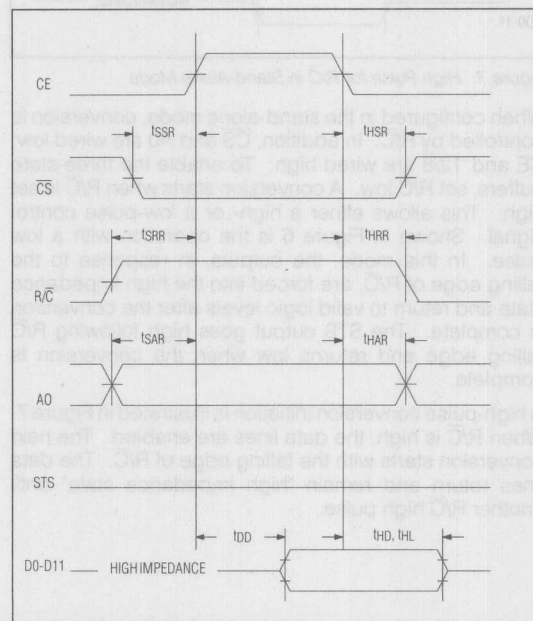


Figure 5. Read Timing

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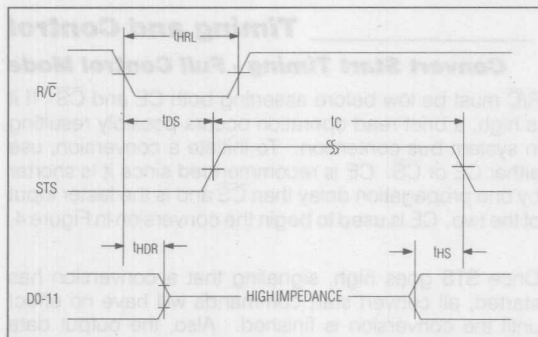


Figure 6. Low Pulse for R/\bar{C} in Stand-Alone Mode

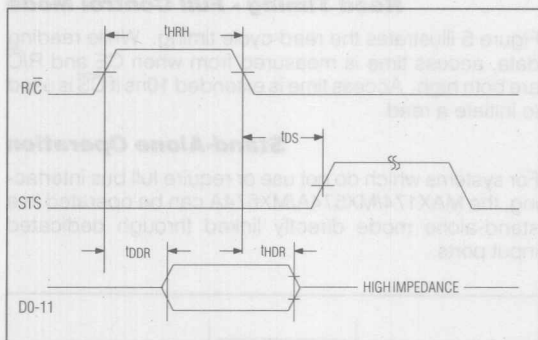


Figure 7. High Pulse for R/\bar{C} in Stand-Alone Mode

When configured in the stand-alone mode, conversion is controlled by R/\bar{C} . In addition, \bar{CS} and $A0$ are wired low; CE and $12/8$ are wired high. To enable the three-state buffers, set R/\bar{C} low. A conversion starts when R/\bar{C} is set high. This allows either a high- or a low-pulse control signal. Shown in Figure 6 is the operation with a low pulse. In this mode, the outputs, in response to the falling edge of R/\bar{C} , are forced into the high impedance state and return to valid logic levels after the conversion is complete. The STS output goes high following R/\bar{C} falling edge and returns low when the conversion is complete.

A high-pulse conversion initiation is illustrated in Figure 7. When R/\bar{C} is high, the data lines are enabled. The next conversion starts with the falling edge of R/\bar{C} . The data lines return and remain "high impedance state" until another R/\bar{C} high pulse.

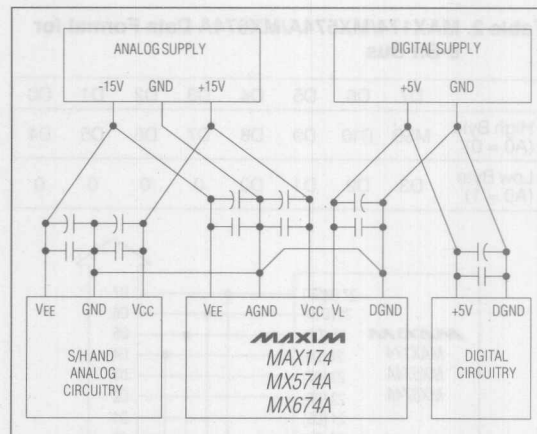


Figure 8. Power-Supply Grounding Practice

Analog Considerations

Application Hints

Physical Layout

For best system performance, printed circuit boards should be used for the MAX174/MX574A/MX674A. Wire-wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital lines parallel to each other or digital lines underneath the MAX174/MX574A/MX674A.

Grounding

The recommended power-supply grounding practice is shown in Figure 8. The ground reference point for the on-chip reference is $AGND$. It should be connected directly to the analog reference point of the system. The analog and digital grounds should be connected together at the package in order to gain all of the accuracy possible from the MAX174/MX574A/MX674A in high digital noise environments. In situations permitting, they can be connected to the most accessible ground reference point. The preference is analog power return.

Power-Supply Bypassing

The MAX174/MX574A/MX674A power supplies must be filtered, well regulated, and free from high-frequency noise, or unstable output codes will result. Unless great care is taken in filtering any switching spikes present in the output, switching power supplies is not suggested for applications requiring 12-bit resolution. Take note that a few millivolts of noise converts to several error counts in a 12-bit ADC.

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MAX174/MX574A/MX674A

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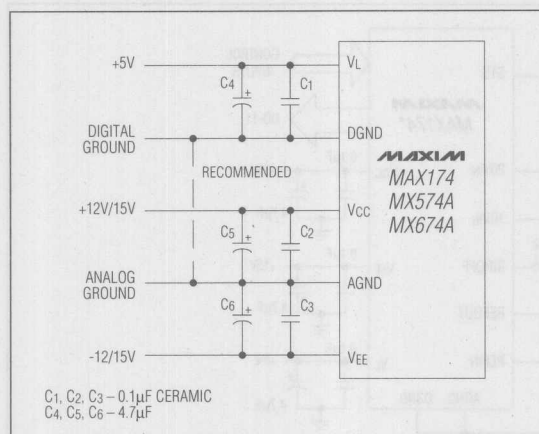


Figure 9. Power-Supply Bypassing

All power-supply pins should use supply decoupling capacitors connected with short lead length to the pins, as shown in Figure 9. The VCC and VEE pins should be decoupled directly to AGND. A 4.7µF tantalum type in parallel with a 0.1µF disc ceramic type is a suitable decoupling.

Internal Reference

The MAX174/MX574A/MX674A have an internal buried zener reference that provides a 10V, low-noise and low-temperature drift output. An external reference voltage can also be used for the ADC. When using ±15V supplies, the internal reference can source up to 2mA in

addition to the BIPOFF and REFIN inputs over the entire operating temperature range. With ±12V supplies, the reference can drive the BIPOFF and REFIN inputs over temperature, but it CANNOT drive an additional load.

Driving the Analog Input

The input leads to AGND and 10VIN or 20VIN should be as short as possible to minimize noise pick up. If long leads are needed, use shielded cables.

When using the 20VIN as the analog input, load capacitance on the 10VIN pin must be minimized. Especially on the faster MAX174, leave the 10VIN pin open to minimize capacitance and to prevent linearity errors caused by inadequate settling time.

The amplifier driving the analog input must have low enough DC output impedance for low full-scale error. Furthermore, low AC output impedance is also required since the analog input current is modulated at the clock rate during the conversion. The output impedance of an amplifier is the open-loop output impedance divided by the loop gain at the frequency of interest.

MX574A and MX674A - The approximate internal clock rate is 600kHz and 1MHz respectively, and amplifiers like the MAX400 can be used to drive the input.

MAX174 - The internal clock rate is 2MHz and faster amplifiers like the OP-27, AD711 or OP-42 are required.

Track-and-Hold Interface

The analog input to the ADC must be stable to within 1/2LSB during the entire conversion for specified 12-bit accuracy. This limits the input signal bandwidth to a

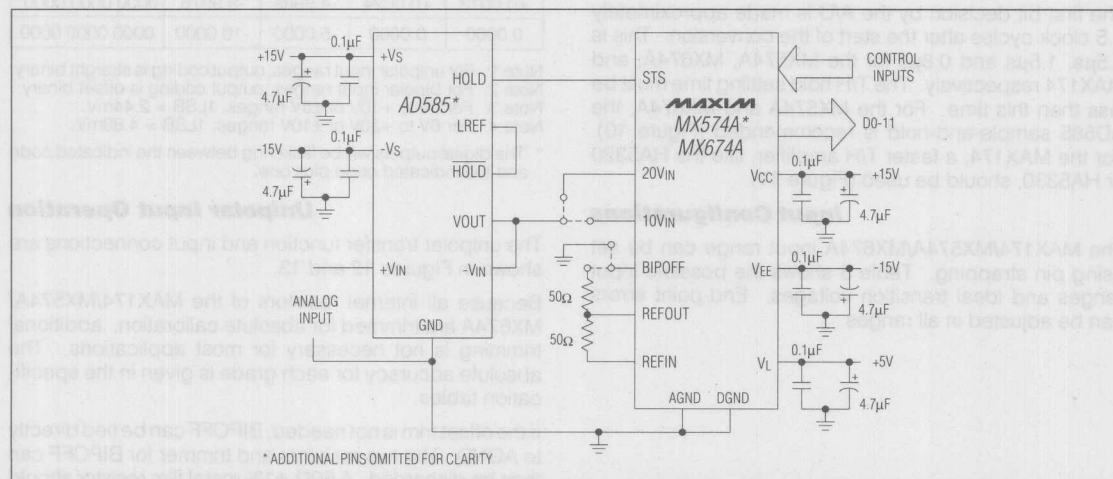


Figure 10. MX574A/MX674A to AD585 Sample-and-Hold Interface

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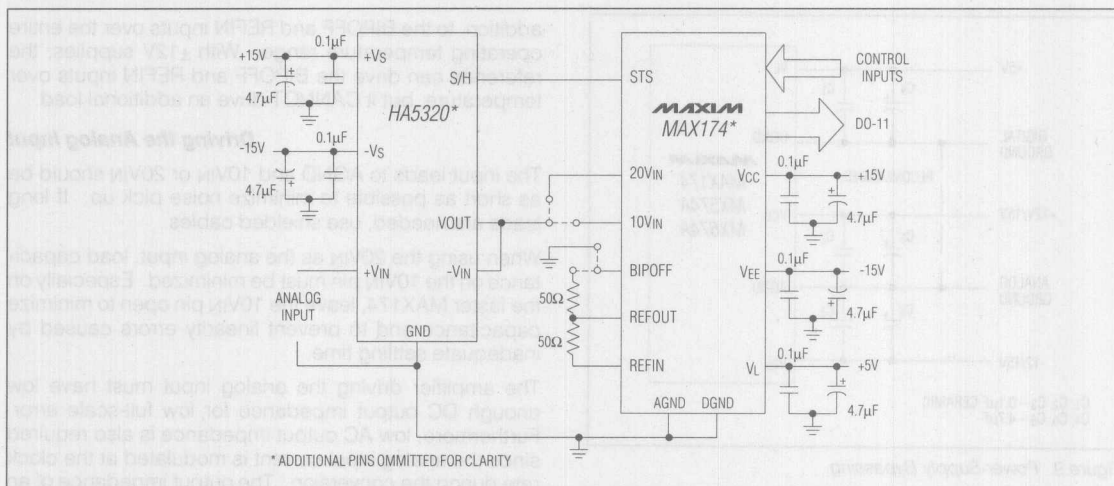


Figure 11. MAX174 to HA5320 Sample-and-Hold Interface

couple of hertz for sinusoidal inputs even with the faster MAX174. For higher bandwidth signals, a track-and-hold amplifier should be used.

The STS output may be used to provide the Hold signal to the track-and-hold amplifier. However, since the A/D's DAC is switched at approximately the same time as the conversion is initiated, the switching transients at the output of the T/H caused by the DAC switching may result in code dependent errors. It is recommended that the Hold signal to the T/H amplifier precede a conversion or be coincident with the conversion start.

The first bit decision by the A/D is made approximately 1.5 clock cycles after the start of the conversion. This is 2.5µs, 1.5µs and 0.8µs for the MX574A, MX674A, and MAX174 respectively. The T/H hold settling time must be less than this time. For the MX574A and MX674A, the AD585 sample-and-hold is recommended (Figure 10). For the MAX174, a faster T/H amplifier, like the HA5320 or HA5330, should be used (Figure 11).

Input Configurations

The MAX174/MX574A/MX674A input range can be set using pin strapping. Table 3 shows the possible input ranges and ideal transition voltages. End-point errors can be adjusted in all ranges.

Table 3. Input Ranges and Ideal Digital Output Codes

ANALOG INPUT VOLTAGE (Volts)				DIGITAL OUTPUT	
0 to +10V	0 to +20V	±5V	±10V	MSB	LSB
+10.0000	+20.0000	+5.0000	+10.0000	1111	1111 1111
+9.9963	+19.9927	+4.9963	+9.9927	1111	1111 1110*
+5.0012	+10.0024	+0.0012	+0.0024	1000	0000 0000*
+4.9988	+9.9976	-0.0012	-0.0024	0111	1111 1111*
+4.9963	+9.9927	-0.0037	-0.0073	0111	1111 1110*
+0.0012	+0.0024	-4.9988	-9.9976	0000	0000 0000*
0.0000	0.0000	-5.0000	-10.0000	0000	0000 0000

Note 1: For unipolar input ranges, output coding is straight binary.

Note 2: For bipolar input ranges, output coding is offset binary.

Note 3: For 0V to +10V or ±5V ranges, 1LSB = 2.44mV.

Note 4: For 0V to +20V or ±10V ranges, 1LSB = 4.88mV.

* The digital outputs will be flickering between the indicated code and the indicated code plus one.

Unipolar Input Operation

The unipolar transfer function and input connections are shown in Figures 12 and 13.

Because all internal resistors of the MAX174/MX574A/MX674A are trimmed for absolute calibration, additional trimming is not necessary for most applications. The absolute accuracy for each grade is given in the specification tables.

If the offset trim is not needed, BIPOFF can be tied directly to AGND. The two resistors and trimmer for BIPOFF can then be discarded. A 50Ω ±1% metal film resistor should be attached between REFOUT and REFIN.

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For a 0V to +10V input range, the analog input is connected between AGND and 10VIN. For a 0V to +20V input range, the analog input is connected between AGND and 20VIN. These ADCs can easily handle an input signal beyond the supplies. If full-scale trim is not needed, the gain trimmer, R2, should be swapped with a 50 Ω resistor. Should a 10.24V input range be selected, a 200 Ω trimmer should be inserted in series with 10VIN. For a full-scale input range of 20.48V, use a 500 Ω trimmer in series with 20VIN. The nominal input impedance into 10VIN is 5k Ω and 10k Ω for 20VIN.

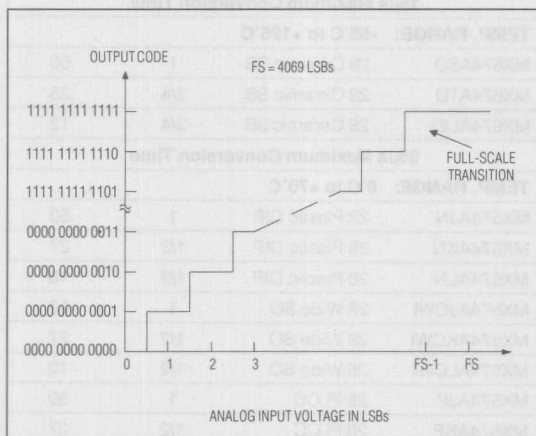


Figure 12. Ideal Unipolar Transfer Function

Offset and Full-Scale Adjustment

In applications where the offset and full-scale range have to be adjusted, use the circuit shown in Figure 12. The offset should be adjusted first. Apply 1/2LSB at the analog input and adjust R1 until the digital output code flickers between 0000 0000 0000 and 0000 0000 0001.

To adjust the full-scale range, apply FS - 3/2LSB at the analog input and adjust R2 until the output code changes between 1111 1111 1110 and 1111 1111 1111.

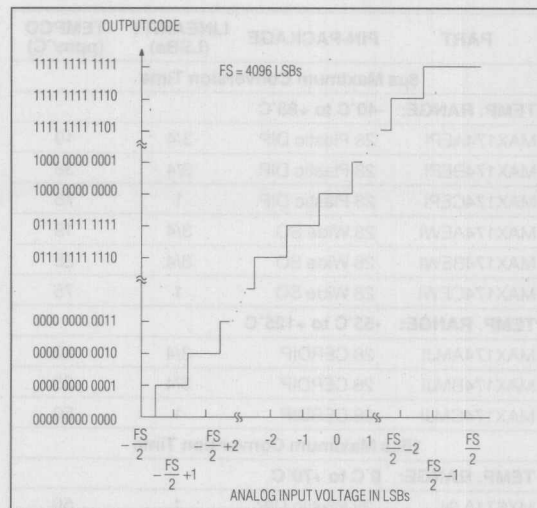


Figure 14. Ideal Bipolar Transfer Function

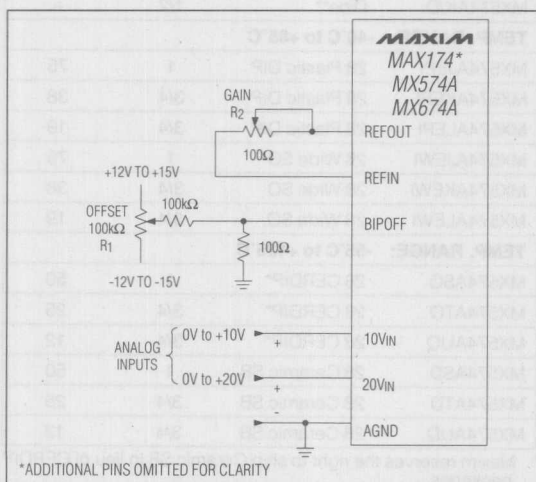


Figure 13. Unipolar Input Connections

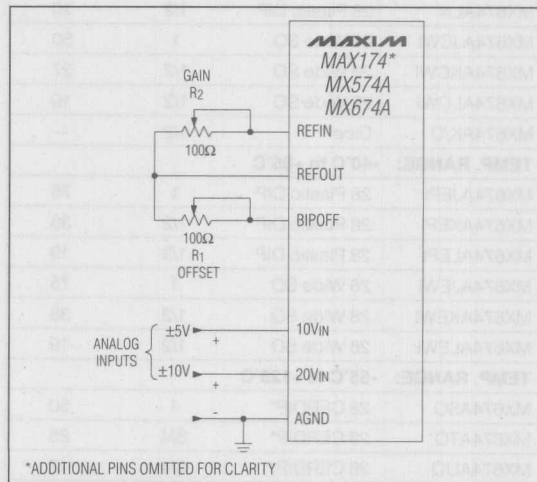


Figure 15. Bipolar Input Connections

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Bipolar Input Operation

The Bipolar transfer function is shown in Figure 14, and input connections are shown in Figure 15. One or both of the trimmers can be exchanged with a $50\Omega \pm 1\%$ fixed resistor if the offset and gain specifications suffice.

Offset and Full-Scale Adjustment

To begin bipolar calibration, a signal 1/2LSB above negative full-scale is applied. R1 is trimmed until the digital output flickers between 0000 0000 0000 and 0000 0000 0001. Next, a signal 3/2LSB below positive full scale is applied. Then, R2 is trimmed until the output flickers between 1111 1111 1110 and 1111 1111 1111.

Ordering Information (continued)

PART	PIN-PACKAGE	LINEARITY (LSBs)	TEMPCO (ppm/°C)
8μs Maximum Conversion Time			
TEMP. RANGE: -40°C to +85°C			
MAX174AEPI	28 Plastic DIP	3/4	19
MAX174BEPI	28 Plastic DIP	3/4	38
MAX174CEPI	28 Plastic DIP	1	75
MAX174AEWI	28 Wide SO	3/4	19
MAX174BEWI	28 Wide SO	3/4	38
MAX174CEWI	28 Wide SO	1	75
TEMP. RANGE: -55°C to +125°C			
MAX174AMJI	28 Cerdip	3/4	12
MAX174BMJI	28 Cerdip	3/4	25
MAX174CMJI	28 Cerdip	1	50
15μs Maximum Conversion Time			
TEMP. RANGE: 0°C to +70°C			
MX674AJN	28 Plastic DIP	1	50
MX674AKN	28 Plastic DIP	1/2	27
MX674ALN	28 Plastic DIP	1/2	10
MX674AJCWI	28 Wide SO	1	50
MX674AKCWI	28 Wide SO	1/2	27
MX674ALCWI	28 Wide SO	1/2	10
MX674AK/D	Dice**	1/2	--
TEMP. RANGE: -40°C to +85°C			
MX674AJEPI	28 Plastic DIP	1	75
MX674AKEPI	28 Plastic DIP	1/2	38
MX674ALEPI	28 Plastic DIP	1/2	19
MX674AJEWI	28 Wide SO	1	75
MX674AKEWI	28 Wide SO	1/2	38
MX674ALEWI	28 Wide SO	1/2	19
TEMP. RANGE: -55°C to +125°C			
MX674ASQ	28 Cerdip*	1	50
MX674ATQ	28 Cerdip*	3/4	25
MX674AUQ	28 Cerdip*	3/4	12

PART	PIN-PACKAGE	LINEARITY (LSBs)	TEMPCO (ppm/°C)
15μs Maximum Conversion Time			
TEMP. RANGE: -55°C to +125°C			
MX674ASD	28 Ceramic SB	1	50
MX674ATD	28 Ceramic SB	3/4	25
MX674AUD	28 Ceramic SB	3/4	12
25μs Maximum Conversion Time			
TEMP. RANGE: 0°C to +70°C			
MX574AJN	28 Plastic DIP	1	50
MX574AKN	28 Plastic DIP	1/2	27
MX574ALN	28 Plastic DIP	1/2	10
MX574AJCWI	28 Wide SO	1	50
MX574AKCWI	28 Wide SO	1/2	27
MX574ALCWI	28 Wide SO	1/2	10
MX574AJP	28 PLCC	1	50
MX574AKP	28 PLCC	1/2	27
MX574ALP	28 PLCC	1/2	10
MX574AK/D	Dice**	1/2	--
TEMP. RANGE: -40°C to +85°C			
MX574AJEPI	28 Plastic DIP	1	75
MX574AKEPI	28 Plastic DIP	3/4	38
MX574ALEPI	28 Plastic DIP	3/4	19
MX574AJEWI	28 Wide SO	1	75
MX574AKEWI	28 Wide SO	3/4	38
MX574ALEWI	28 Wide SO	3/4	19
TEMP. RANGE: -55°C to +125°C			
MX574ASQ	28 Cerdip*	1	50
MX574ATQ	28 Cerdip*	3/4	25
MX574AUQ	28 Cerdip*	3/4	12
MX574ASD	28 Ceramic SB	1	50
MX574ATD	28 Ceramic SB	3/4	25
MX574AUD	28 Ceramic SB	3/4	12

* Maxim reserves the right to ship Ceramic SB in lieu of Cerdip packages.

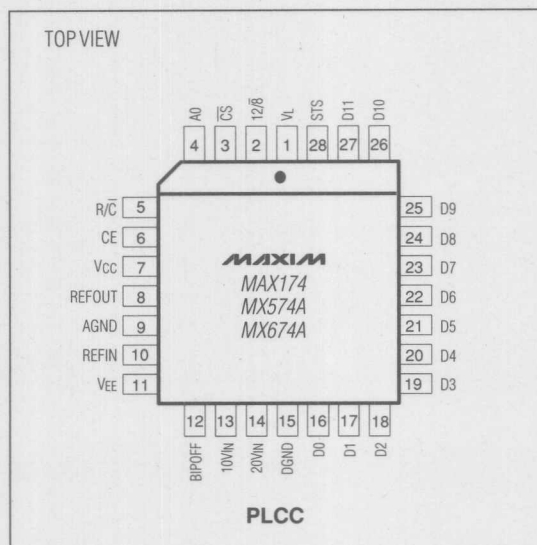
** Consult factory for dice specifications.

Industry Standard Complete 12-Bit A/D Converters

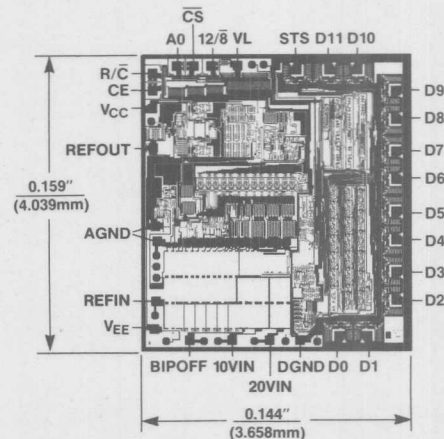
MAX174/MX574A/MX674A

1

Pin Configurations (continued)



Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

1-117

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM CMOS 10-Bit A/D Converter with Track-and-Hold

General Description

The MAX177 is a complete CMOS sampling 10-bit analog-to-digital converter (ADC) that combines an on-chip track-and-hold and voltage reference along with high conversion speed and low power consumption. A conversion time of 8.33 μ s includes settling time for the track-and-hold. An internal buried zener reference provides low drift with low noise.

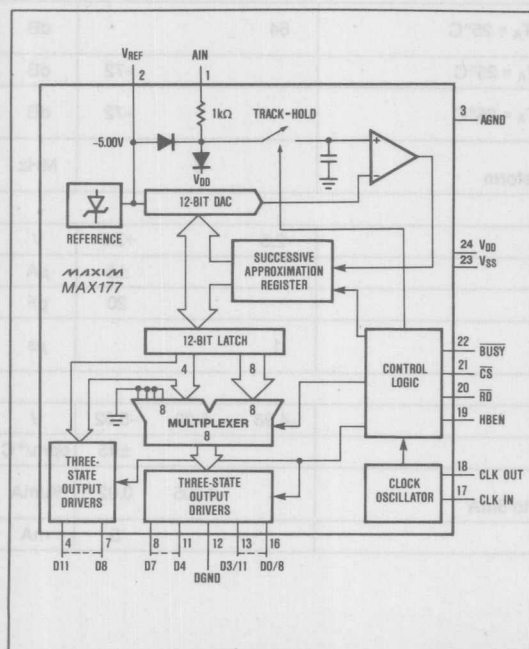
The MAX177 accepts -2.5V to +2.5V inputs. External components are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry can either be driven from an external clock source or a crystal.

The MAX177 employs a standard microprocessor interface. Three-state data outputs can be configured for 8- or 12-bit data buses. Data access and bus release timing specs are compatible with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)
Audio and Telecom Processing
High Accuracy Process Control
High Speed Data Acquisition

Functional Diagram



Features

- ◆ 12-Bit Resolution and 10-Bit Linearity
- ◆ 8.33 μ s Conversion Time
- ◆ Internal Analog Track-Hold
- ◆ 6MHz Full Power Bandwidth
- ◆ On-Chip ± 40 ppm/ $^{\circ}$ C Voltage Reference
- ◆ High Input Resistance (500M Ω)
- ◆ 100ns Data Access Time
- ◆ 180mW (Max) Power Consumption
- ◆ 24 Lead Narrow DIP and Wide SO Packages

Ordering Information

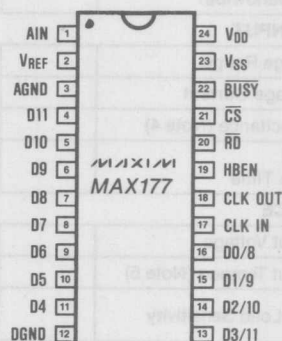
PART	TEMP. RANGE	PACKAGE*	ERROR
MAX177CNG	0 $^{\circ}$ C to +70 $^{\circ}$ C	Plastic DIP	± 1 LSB
MAX177CWG	0 $^{\circ}$ C to +70 $^{\circ}$ C	Wide SO	± 1 LSB
MAX177C/D	0 $^{\circ}$ C to +70 $^{\circ}$ C	Dice**	± 1 LSB
MAX177ENG	-40 $^{\circ}$ C to +85 $^{\circ}$ C	Plastic DIP	± 1 LSB
MAX177EWG	-40 $^{\circ}$ C to +85 $^{\circ}$ C	Wide SO	± 1 LSB
MAX177MRG	-55 $^{\circ}$ C to +125 $^{\circ}$ C	CERDIP	± 1 LSB

* All devices — 24 lead packages

** Consult factory for dice specifications.

Pin Configuration

Top View



MAXIM

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Maxim Integrated Products 1-119

MAX177

1

CMOS 10-Bit A/D Converter with Track-and-Hold

ABSOLUTE MAXIMUM RATINGS

V _{DD} to DGND	-0.3V to +7V
V _{SS} to DGND	+0.3V to -17V
AGND to DGND	-0.3V to V _{DD} + 0.3V
AIN to AGND	-15V to +15V
Digital Input Voltage to DGND (Pins 17, 19-21)	-0.3V to V _{DD} + 0.3V
Digital Output Voltage to DGND (Pins 4-11, 13-16, 18, 22)	-0.3V to V _{DD} + 0.3V

Operating Temperature Ranges

MAX177C	0°C to +70°C
MAX177E	-40°C to +85°C
MAX177M	-55°C to +125°C
Storage Temperature Range	-65°C to +160°C
Power Dissipation (any Package)	1000mW
Derates Above +75°C by	10mW/°C
Lead Temperature (Soldering 10 seconds)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode, T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.5MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
No Missing Code Resolution			10			Bits
Integral Non-Linearity	INL				0.05	%FSR
Offset Error (Note 1)					±8	mV
Full Scale Error (Note 2)		T _A = 25°C, Includes Reference Error			±0.4	%
Full Scale Tempco (Notes 3, 4)		Excludes Internal Reference Drift			±5	ppm/°C
Conversion Time	t _{CONV}	Synchronous (12.5 clock cycles) (13 clock cycles)			8.33 8.67	μs
DYNAMIC ACCURACY (V _{DD} = 5V, V _{SS} = 15V, Sample Rate = 100kHz)						
Signal to Noise and Distortion Ratio	S/(N+D)	10kHz Input Signal, T _A = 25°C	64			dB
Total Harmonic Distortion	THD	10kHz Input Signal, T _A = 25°C			-72	dB
Peak Harmonic or Spurious Noise		10kHz Input Signal, T _A = 25°C			-72	dB
Full Power Sampling Bandwidth		In Sample Mode, Under-Sampled Waveform		6		MHz
ANALOG INPUT						
Input Voltage Range			-2.5		+2.5	V
Input Leakage Current					±5	μA
Input Capacitance (Note 4)					20	pF
Track-and-Hold Acquisition Time			1			μs
REFERENCE						
V _{REF} Output Voltage		T _A = 25°C	-4.98	-5.00	-5.02	V
V _{REF} Output Tempco (Note 5)					±45	ppm/°C
Reference Load Sensitivity		ΔFS/ΔI _{REF} , I _{REF} Load Change: 0 to 5mA		0.005	0.02	%/mA
Output Sink Current					5	mA

CMOS 10-Bit A/D Converter with Track-and-Hold

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +5V \pm 5\%$, $V_{SS} = -11.4V$ to $-15.75V$, Slow Memory Mode, $T_A = T_{MIN}$ to T_{MAX} , $f_{CLK} = 1.5MHz$ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input Low Voltage	V_{IL}	\overline{CS} , \overline{RD} , \overline{HBEN} , CLK IN			0.8	V
Input High Voltage	V_{IH}	\overline{CS} , \overline{RD} , \overline{HBEN} , CLK IN	2.4			V
Input Capacitance (Note 4)	C_{IN}	\overline{CS} , \overline{RD} , \overline{HBEN} , CLK IN			10	pF
Input Current	I_{IN}	$V_{IN} = 0V$ to V_{DD} , \overline{CS} , \overline{RD} , \overline{HBEN} , CLK IN			10 20	μA
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D11-D0/8, \overline{BUSY} , CLK OUT $I_{SINK} = 1.6mA$			0.4	V
Output High Voltage	V_{OH}	D11-D0/8, \overline{BUSY} , CLK OUT $I_{SOURCE} = 200\mu A$	4			V
Three-State Leakage Current	I_L	D11-D0/8, $V_{OUT} = 0V$ to V_{DD}			± 10	μA
Three-State Output Capacitance (Note 4)	C_O				15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	$\pm 5\%$ For Specified Performance		5		V
Negative Supply Voltage	V_{SS}	$\pm 5\%$ For Specified Performance	-12		-15	V
Positive Supply Rejection		FS Change, $V_{SS} = -15V$ or $-12V$ $V_{DD} = 4.75$ to $5.25V$		± 0.01		%
Negative Supply Rejection		FS Change, $V_{DD} = 5V$ $V_{SS} = -14.24$ to $-15.75V$ $V_{SS} = -11.4$ to $-12.6V$		± 0.01		%
Positive Supply Current	I_{DD}	$\overline{CS} = \overline{RD} = V_{DD}$, $A_{IN} = 5V$		4	6	mA
Negative Supply Current	I_{SS}	$\overline{CS} = \overline{RD} = V_{DD}$, $A_{IN} = 5V$		7	10	mA
Power Dissipation		$V_{DD} = +5V$, $V_{SS} = -12V$		104	150	mW

Note 1: Typical change over temp is $\pm 1mV$.

Note 2: Ideal last code transition = FS - 1.8mV LSB, adjusted for offset.

Note 3: Full Scale Tempco = dFS/dT , where dFS is full scale change from $T_A = 25^\circ C$ to T_{MIN} or T_{MAX} .

Note 4: Guaranteed by design, not subject to test.

Note 5: V_{REF} Tempco = dV_{REF}/dT , where dV_{REF} is reference voltage change from $T_A = 25^\circ C$ to T_{MIN} to T_{MAX} .

Note 6: All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 7: This specification is 100% production tested.

Note 8: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 9: t_7 is defined as the time required for the data line to change 0.5V when loaded with the circuits of Figure 2.

For additional information on using the MAX177, please refer to MAX163/164/167 data sheet.

CMOS 10-Bit A/D Converter with Track-and-Hold

TIMING CHARACTERISTICS

($V_{DD} = +5V$, $V_{SS} = -12V$ or $-15V$, $T_A = T_{MIN}$ to T_{MAX} , Note 6, specifications in bold type are 100% tested, others are guaranteed by design, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	$T_A = 25^\circ C$			MAX177C/E		MAX177M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CS to \overline{RD} Setup Time	t_1		0			0		0		ns
\overline{RD} to BUSY Delay (Note 7)	t_2	$CL = 50pF$		80	170		220		260	ns
Data Access Time (Notes 7, 8)	t_3	$CL = 100pF$		50	100		130		150	ns
\overline{RD} Pulse Width	t_4		100			130		150		ns
CS to \overline{RD} Hold Time	t_5		0			0		0		ns
Data Setup Time After BUSY (Notes 7, 8)	t_6			40	80		105		120	ns
Bus Relinquish Time (Notes 7, 9)	t_7			30	50		65		75	ns
HBEN to \overline{RD} Setup Time	t_8			0			0		0	ns
HBEN to \overline{RD} Hold Time	t_9			0			0		0	ns
Delay Between READ Operations	t_{10}			200			200		200	ns
Delay Between Conversions	t_{11}			1			1		1	μs
Aperture Delay	t_{12}	Jitter < 50ps		25						ns

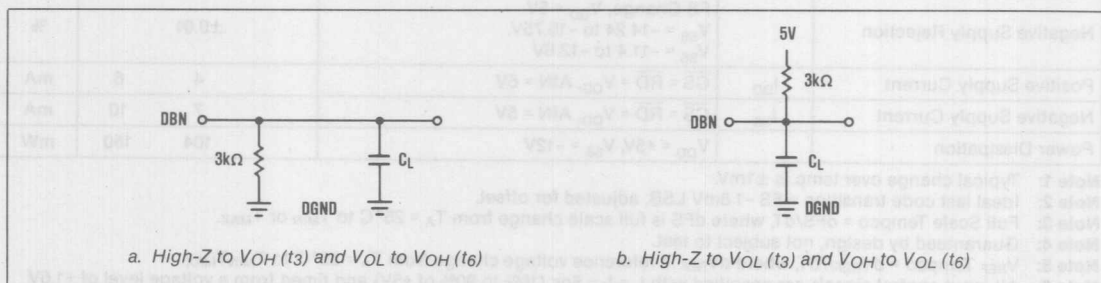


Figure 1. Load Circuits for Access Time

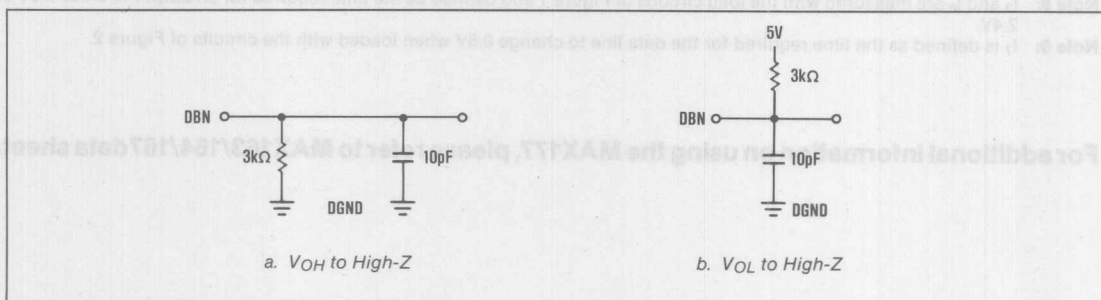


Figure 2. Load Circuits for Bus Relinquish Time

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ADVANCE INFORMATION

FIRST PAGE OF DATA SHEET IN PREPARATION

MAXIM 12-Bit A/D Converter with T/H and Reference

MAX178

General Description

The MAX178 is a 12-bit analog-to-digital converter (ADC), whose end points (offset and gain) are continuously calibrated in a transparent fashion. This calibration, along with a laser-trimmed R-2R ladder, provides true 12-bit performance without external adjustments to compensate for full-scale and zero errors. The MAX178 includes an internal reference, on-board oscillator, and Track-and-Hold (T/H) analog input. At the beginning of each conversion, an auto-zero cycle reduces system offset voltages to typically less than 100 μ V.

Designed for easy microprocessor (μ P) interfacing, the device includes decoded device address (CS), READ (RD), and WRITE (WR). The output is available in 2 bytes over an 8-bit, three-state output bus. Either byte may be read first. To facilitate polling of the converter's status, 2 converter busy flags are available.

The analog input voltage range is 0V to +5V when using a +5V reference voltage.

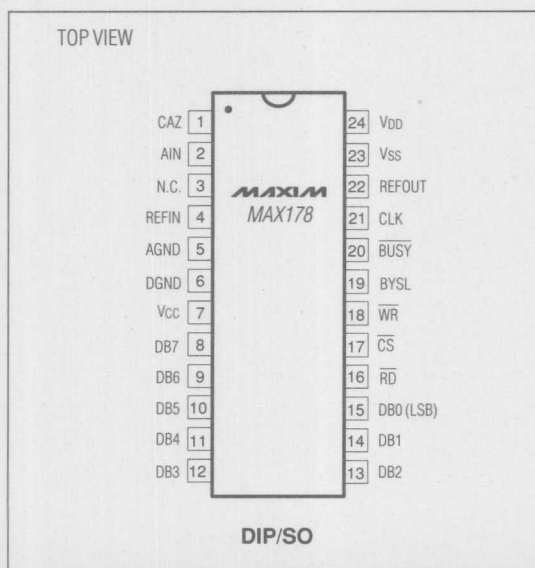
Features

- ◆ Continuous Zero and Full-Scale Error Calibration
- ◆ No External Adjustments for Specified Accuracy
- ◆ T/H Front End and Internal Reference
- ◆ DC and Dynamic Tested
- ◆ Auto-Zero Cycle: 100 μ V Zero Error
- ◆ 8- and 16-Bit μ P Interface
- ◆ Offered in 24-Pin DIP and Wide SO Packages

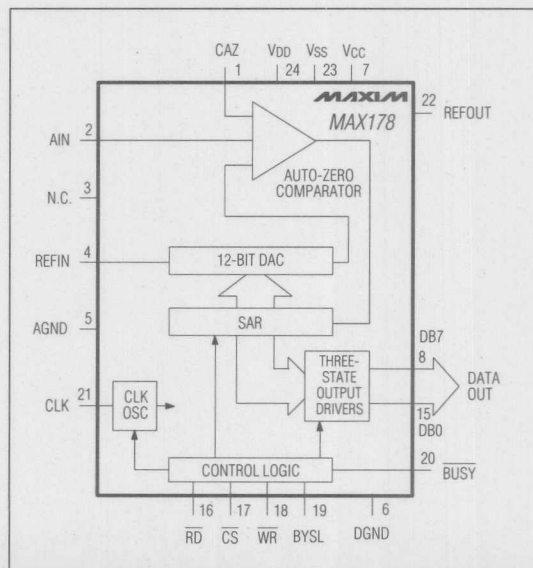
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX178ACNG	0°C to +70°C	24 Plastic DIP
MAX178BCNG	0°C to +70°C	24 Plastic DIP
MAX178ACWG	0°C to +70°C	24 Wide SO
MAX178BCWG	0°C to +70°C	24 Wide SO
MAX178AENG	-40°C to +85°C	24 Plastic DIP
MAX178BENG	-40°C to +85°C	24 Plastic DIP
MAX178AEWG	-40°C to +85°C	24 Wide SO
MAX178BEWG	-40°C to +85°C	24 Wide SO
MAX178AMRG	-55°C to +125°C	24 Cerdip
MAX178BMRG	-55°C to +125°C	24 Cerdip

Pin Configuration



Functional Diagram



MAXIM

Maxim Integrated Products 1-123

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Complete 8/6-Channel, 12-Bit Data Acquisition Systems

General Description

The MAX180/MAX181 are complete 12-bit Data Acquisition Systems (DAS) which combine 8/6-channel input multiplexer, high bandwidth Track-and-Hold (T/H), low-drift zener reference, and flexible microprocessor (μ P) interface with high conversion speed and low power consumption. The MAX180/MAX181 can be configured by a μ P for unipolar or bipolar conversions and single-ended or differential inputs. Both devices sample and digitize at 100kHz throughput rate and feature a fast 8- or 16-bit μ P interface.

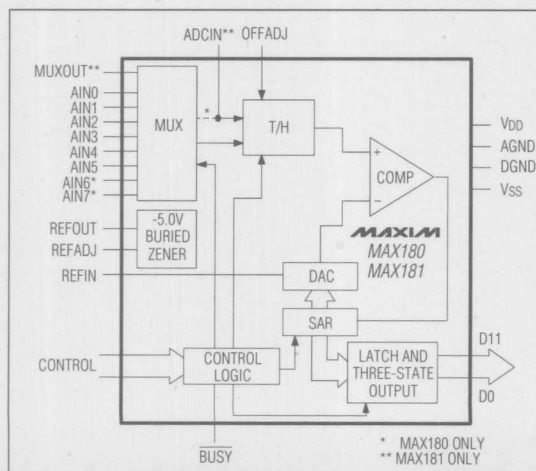
The MAX180/MAX181 differ in two respects. The MAX180 has 8 analog input channels, while the MAX181 has 6. The multiplexer output of the MAX180 is fed directly into the Analog-to-Digital Converter (ADC) input. The MAX181 brings out both the multiplexer output and ADC input to separate pins, allowing a programmable gain amplifier to be inserted between the MUX and the ADC.

The systems allow the user to choose between an internal or an external reference. Furthermore, the internal reference value and the offset can be adjusted, allowing the overall system gain and offset errors to be nulled. The multiplexer has high impedance inputs, simplifying analog drive requirements.

Applications

Digital Signal Processing (DSP)
High-Accuracy Process Control
Electro-Mechanical Systems
Automatic Testing Systems

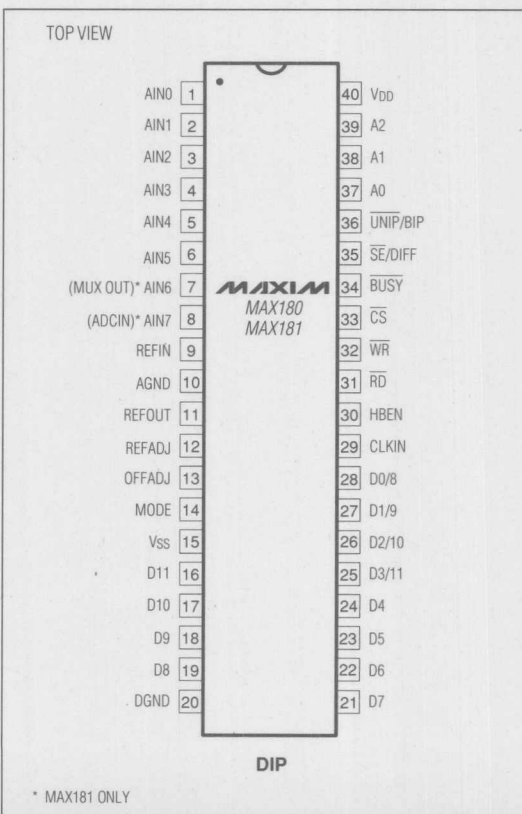
Block Diagram



Features

- ◆ Built-In Track-and-Hold
- ◆ 100kHz Sampling Rate
- ◆ Internal 25ppm/°C Buried Zener Reference
- ◆ 8/6-Channel Multiplexed Inputs
- ◆ Configurable for Unipolar (0V to 5V) or Bipolar (-2.5V to +2.5V) Input Range for each Input Channel
- ◆ Each Channel Configurable for Single-Ended or Differential Inputs
- ◆ +5V/-12V or -15V Dual-Supply Operation with 150mW Power Dissipation
- ◆ 8- or 16-Bit Fast μ P Interface
- ◆ DC and Dynamic Tested

Pin Configuration



MAX180/MAX181

1

4-Channel 12-Bit A/D Converter with T/H and Reference

MAX182

General Description

The MAX182 is a 4-channel, 12-bit analog-to-digital converter (ADC), whose end points (offset and gain) are continuously calibrated in a transparent fashion. This calibration, along with a laser-trimmed R-2R ladder, provides true 12-bit performance without external adjustments to compensate for full-scale and offset errors. The MAX182 includes an internal reference, on-board oscillator, and Track-and-Hold (T/H) analog input. At the beginning of each conversion, an auto-zero cycle reduces system offset voltages to typically less than 100mV.

Designed for easy microprocessor (μ P) interfacing, the device includes decoded device address (CS), READ (RD), and WRITE (WR). The output is available in 2 bytes over an 8-bit, three-state output bus. Either byte may be read first. To facilitate polling of the converter's status, 2 converter busy flags are available. Address inputs A0 and A1 control the 4-channel input multiplexer.

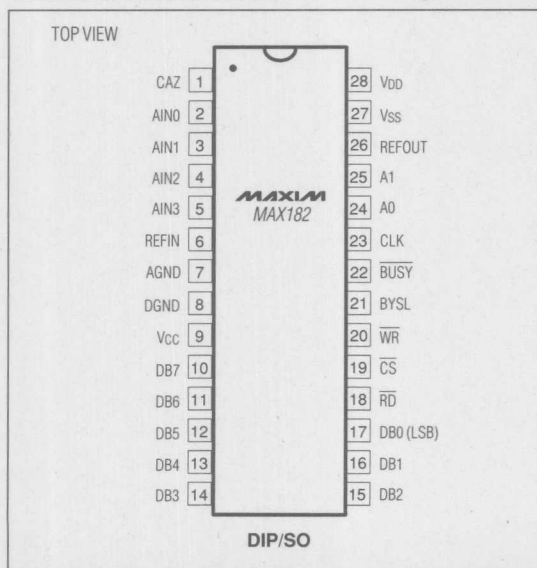
The analog input voltage range is 0V to 5V when using a +5V reference voltage. All 4 analog inputs are high impedance and have excellent channel-to-channel matching (typically 0.05LSB).

Features

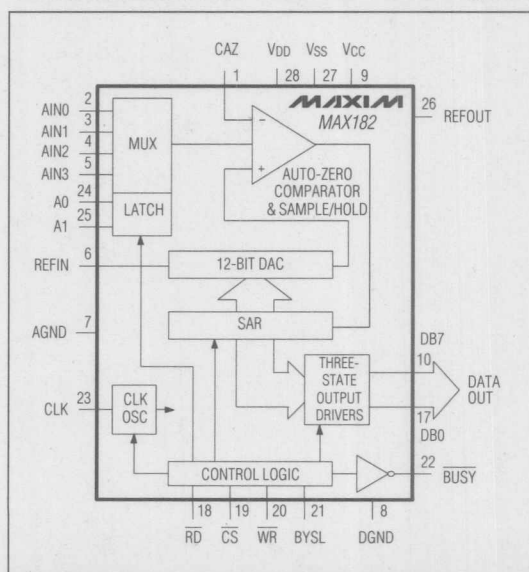
- ◆ Continuous Zero and Full-Scale Error Calibration
- ◆ No External Adjustments for Specified Accuracy
- ◆ T/H Front End and Internal Reference
- ◆ 4-Channel input MUX
- ◆ Auto-Zero Cycle: 100 μ V Zero Error
- ◆ DC and Dynamic Tested
- ◆ 8- and 16-Bit μ P Interface
- ◆ Offered in 28-Pin DIP and Wide SO Packages

1

Pin Configuration



Functional Diagram



MAXIM

High-Speed A/D Converters

MAX183/184/185

1

General Description

The MAX183/184/185 are high-speed BiCMOS A/D Converters (ADCs) with conversion times as short as 3 μ s while consuming only 110mW power. All three parts perform identically except for their conversion times: MAX183 - 3 μ s, MAX184 - 5 μ s, and MAX185 - 10 μ s.

The MAX183/184/185 work with an external voltage reference so that the optimum reference can be chosen for each application. An on-chip reference input buffer allows one system reference to drive multiple ADCs. In applications where absolute accuracy and temperature coefficients are not critical, a low-cost reference will suffice. If precision over a wide temperature range is required, a high-stability reference should be used.

For precise conversion times, an internal clock circuit can be used with a crystal. Otherwise, the clock input can be driven from an external source, such as a microprocessor (μ P) clock.

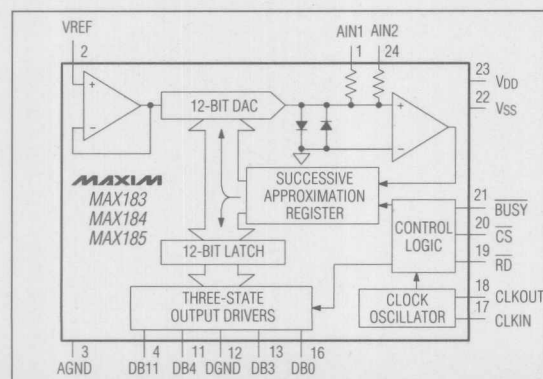
The MAX183/184/185 operate from +5V and -12V or -15V supplies. Input ranges can be selected for 0V to +5V, 0V to +10V, and \pm 5V, making them ideal for personal computer data acquisition cards. A high-speed digital interface (90ns bus interface time), with three-state data outputs and standard control inputs, is compatible with all common μ Ps.

The MAX183/184/185 are available in space saving 24-pin narrow plastic DIP, CERDIP, and wide SO packages.

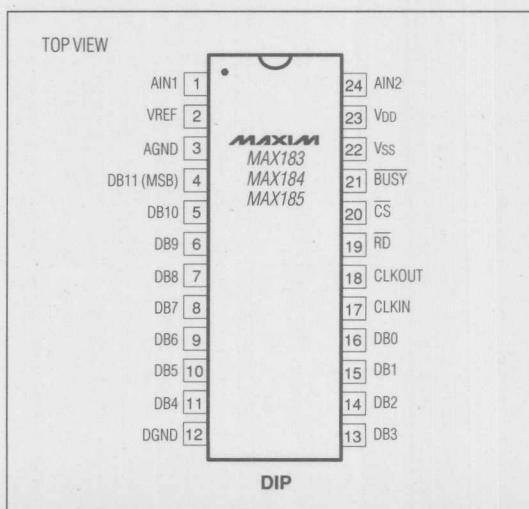
Applications

Telecommunications
Sonar and Radar Signal Processing
High-Speed Data Acquisition Systems
Personal Computer I/O Boards

Functional Diagram



Pin Configurations



MAXIM

Maxim Integrated Products 1-129

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D/A Converters

MAX500	CMOS Quad, Serial Interface, 8-Bit D/A Converter	2-1
MAX543	CMOS 12-Bit Serial Multiplying D/A Converter	2-13

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

CMOS Quad, Serial Interface, 8-Bit D/A Converter

MAX500

General Description

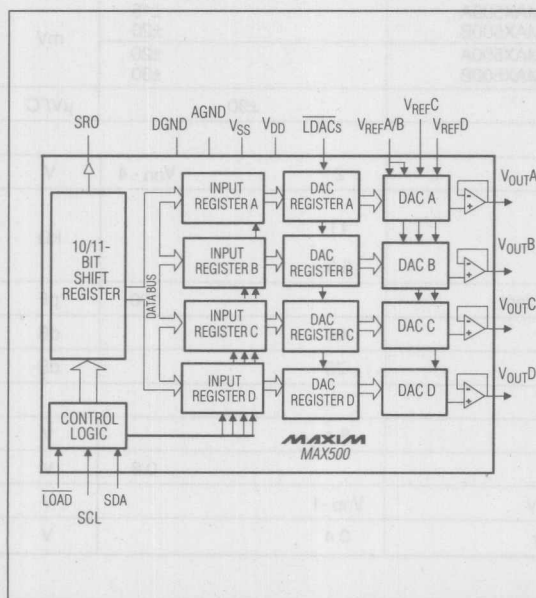
MAX500 is a quad 8-bit voltage output digital to analog converter (DAC) with a cascadable serial interface. The MAX500 circuit includes four output buffer amplifiers and input logic for an easy-to-use two- or three-wire serial interface. In a system with several MAX500s, only one serial data line is required to load all the DACs by cascading them. The MAX500 contains double-buffered logic and a 10-bit shift register which allows all four DACs to be updated simultaneously using one control signal. There are three reference inputs so that the range of two of the DACs can be independently set while the other two DACs track each other.

The MAX500 achieves 8-bit performance over the full operating temperature ranges without external trimming.

Applications

Minimum Component Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment

Functional Block Diagram



Features

- ◆ Buffered Voltage Outputs
- ◆ Double-Buffered Digital Inputs
- ◆ Microprocessor and TTL/CMOS Compatible
- ◆ Requires No External Adjustments
- ◆ Two- or Three-Wire Cascadable Serial Interface
- ◆ 16-Pin Package
- ◆ Operates from Single or Dual Supplies

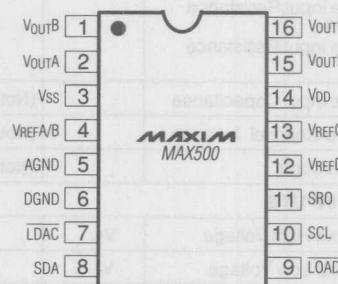
Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
MAX500ACPE	0°C to +70°C	Plastic DIP	±1 LSB
MAX500BCPE	0°C to +70°C	Plastic DIP	±2 LSB
MAX500ACWE	0°C to +70°C	Wide SO	±1 LSB
MAX500BCWE	0°C to +70°C	Wide SO	±2 LSB
MAX500BC/D	0°C to +70°C	Dice	±2 LSB
MAX500AEWE	-40°C to +85°C	Wide SO	±1 LSB
MAX500BEWE	-40°C to +85°C	Wide SO	±2 LSB
MAX500AEJE	-40°C to +85°C	CERDIP	±1 LSB
MAX500BEJE	-40°C to +85°C	CERDIP	±2 LSB
MAX500AMJE	-55°C to +125°C	CERDIP	±1 LSB
MAX500BMJE	-55°C to +125°C	CERDIP	±2 LSB

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Pin Configuration

Top View



MAXIM

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CMOS Quad, Serial Interface, 8-Bit D/A Converter

MAX500

ABSOLUTE MAXIMUM RATINGS

V _{DD} to AGND	-0.3V, +17V
V _{DD} to DGND	-0.3V, +17V
V _{SS} to DGND	-7V, V _{DD} +0.3V
V _{DD} to V _{SS}	-0.3V, +24V
Digital Input Voltage to DGND	-0.3V, V _{DD} +0.3V
V _{REF} to AGND	-0.3V, V _{DD} +0.3V
V _{OUT} to AGND (Note 1)	-0.3V, V _{DD} +0.3V

Power Dissipation (any package) to +75°C	500mW
Derate Above +75°C	.8mW/°C
Operating Temperature Range	
MAX500XC	0°C to +70°C
MAX500XE	-40°C to +85°C
MAX500XM	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering 10 sec.)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: Dual Supply Specifications

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V), T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V _{DD} = 15V ±5% V _{REF} = 10V	MAX500A MAX500B			±1 ±2	LSB
Relative Accuracy		MAX500A MAX500B				±½ ±1	LSB
Differential Nonlinearity Guaranteed Monotonic						±1	LSB
Full Scale Error		MAX500A MAX500B				±½ ±1	LSB
Full Scale Tempco		V _{REF} = 10V			±5		ppm/°C
Zero Code Error		T _A = 25°C	MAX500A MAX500B			±15 ±20	mV
		T _A = T _{MIN} to T _{MAX}	MAX500A MAX500B			±20 ±30	
Zero Code Tempco					±30		µV/°C
REFERENCE INPUT							
Reference Input Range				2		V _{DD} - 4	V
Reference Input Resistance Pins 12, 13				11			kΩ
Reference Input Resistance Pin 4				5.5			
Reference Input Capacitance		(Note 2) Code Dependent				100	pF
Channel-to-Channel Isolation		(Note 3)		-60			dB
AC Feedthrough		(Note 3)		-70			dB
DIGITAL INPUTS							
Digital Input High Voltage	V _{IH}			2.4			V
Digital Input Low Voltage	V _{IL}					0.8	V
Digital Output High Voltage	V _{OH}	I _{OUT} = -1mA, SRO only		V _{DD} - 1			V
Digital Output Low Voltage	V _{OL}	I _{OUT} = 1mA, SRO only		0.4			V

CMOS Quad, Serial Interface, 8-Bit D/A Converter

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ELECTRICAL CHARACTERISTICS: Dual Supply Specifications (continued)

($V_{DD} = +11.4V$ to $+16.5V$, $V_{SS} = -5V \pm 10\%$, $AGND = DGND = 0V$, $V_{REF} = +2V$ to $(V_{DD} - 4V)$, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Leakage Current		(Note 4) Excluding LOAD LOAD = 0V			± 1 30	μA
Digital Input Capacitance		(Note 5)			8	pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate		(Note 5)	3			V/ μs
V_{OUT} Settling Time		To $\pm 1/2$ LSB, $V_{REF} = 10V$, $V_{DD} = +15V$, 2k Ω in parallel with 100pF load			4	μs
Digital Feedthrough		(Note 6)		50		nV-s
Digital Crosstalk		(Note 6)		50		nV-s
Output Load Resistance		$V_{OUT} = 10V$	2			k Ω
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	For specified performance	11.4		16.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, $T_A = 25^\circ C$ $T_A = T_{MIN}$ to T_{MAX}			10 12	mA
Negative Supply Current	I_{SS}	Outputs unloaded, $T_A = 25^\circ C$ $T_A = T_{MIN}$ to T_{MAX}			-9 -10	mA
SWITCHING CHARACTERISTICS (Note 5)						
THREE-WIRE MODE						
SDA Valid to SCL Setup	t_{S1}		150			ns
SDA Valid to SCL Hold	t_H		0			ns
SCL High Time	t_1		350			ns
SCL Low Time	t_2		350			ns
LOAD Pulse Width	t_{LDW}		150			ns
LOAD Delay from SCL	t_{LDS}		150			ns
LDAC Pulse Width	t_{LDAC}		150			ns
SRO Output Delay	t_{D1}	$C_{LOAD} = 50pF$			150	ns
TWO-WIRE MODE						
SDA Valid to SCL Hold	t_H		0			ns
SCL High Time	t_1		350			ns
SCL Low Time	t_2		350			ns
LDAC Pulse Width	t_{LDAC}		150			ns
SCL Valid to SDA Setup	t_{S1}	(Start condition)	150			ns
SDA Valid to SCL Setup	t_{S2}	(Stop condition)	100			ns
SDA Valid to Rising SCL	t_{S3}		125			ns
SRO Output Delay	t_{D1}	$C_{LOAD} = 50pF$			150	ns

8-Bit D/A Converter

ELECTRICAL CHARACTERISTICS: Single Supply Specifications

($V_{DD} = +15V \pm 5\%$, $V_{SS} = AGND = DGND = 0V$, $V_{REF} = 10V$, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution			8			Bits
Total Unadjusted Error		$V_{DD} = 15V \pm 5\%$ $V_{REF} = 10V$			± 1 ± 2	LSB
Relative Accuracy		MAX500A MAX500B			$\pm 1/2$ ± 1	LSB
Differential Nonlinearity Guaranteed Monotonic					± 1	LSB
Full Scale Error		MAX500A MAX500B			$\pm 1/2$ ± 1	LSB
Full Scale Tempco		$V_{REF} = 10V$		± 5		ppm/ $^{\circ}C$
Zero Code Error		$T_A = 25^{\circ}C$	MAX500A MAX500B		± 15 ± 20	mV
		$T_A = T_{MIN}$ to T_{MAX}	MAX500A MAX500B		± 20 ± 30	
Zero Code Tempco				± 30		$\mu V/^{\circ}C$
REFERENCE INPUT – All specifications are the same as for dual supplies.						
DIGITAL INPUTS – All specifications are the same as for dual supplies.						
DYNAMIC PERFORMANCE – All specifications are the same as for dual supplies.						
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	For specified performance	14.25		15.75	V
Positive Supply Current	I_{DD}	Outputs Unloaded $T_A = 25^{\circ}C$ $T_A = T_{MIN}$ to T_{MAX}			10 12	mA
SWITCHING CHARACTERISTICS – All specifications are the same as for dual supplies.						

Note 1: The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded.

Typical short circuit current to AGND is 25mA.

Note 2: Guaranteed by design. Not production tested.

Note 3: $V_{REF} = 10$ kHz, 10V peak-to-peak sine wave.

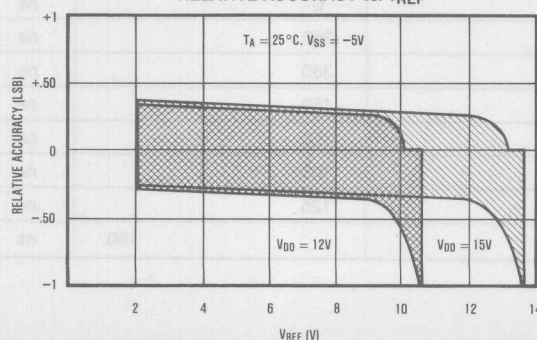
Note 4: LOAD has a weak internal pull-up resistor to V_{DD} .

Note 5: Sample tested at $+25^{\circ}C$ to ensure compliance.

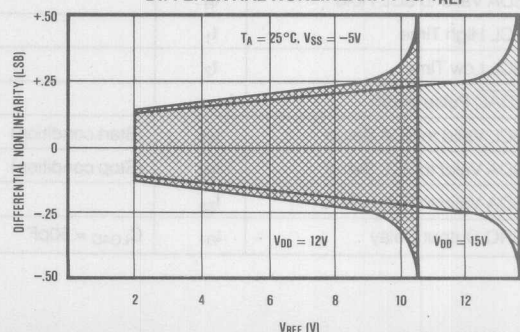
Note 6: DAC switched from all 1s to all 0s, and all 0s to all 1s code.

Typical Operating Characteristics

RELATIVE ACCURACY vs. V_{REF}

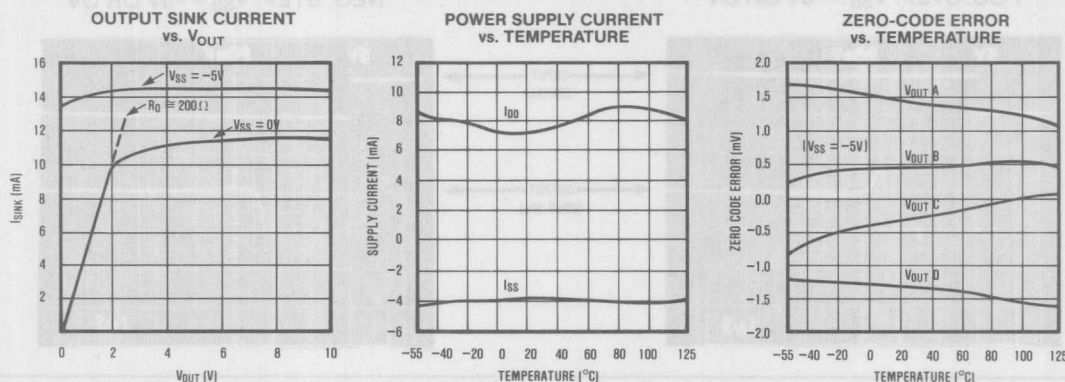


DIFFERENTIAL NONLINEARITY vs. V_{REF}



CMOS Quad, Serial Interface, 8-Bit D/A Converter

Typical Operating Characteristics (Continued)



Detailed Description

The MAX500 has four matched voltage output digital-to-analog converters (DAC). The DACs are "inverted" R-2R ladder networks which convert 8 digital bits into equivalent analog output voltages in proportion to the applied reference voltage(s). Two DACs in the MAX500 have a separate reference input while the other two DACs share one reference input. A simplified circuit diagram of one of the four DACs is provided in Figure 1.

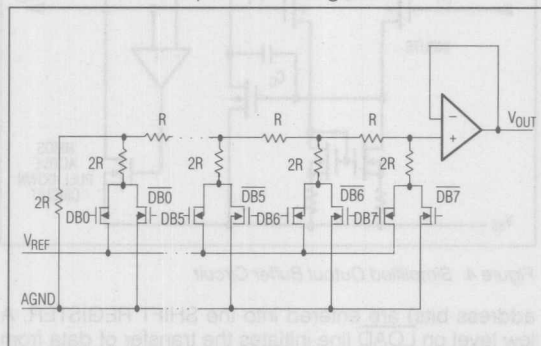


Figure 1. Simplified DAC Circuit Diagram

V_{REF} Input

The voltage at V_{REF} pins (pins 4, 12 and 13) sets the full scale output of the DAC. The input impedance of the V_{REF} inputs is code dependent. The lowest value, approximately $11k\Omega$ ($5.5k\Omega$ for pin 4), occurs when the input code is 01010101. The maximum value of infinity occurs when the input code is 00000000. Because the input resistance at V_{REF} is code dependent, the DAC's reference sources should have an output impedance of no more than 20Ω (no more than 10Ω for pin 4). The input capacitance at V_{REF} is also code dependent and typically varies from 15pF to 35pF (30pF to 70pF for pin 4).

V_{OUTA} , V_{OUTB} , V_{OUTC} , and V_{OUTD} can be represented by a digitally programmable voltage source as:

$$V_{OUT} = N_b \times \frac{V_{REF}}{256}$$

where N_b is the numeric value of the DAC's binary input code.

Output Buffer Amplifiers

All voltage outputs are internally buffered by precision unity gain followers which slew at greater than $3V/\mu s$. When driving $2k\Omega$ in parallel with $100pF$ with a full scale transition (0V to +10V or +10V to 0V), the output settles to $\pm 1/2$ LSB in less than $4\mu s$. The buffers will also drive $2k\Omega$ in parallel with $500pF$ to 10V levels without oscillation. Typical dynamic response and settling performance of the MAX500 is shown in Figures 2 and 3.

A simplified circuit diagram of an output buffer is shown in Figure 4. Input common mode range to AGND is provided by a PMOS input structure. The output circuitry incorporates a pull-down circuit to actively drive V_{OUT} to within +15mV of the negative supply (V_{SS}). The buffer circuitry allows each DAC output to sink, as well as source up to 5mA. This is especially important in single supply applications, where V_{SS} is connected to AGND, so that the zero error is kept at or under $1/2$ LSB ($V_{REF} = +10V$). A plot of the output sink current versus output voltage is shown in the Typical Operating Characteristics section.

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic, however, the power supply current (I_{DD}) is somewhat dependent on the input logic level. Supply current is specified for TTL input levels (worst case) but is reduced (by about $150\mu A$) when the logic inputs are driven near DGND or 4 volts above DGND.

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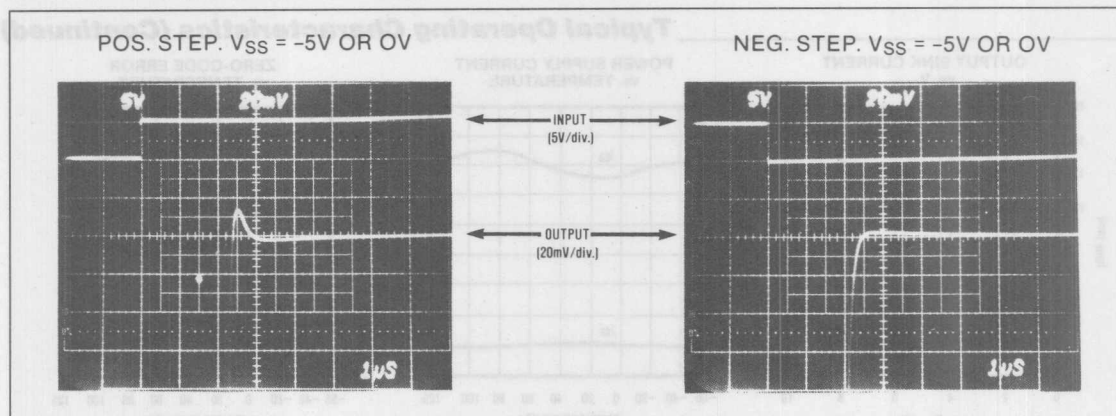


Figure 2. Positive and Negative Settling Times, $V_{SS} = 0V$ or $-5V$

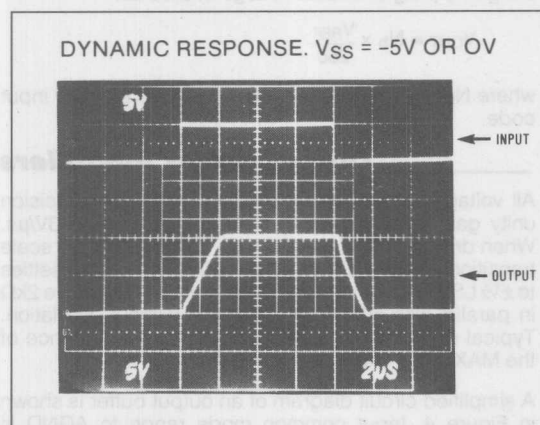


Figure 3. Dynamic Response, $V_{SS} = 0V$ or $-5V$

The MAX500 allows the user to choose between a three-wire serial interface and a two-wire serial interface. The choice between the two-wire and the three-wire interface is set by the LOAD signal. If the LOAD is allowed to float (it has a weak internal pull-up resistor to V_{DD}), the two-wire interface is selected. If the LOAD signal is kept to a TTL logical high level, the three-wire interface is selected.

Three-Wire Interface

The three-wire interface uses the classic Serial Data (SDA), Serial Clock (SCL), and LOAD signals used in standard shift registers. The data is clocked in on the falling edge of SCL until all 10 bits (8 data bits and 2

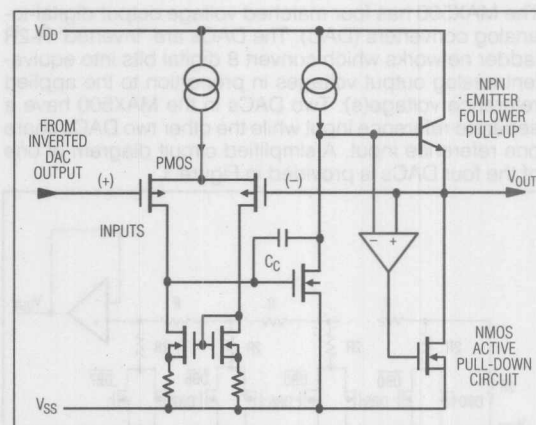


Figure 4. Simplified Output Buffer Circuit

address bits) are entered into the SHIFT REGISTER. A low level on LOAD line initiates the transfer of data from the SHIFT REGISTER to the addressed INPUT REGISTER. The data can stay in this register until all four of the INPUT REGISTERS are updated. Then all of the DAC REGISTERS can be simultaneously updated using the LDAC (LOAD DAC) signal. When LDAC is low, the INPUT REGISTER's data is loaded into the DAC REGISTERS (see Figure 5 for timing diagram). This mode is cascadable by connecting Serial Output (SRO) to the second chip's SDA pin. The delay of the SRO pin from SCL does not cause setup/hold time violations no matter how many MAX500s are cascaded.

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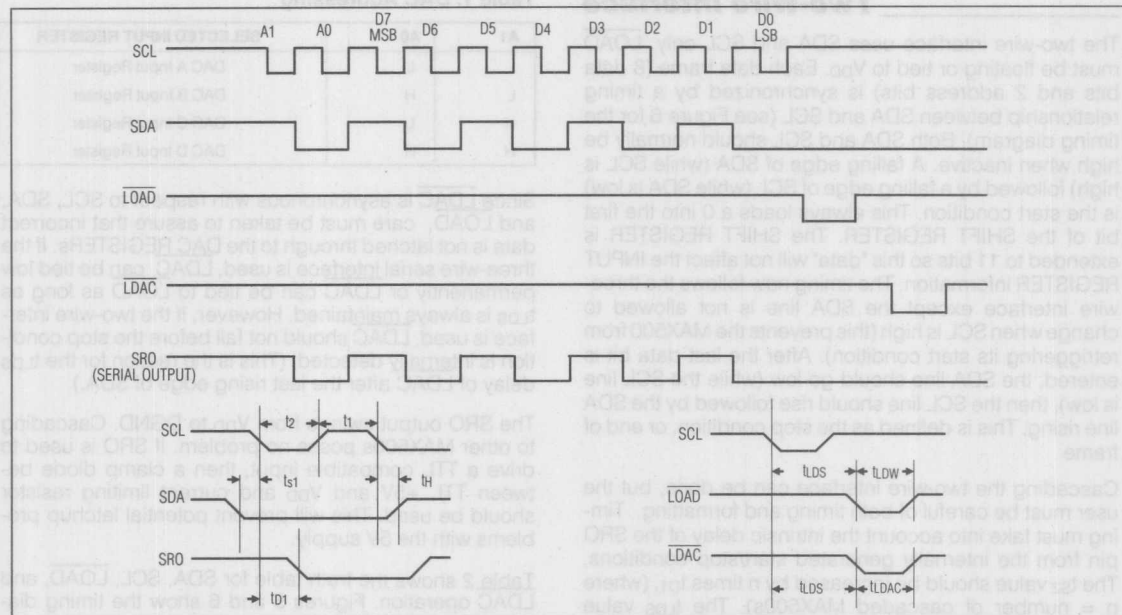


Figure 5. 3-Wire Mode

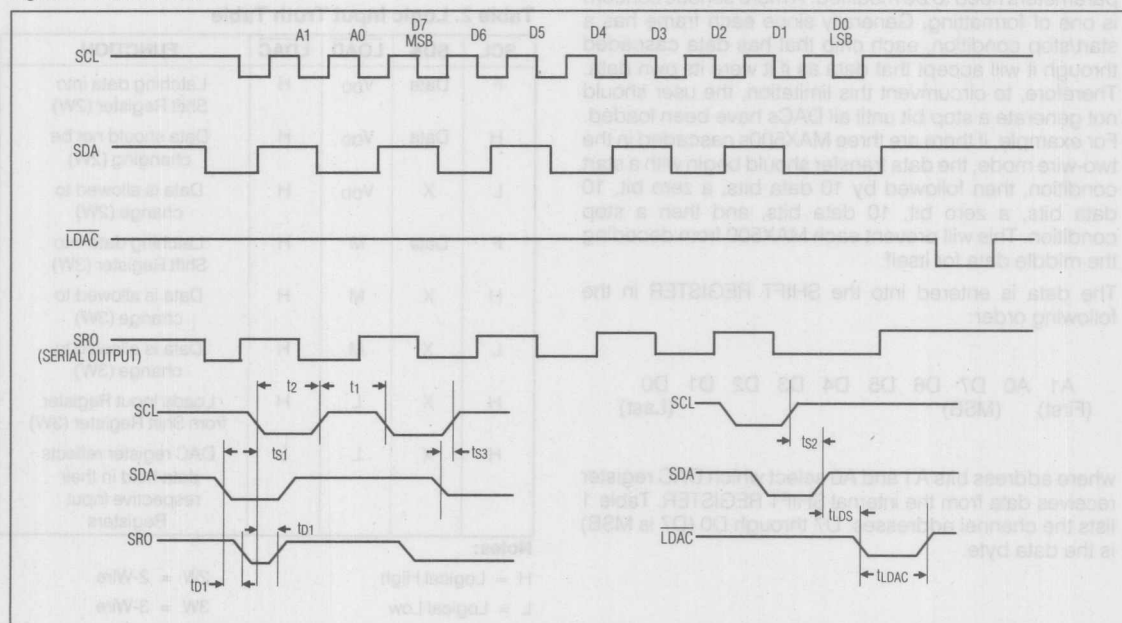


Figure 6. 2-Wire Mode

8-Bit D/A Converter

Two-Wire Interface

The two-wire interface uses SDA and SCL only. $\overline{\text{LOAD}}$ must be floating or tied to V_{DD} . Each data frame (8 data bits and 2 address bits) is synchronized by a timing relationship between SDA and SCL (see Figure 6 for the timing diagram). Both SDA and SCL should normally be high when inactive. A falling edge of SDA (while SCL is high) followed by a falling edge of SCL (while SDA is low) is the start condition. This always loads a 0 into the first bit of the SHIFT REGISTER. The SHIFT REGISTER is extended to 11 bits so this "data" will not affect the INPUT REGISTER information. The timing now follows the three-wire interface except the SDA line is not allowed to change when SCL is high (this prevents the MAX500 from retriggering its start condition). After the last data bit is entered, the SDA line should go low (while the SCL line is low), then the SCL line should rise followed by the SDA line rising. This is defined as the stop condition, or end of frame.

Cascading the two-wire interface can be done, but the user must be careful of both timing and formatting. Timing must take into account the intrinsic delay of the SRO pin from the internally generated start/stop conditions. The t_{S2} value should be increased by n times t_{D1} , (where n = number of cascaded MAX500s). The t_{LDS} value should also be increased by n times t_{D1} . No other timing parameters need to be modified. A more serious concern is one of formatting. Generally since each frame has a start/stop condition, each chip that has data cascaded through it will accept that data as if it were its own data. Therefore, to circumvent this limitation, the user should not generate a stop bit until all DACs have been loaded. For example, if there are three MAX500s cascaded in the two-wire mode, the data transfer should begin with a start condition, then followed by 10 data bits, a zero bit, 10 data bits, a zero bit, 10 data bits, and then a stop condition. This will prevent each MAX500 from decoding the middle data for itself.

The data is entered into the SHIFT REGISTER in the following order:

A1 A0 D7 D6 D5 D4 D3 D2 D1 D0
(First) (MSB) (Last)

where address bits A1 and A0 select which DAC register receives data from the internal SHIFT REGISTER. Table 1 lists the channel addresses. D7 through D0 (D7 is MSB) is the data byte.

Table 1. DAC Addressing

A1	A0	SELECTED INPUT REGISTER
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Since $\overline{\text{LDAC}}$ is asynchronous with respect to SCL, SDA, and $\overline{\text{LOAD}}$, care must be taken to assure that incorrect data is not latched through to the DAC REGISTERS. If the three-wire serial interface is used, $\overline{\text{LDAC}}$ can be tied low permanently or $\overline{\text{LDAC}}$ can be tied to $\overline{\text{LOAD}}$ as long as t_{LDS} is always maintained. However, if the two-wire interface is used, $\overline{\text{LDAC}}$ should not fall before the stop condition is internally detected. (This is the reason for the t_{LDS} delay of $\overline{\text{LDAC}}$ after the last rising edge of SDA.)

The SRO output swings from V_{DD} to DGND. Cascading to other MAX500s poses no problem. If SRO is used to drive a TTL compatible input, then a clamp diode between TTL +5V and V_{DD} and current limiting resistor should be used. This will prevent potential latchup problems with the 5V supply.

Table 2 shows the truth table for SDA, SCL, $\overline{\text{LOAD}}$, and $\overline{\text{LDAC}}$ operation. Figures 5 and 6 show the timing diagrams for the MAX500.

Table 2. Logic Input Truth Table

SCL	SDA	LOAD	LDAC	FUNCTION
F	Data	V_{DD}	H	Latching data into Shift Register (2W)
H	Data	V_{DD}	H	Data should not be changing (2W)
L	X	V_{DD}	H	Data is allowed to change (2W)
F	Data	M	H	Latching data into Shift Register (3W)
H	X	M	H	Data is allowed to change (3W)
L	X	M	H	Data is allowed to change (3W)
H	X	L	H	Loads Input Register from Shift Register (3W)
H	X	L	L	DAC register reflects data held in their respective Input Registers

Notes:

H = Logical High

L = Logical Low

M = TTL Logical High

X = Don't Care

2W = 2-Wire

3W = 3-Wire

F = Falling Edge

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Applications Information

Power Supply and Reference Operating Ranges

The MAX500 is fully specified to operate with V_{DD} between $+12V \pm 5\%$ and $+15V \pm 10\%$ ($+11.4V$ to $+16.5V$), and with V_{SS} from $0V$ to $-5.5V$. 8-bit performance is also guaranteed for single supply operation ($V_{SS} = 0V$), however, zero code error is reduced when V_{SS} is $-5V$ (see Output Buffer Amplifier section).

For adequate DAC and buffer operating range, the V_{REF} voltage must always be at least $4V$ below V_{DD} . The MAX500 is specified to operate with a reference input range of $+2V$ to $V_{DD} - 4V$.

Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (1N914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between DAC outputs, the reference input(s), and the digital inputs. This is particularly important if the reference is driven from an AC source. Figure 7 shows suggested circuit board layouts for minimizing crosstalk.

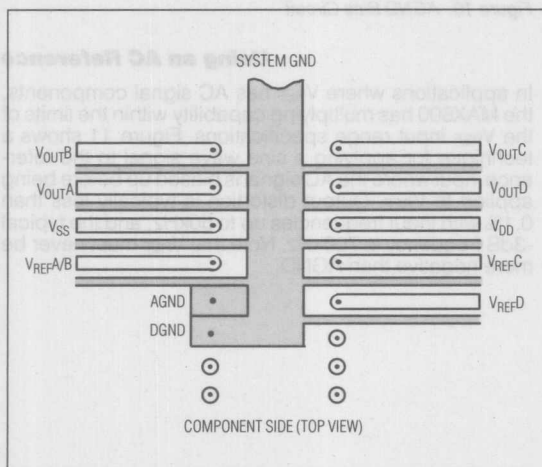


Figure 7. Suggested MAX500 PCB Layout for Minimizing Crosstalk

Unipolar Output

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Unipolar circuit configuration is shown in Figure 8 for the MAX500. The device can be operated from a single supply with a slight increase in zero error (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at V_{REF} must always be positive with respect to AGND. The unipolar code table is given in Table 3.

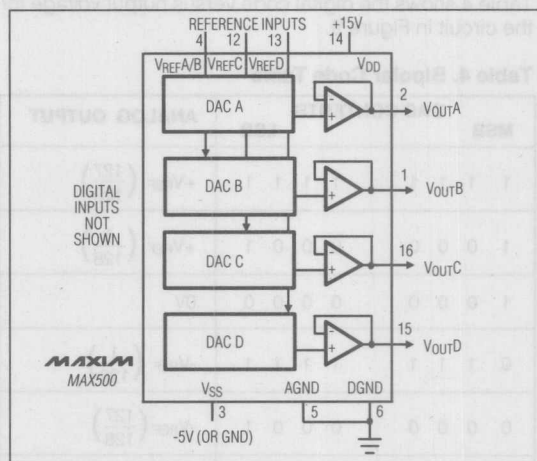


Figure 8. MAX500 Unipolar Output Circuit

Table 3. Unipolar Code Table

DAC CONTENTS		ANALOG OUTPUT
MSB	LSB	
1 1 1 1	1 1 1 1	$+V_{REF} \left(\frac{255}{256} \right)$
1 0 0 0	0 0 0 1	$+V_{REF} \left(\frac{129}{256} \right)$
1 0 0 0	0 0 0 0	$+V_{REF} \left(\frac{128}{256} \right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF} \left(\frac{127}{256} \right)$
0 0 0 0	0 0 0 1	$+V_{REF} \left(\frac{1}{256} \right)$
0 0 0 0	0 0 0 0	0V

Note: $1 \text{ LSB} = (V_{REF}) (2^{-8}) = +V_{REF} \left(\frac{1}{256} \right)$

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Bipolar Output

Each DAC output may be configured for bipolar operation using the circuit in Figure 9. One op-amp and two resistors are required per channel. With $R_1 = R_2$:

$$V_{OUT} = V_{REF} (2D_A - 1)$$

where D_A is a fractional representation of the digital word in Register A.

Table 4 shows the digital code versus output voltage for the circuit in Figure 9.

Table 4. Bipolar Code Table

MSB	DAC CONTENTS				LSB	ANALOG OUTPUT
1	1	1	1	1	1 1 1 1	$+V_{REF} \left(\frac{127}{128} \right)$
1	0	0	0	0	0 0 0 1	$+V_{REF} \left(\frac{1}{128} \right)$
1	0	0	0	0	0 0 0 0	0V
0	1	1	1	1	1 1 1 1	$-V_{REF} \left(\frac{1}{128} \right)$
0	0	0	0	0	0 0 0 1	$-V_{REF} \left(\frac{127}{128} \right)$
0	0	0	0	0	0 0 0 0	$-V_{REF} \left(\frac{128}{128} \right) = -V_{REF}$

Note: 1 LSB = $(V_{REF}) (2^{-8}) = +V_{REF} \left(\frac{1}{256} \right)$

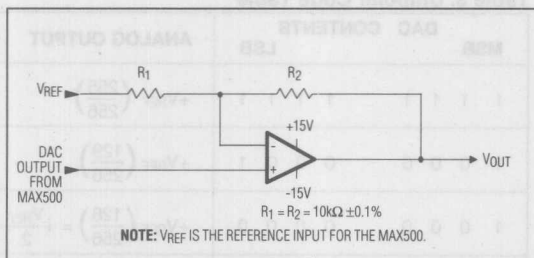


Figure 9. Bipolar Output Circuit

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a "zero" input code. This is shown in Figure 10. The output voltage at V_{OUTA} is:

$$V_{OUTA} = V_{BIAS} + D_A V_{IN}$$

where D_A is a fractional representation of the digital input word. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Since AGND current is a function of the 4 DAC codes, it should be driven by a low impedance source. V_{BIAS} must be positive.

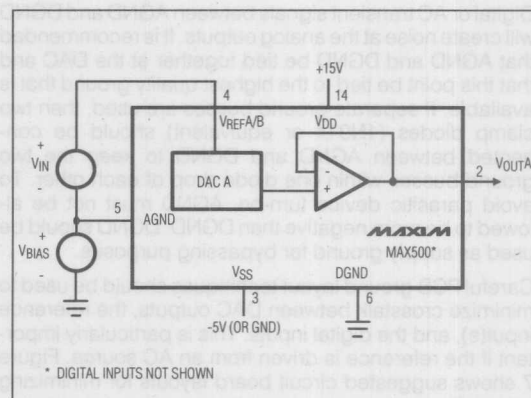


Figure 10. AGND Bias Circuit

Using an AC Reference

In applications where V_{REF} has AC signal components, the MAX500 has multiplying capability within the limits of the V_{REF} input range specifications. Figure 11 shows a technique for applying a sine wave signal to the reference input where the AC signal is biased up before being applied to V_{REF} . Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that V_{REF} must never be more negative than AGND.

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Generating V_{SS}

The performance of the MAX500 is specified for both dual and single supply ($V_{SS} = 0V$) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a $-5V$ V_{SS} supply can be generated using an ICL7660 in one of the circuits of Figure 12.

Digital Interface Applications

Figures 13 through 16 show examples of interfacing the MAX500 to most popular microprocessors.

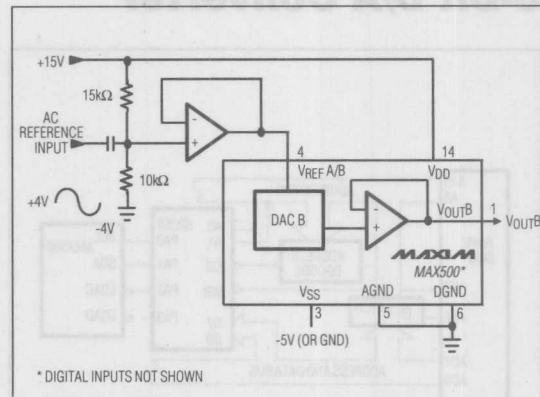


Figure 11. AC Reference Input Circuit

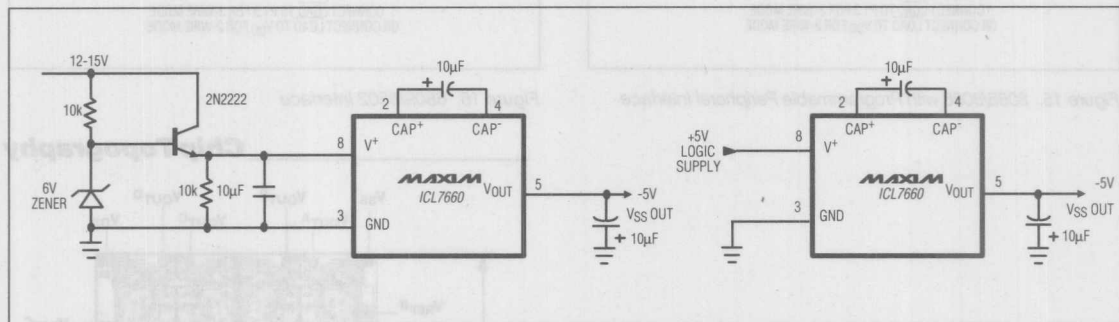


Figure 12. Generating $-5V$ for V_{SS}

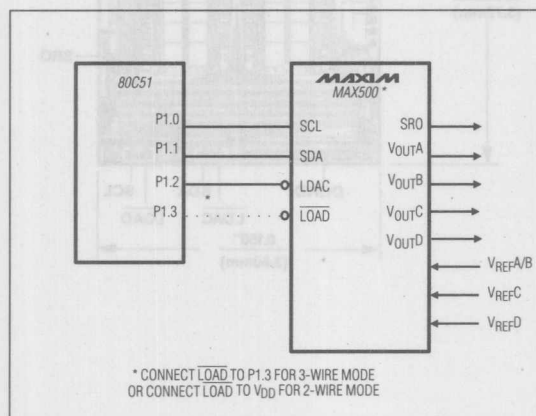


Figure 13. 80C51 Interface

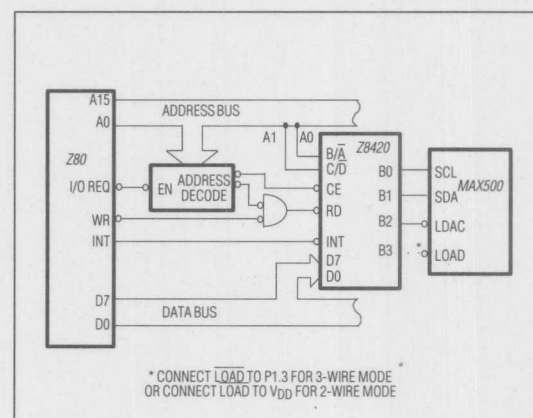


Figure 14. Z-80 with Z8420 PIO Interface

CMOS Quad, Serial Interface, 8-Bit D/A Converter

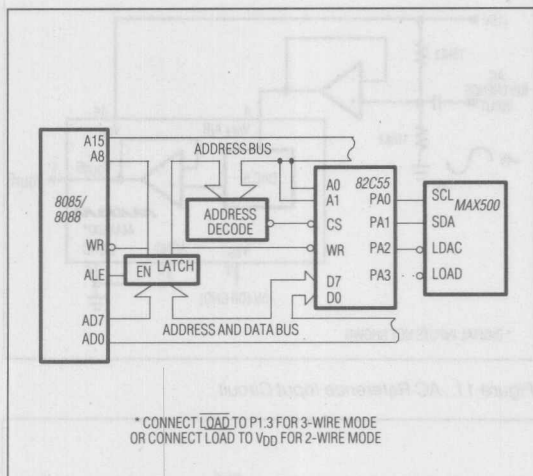


Figure 15. 8085/8088 with Programmable Peripheral Interface

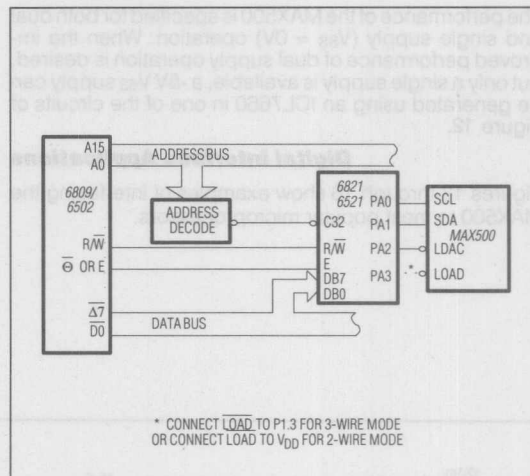
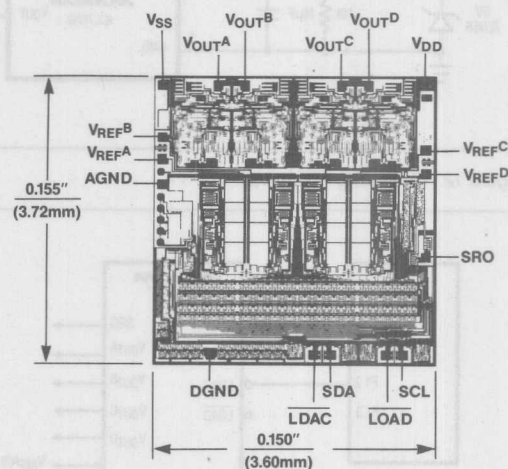


Figure 16. 6809/6502 Interface

Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

CMOS 12-Bit Serial Input Multiplying D/A Converter

MAX543

General Description

The MAX543 is a 12-bit current-output multiplying digital-to-analog converter (DAC) that is packaged in a space-saving 8-pin DIP or 16-pin surface mount SO. Its 3-wire serial interface saves additional circuit board space and also results in low power dissipation. When used with microprocessors (μ P) with a serial port, the MAX543 minimizes the digital noise feed-through from its input pins to its output. The serial port can be used as a dedicated analog bus and kept inactive while the MAX543 is in use. Serial interfacing also reduces the complexity of opto- or transformer-isolated applications.

The MAX543 contains a 12-bit R-2R type DAC, a serial-in parallel-out shift register, a DAC register and control logic. On the rising edge of the clock (CLK) pulse the serial input (SRI) data is shifted into the MAX543. When all the data is clocked in, it is transferred into the DAC register by taking the LOAD input low.

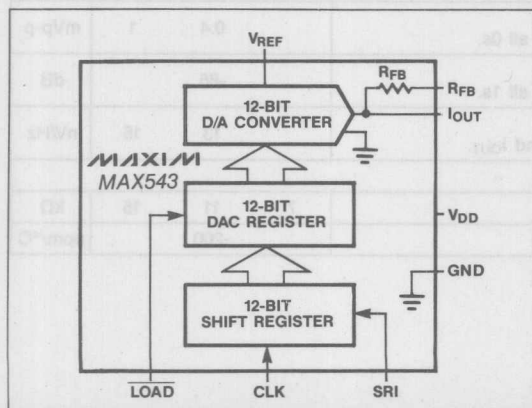
The MAX543 is specified both with a single +5V and +15V power supply. With a +5V supply, the digital inputs are TTL and +5V CMOS compatible. High voltage CMOS compatibility is maintained with a +15V supply.

Maxim's MAX543 uses low tempco thin-film resistors laser trimmed to $\pm 1/4$ LSB linearity and better than ± 1 LSB gain accuracy. The digital inputs are protected against electrostatic discharge (ESD) damage and can typically withstand over 5,000V of ESD voltages.

Applications

Automatic Calibration
Motion Control Systems
 μ P Controlled Systems
Programmable Amplifiers/Attenuators
Digitally Controlled Filters

Functional Block Diagram



Features

- ◆ 12-Bit Accuracy in 8-Pin Mini-DIP
- ◆ Fast 3-Wire Serial Interface
- ◆ Low INL and DNL ($\pm 1/2$ LSB Max)
- ◆ Gain Accuracy to ± 1 LSB Max
- ◆ Low Gain Tempco (5ppm/ $^{\circ}$ C Max)
- ◆ Operates with +5V or +15V Supplies
- ◆ TTL/CMOS Compatible
- ◆ ESD Protected

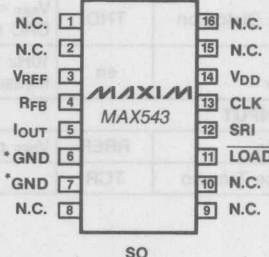
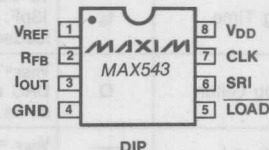
Ordering Information

PART	TEMP. RANGE	PACKAGE	LINEARITY
MAX543ACPA	0 $^{\circ}$ C to +70 $^{\circ}$ C	Plastic DIP	$\pm 1/2$ LSB
MAX543BCPA	0 $^{\circ}$ C to +70 $^{\circ}$ C	Plastic DIP	± 1 LSB
MAX543ACWE	0 $^{\circ}$ C to +70 $^{\circ}$ C	Wide SO	$\pm 1/2$ LSB
MAX543BCWE	0 $^{\circ}$ C to +70 $^{\circ}$ C	Wide SO	± 1 LSB
MAX543AEWE	-40 $^{\circ}$ C to +85 $^{\circ}$ C	Wide SO	$\pm 1/2$ LSB
MAX543BEWE	-40 $^{\circ}$ C to +85 $^{\circ}$ C	Wide SO	± 1 LSB
MAX543BC/D	0 $^{\circ}$ C to +70 $^{\circ}$ C	Dice	± 1 LSB
MAX543AEJA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	CERDIP	$\pm 1/2$ LSB
MAX543BEJA	-40 $^{\circ}$ C to +85 $^{\circ}$ C	CERDIP	± 1 LSB
MAX543AMJA	-55 $^{\circ}$ C to +125 $^{\circ}$ C	CERDIP	$\pm 1/2$ LSB
MAX543BMJA	-55 $^{\circ}$ C to +125 $^{\circ}$ C	CERDIP	± 1 LSB

All DIP packages are 8 leads; all SO packages are 16 leads.

Pin Configurations

Top View



* Leads 6 and 7 must be connected together as close to the package as possible.

MAXIM

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Maxim Integrated Products 2-13

CMOS 12-Bit Serial Input Multiplying D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	+17V
V_{REF} to GND	$\pm 25V$
V_{RFB} to GND	$\pm 25V$
Digital Input Voltage to GND	-0.3V, $V_{DD} + 0.3V$
V_{IOUT} to GND	-0.3V, $V_{DD} + 0.3V$
Power dissipation to +75°C (any package)	470mW
Derate above +75°C by	6mW/°C

Operating Temperature Ranges

MAX543AC/BC	0°C to 70°C
MAX543AE/BE	-40°C to +85°C
MAX543AM/BM	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering 10 seconds)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = +5V, +12V$ or $+15V$; $V_{REF} = +10V$; $V_{IOUT} = GND = 0V$; over specified temperature range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		12			Bits
Integral Nonlinearity	INL	MAX543A MAX543B		$\pm 1/2$ ± 1		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic to 12 bits over temperature MAX543A MAX543B		$\pm 1/2$ ± 1		LSB
Gain Error	FSE	Using internal R_{FB} $T_A = +25^\circ C$ $T_A = T_{MIN}$ to T_{MAX}		± 1 ± 2 ± 2		LSB
Gain Tempco $\Delta Gain/\Delta Temp$ (Note 1)	TCFS	Using internal R_{FB}		± 1	± 5	ppm/°C
DC Supply Rejection	PSR	$\Delta V_{DD} = \pm 5\%$			± 0.001	%/%
DYNAMIC PERFORMANCE (Note 1)						
Current Settling Time	t_s	To 1/2LSB. I_{OUT} load is $100\Omega \parallel 13pF$. DAC register alternately loaded with all 1s and all 0s. $T_A = +25^\circ C$		0.25	1	μs
Digital to Analog Glitch	Q	$V_{REF} = 0V$. I_{OUT} load is $100\Omega \parallel 13pF$. DAC register alternately loaded with all 1s and all 0s.		2	20	nV-s
AC Feedthrough at I_{OUT}	FTE	$V_{REF} = \pm 10V_{p-p}$ at 10kHz. DAC register loaded with all 0s.		0.4	1	mVp-p
Total Harmonic Distortion	THD	$V_{REF} = 6V_{rms}$ at 1kHz. DAC register loaded with all 1s.		-85		dB
Output Noise Voltage Density	e_n	10Hz to 100kHz. Measured between R_{FB} and I_{OUT} .		13	15	nV/Hz
REFERENCE INPUT						
Input Resistance	RREF	V_{REF} pin to I_{OUT}	7	11	15	k Ω
Input Resistance Tempco	TCR			-200		ppm/°C

CMOS 12-Bit Serial Input Multiplying D/A Converter

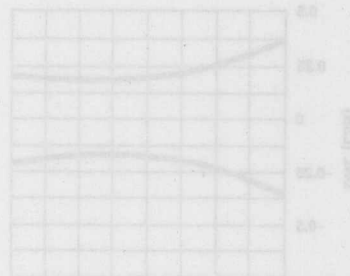
ELECTRICAL CHARACTERISTICS (Continued)

($V_{DD} = +5V, +12V$ or $+15V$; $V_{REF} = +10V$; $V_{IOUT} = GND = 0V$; over specified temperature range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG OUTPUT							
I _{OUT} Leakage Current	I _{LKG}	DAC register loaded with all 0s.	T _A = +25°C		±0.5	±5	nA
			T _A = T _{MIN} to T _{MAX}	MAX543AC/BC/AE/BE		±25	
				MAX543AM/BM		±100	
I _{OUT} Capacitance (Note 1)	C _{OUT}	DAC register loaded with all 0s.		55	80	pF	
		DAC register loaded with all 1s.		85	110		
DIGITAL INPUTS							
Input High Voltage	V _{IH}		V _{DD} = +5V V _{DD} = +15V	2.4 13.5			V
Input Low Voltage	V _{IL}		V _{DD} = +5V V _{DD} = +15V			0.8 1.5	V
Input Leakage Current	I _{IN}	Digital Inputs at 0V or V _{DD}				±1	μA
Input Capacitance (Note 1)	C _{IN}	Digital Inputs at 0V or V _{DD}				8	pF
SWITCHING CHARACTERISTICS (Note 2)							
CLK Pulse Width High	t _{CH}			90			ns
CLK Pulse Width Low	t _{CL}			120			ns
SRI Data to CLK Setup	t _{DS}			40			ns
SRI Data to CLK Hold	t _{DH}			80			ns
LOAD Pulse Width	t _{LD}			120			ns
LSB CLK to LOAD	t _{SL}			0			ns
LOAD High to CLK	t _{LC}			0			ns
POWER SUPPLY							
V _{DD} Range	V _{DD}		V _{DD} = +12V or +15V V _{DD} = +5V	+11.4 +4.75		+15.75 +5.25	V
I _{DD} Range	I _{DD}	All digital inputs at V _{IL} or V _{IH}				500	μA
		All digital inputs at 0V or V _{DD}			5	100	

Note 1: Guaranteed by design and not subject to test.

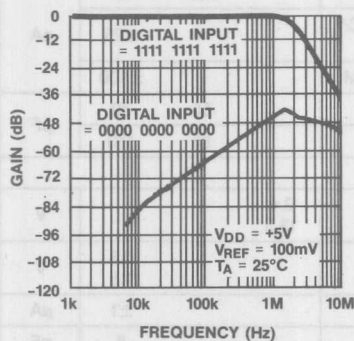
Note 2: Sample tested at $+25^\circ C$ to ensure compliance.



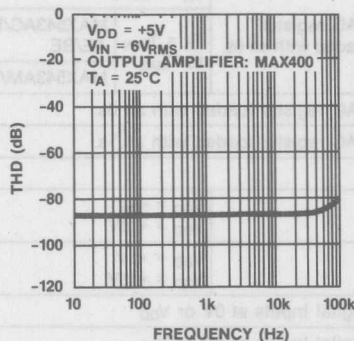
CMOS 12-Bit Serial Input Multiplying D/A Converter

Typical Operating Characteristics

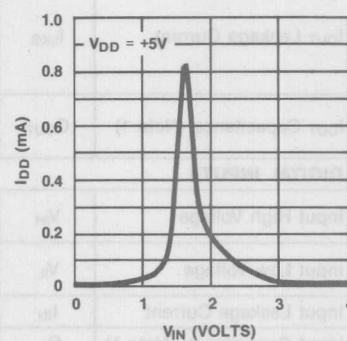
GAIN vs FREQUENCY
(OUTPUT AMPLIFIER: MAX400)



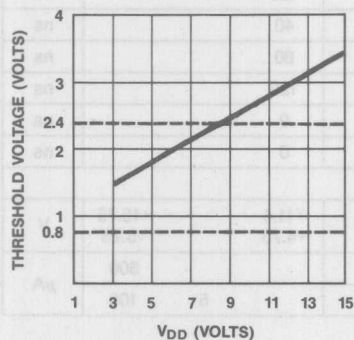
TOTAL HARMONIC DISTORTION
vs FREQUENCY
(MULTIPLYING MODE)



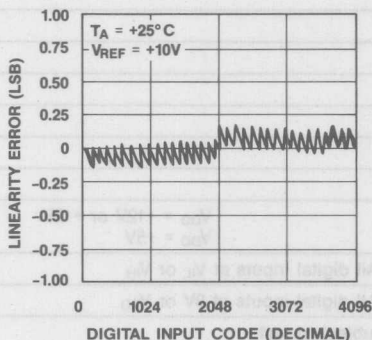
SUPPLY CURRENT vs
LOGIC INPUT VOLTAGE



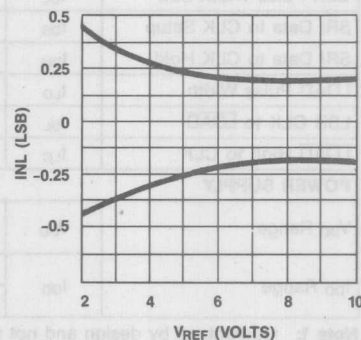
LOGIC THRESHOLD VOLTAGE
vs SUPPLY VOLTAGE



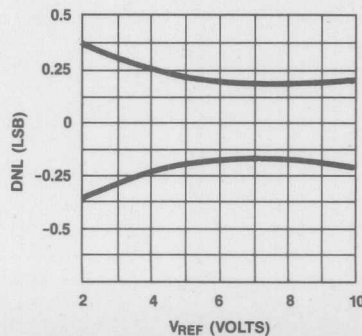
LINEARITY ERROR vs
DIGITAL CODE



LINEARITY ERROR vs
REFERENCE VOLTAGE



DNL ERROR vs
REFERENCE VOLTAGE



CMOS 12-Bit Serial Input Multiplying D/A Converter

MAX543

Detailed Description D/A Converter

The MAX543 DAC circuit consists of a laser trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binary weighted currents are switched to either I_{OUT} or GND depending on the status of each input data bit. Although the current at I_{OUT} and GND depends on the digital input code, the sum of the two output currents are always equal to the input current at V_{REF} .

The current output I_{OUT} can be converted into a voltage by adding an external output amplifier (Figure 3). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

The internal feedback resistor R_{FB} is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The I_{OUT} pin output capacitance, C_{OUT} , is code dependent and is typically 55pF with all switches to GND and 85pF with all switches to I_{OUT} .

Digital Circuit

Figure 2 shows the timing diagram for the MAX543. The MSB is always loaded first on the rising edge of clock. When all the data is shifted into the MAX543, the DAC register is loaded by taking the LOAD signal low. The DAC register is transparent when LOAD is low and latched when LOAD is high. If the LOAD signal is taken low before the LSB bit is fully shifted into the shift register, the DAC output can produce a "glitch". If this is undesirable, the LOAD signal can be delayed 30ns after the rising edge of the LSB clock edge to avoid this condition.

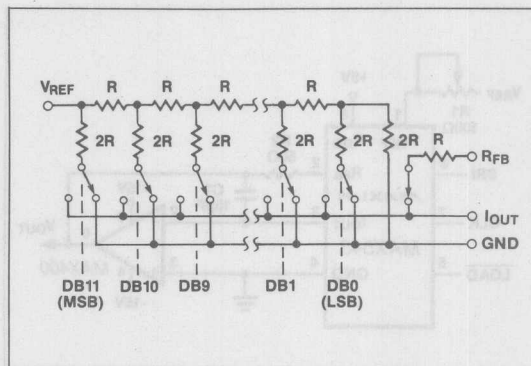


Figure 1. Simplified D/A Circuit of MAX543

The input buffer inverters of the MAX543 act as level shifters converting TTL levels into CMOS logic levels. These input buffers are TTL and +5V-CMOS compatible (0.8V and 2.4V) at $V_{DD} = +5V$. For $V_{DD} = +15V$ the input buffers are CMOS compatible (1.5V and 13.5V). At this supply voltage the input buffers are in their linear region when the input voltages are between 1V and 6V. Therefore to minimize high supply currents, the digital input voltages should be kept as close to the supply and ground voltages (V_{DD} and GND) as possible.

Circuit Configurations

Unipolar Operation

Basic application of the MAX543 is shown in Figure 3. This circuit is used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, V_{REF} .

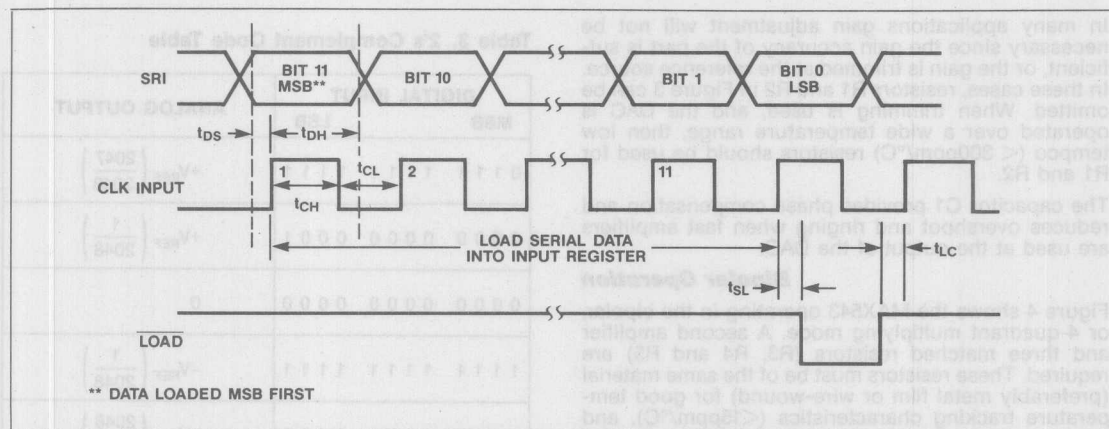


Figure 2. Write Cycle Timing Diagram

CMOS 12-Bit Serial Input Multiplying D/A Converter

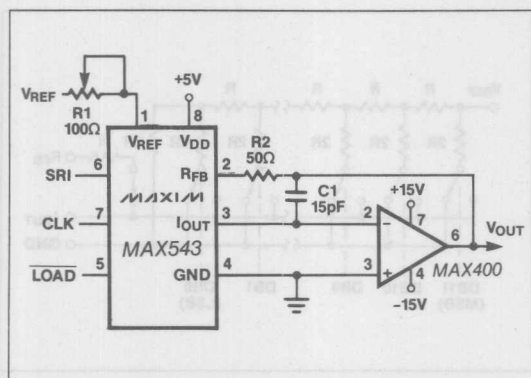


Figure 3. Unipolar Operation

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT		ANALOG OUTPUT
MSB	LSB	
1 1 1 1	1 1 1 1	$+V_{REF} \left(\frac{4095}{4096} \right)$
1 0 0 0	0 0 0 0	$-V_{REF} \left(\frac{2048}{4096} \right) = -\frac{V_{REF}}{2}$
0 0 0 0	0 0 0 1	$-V_{REF} \left(\frac{1}{4096} \right)$
0 0 0 0	0 0 0 0	0

In many applications gain adjustment will not be necessary since the gain accuracy of the part is sufficient, or the gain is trimmed at the reference source. In these cases, resistors R1 and R2 in Figure 3 can be omitted. When trimming is used, and the DAC is operated over a wide temperature range, then low tempco ($< 300\text{ppm}/^\circ\text{C}$) resistors should be used for R1 and R2.

The capacitor C1 provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the output of the DAC.

Bipolar Operation

Figure 4 shows the MAX543 operating in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors (R3, R4 and R5) are required. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature tracking characteristics ($< 15\text{ppm}/^\circ\text{C}$), and should match to 0.01% for 12-bit performance. The output code is offset binary and is listed in Table 2. In

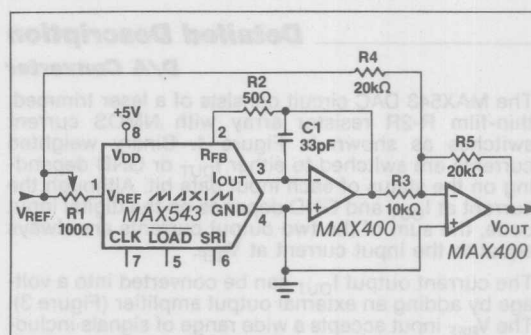


Figure 4. Bipolar Operation

Table 2. Offset Binary Code Table for Circuit of Figure 4

DIGITAL INPUT		ANALOG OUTPUT
MSB	LSB	
1 1 1 1	1 1 1 1	$+V_{REF} \left(\frac{2047}{2048} \right)$
1 0 0 0	0 0 0 0	$+V_{REF} \left(\frac{1}{2048} \right)$
1 0 0 0	0 0 0 0	0
0 1 1 1	1 1 1 1	$-V_{REF} \left(\frac{1}{2048} \right)$
0 0 0 0	0 0 0 0	$-V_{REF} \left(\frac{2048}{2048} \right)$

Table 3. 2's Complement Code Table

DIGITAL INPUT		ANALOG OUTPUT
MSB	LSB	
0 1 1 1	1 1 1 1	$+V_{REF} \left(\frac{2047}{2048} \right)$
0 0 0 0	0 0 0 0	$+V_{REF} \left(\frac{1}{2048} \right)$
0 0 0 0	0 0 0 0	0
1 1 1 1	1 1 1 1	$-V_{REF} \left(\frac{1}{2048} \right)$
1 0 0 0	0 0 0 0	$-V_{REF} \left(\frac{2048}{2048} \right)$

CMOS 12-Bit Serial Input Multiplying D/A Converter

multiplying applications, the MSB determines output polarity while the other 11 bits control the amplitude. The MSB can be inverted in software using an exclusive-OR instruction to make the MAX543 work with 2's complement coding. Table 3 shows the code relationships to output voltage for the 2's complement operation.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. In many applications the gain adjustment will not be necessary, especially when using parts with a guaranteed maximum ± 1 LSB gain error. In these cases, the gain can be trimmed at the reference source and resistors R1 and R2 in Figure 4 omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco ($<300\text{ppm}/^\circ\text{C}$) resistors should be used for R1 and R2.

Single Supply Operation (Voltage Mode)

The MAX543 can be conveniently used in single supply (voltage mode) operation with I_{OUT} biased at any voltage between GND and V_{DD} . I_{OUT} must not be allowed to go 0.3V lower than the GND or 0.3V higher than V_{DD} . Otherwise, internal diodes would turn on causing a high current flow from the supply which could damage the device.

Figure 5 shows the MAX543 connected as a voltage output DAC. I_{OUT} is connected to the reference voltage source and GND is grounded. The DAC output, now appears at the V_{REF} pin which has a constant impedance equal to the reference input resistance (typically 11k Ω). This output should be buffered with an op amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

The input impedance of the reference input (I_{OUT}) for this mode is code dependent, and the response time of the circuit depends on the behavior of the reference source with changing load conditions.

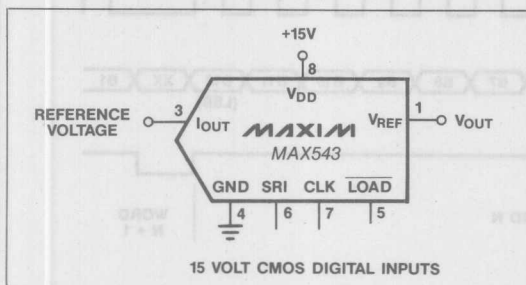


Figure 5. Single Supply Operation Using Voltage Switching Mode

Two advantages of the voltage mode operation are single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (I_{OUT}) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral (INL) and differential nonlinearity (DNL).

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode.

MAX543 Opto-Isolated Application

Figure 6A shows the MAX543 interface to optocouplers for isolated barrier applications. Three optocouplers (OC1 thru OC3) carry the serial data and clocking signals across the isolation barrier. Isolated power sources, V^+ and V^- , supply the MAX543, the output amplifier and optocouplers. If data word updates are infrequent, and large analog output transitions can be tolerated while serial data is being clocked in, then parts count can be reduced by eliminating optocoupler OC3 and tying LOAD (pin 5) of the MAX543 low.

Using type 6N136 optocouplers this circuit accepts serial data at a maximum clock rate of 100kHz, or 130 μs per data word. The SERIAL DATA and LOAD signals should change coincident with the falling edge of CLOCK, as shown in the timing diagram (Figure 6B). A positive CLOCK cycle is masked during the time that LOAD is low.

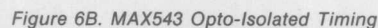
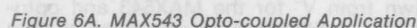
The MAX543 will also work with +5V isolated supplies using the optocoupler circuit of Figure 6A. The values of R1 through R3 should be changed to 3k Ω to maintain switching speed with the lower value of V^+ .

Current drawn from V^- for the MAX543 and optocoupler is 3.5mA at 100kHz clock rate when all data bits are set to zero. V^+ current drops to zero (excluding reference and op amp current) when no new data is being loaded and CLOCK, SERIAL DATA, and LOAD are static high.

Microprocessor Interfacing Interfacing to the 8085

Figure 7 shows the MAX543 interfacing to the 8085 microprocessor. The SOD line from the 8085 is used to send serial data to the DAC. This data is clocked into the MAX543 by executing memory write instructions. The CLK input for the DAC can be generated by decoding address 8000 and the WR signal. The data is transferred into the DAC register with a memory write instruction to address A000 which brings LOAD low. The data for the MAX543 is stored in the right-justified format in registers H and L of the 8085.

MAX543



CMOS 12-Bit Serial Input Multiplying D/A Converter

MAX543

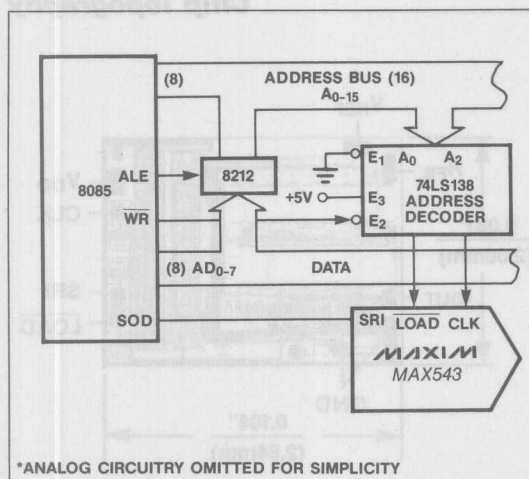


Figure 7. MAX543 - 8085 Interface

Interfacing to the MC6800

Figure 8 shows the MAX543 interfacing to the MC6800 microprocessor. The data is transferred into the MAX543 by executing successive memory WRITE instructions while changing the data between WRITES to construct the serial data to the DAC.

The DB7 data line is used for the SRI signal. The lower half of the memory location 0000 holds the four MSB data bits, and the 0001 location holds the eight LSB data bits. The memory address 2000, R/W, and 02 are decoded to generate the CLK signal for the DAC with each memory WRITE. Similarly, a memory WRITE to address 4000 transfers data into the DAC register by bringing the MAX543's LOAD input low.

Application Information

Output Amplifier Offset

For best linearity, I_{OUT} and GND should be terminated at exactly 0V. In most applications I_{OUT} is connected to the summing junction of an inverting op amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS} (1 + R_{FB}/R_O)$$

where V_{OS} is the op amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically 4/3 V_{OS} to 2 V_{OS} , a change of 2/3 V_{OS} . An amplifier with 3mV of offset will, therefore, degrade the linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10LSB.

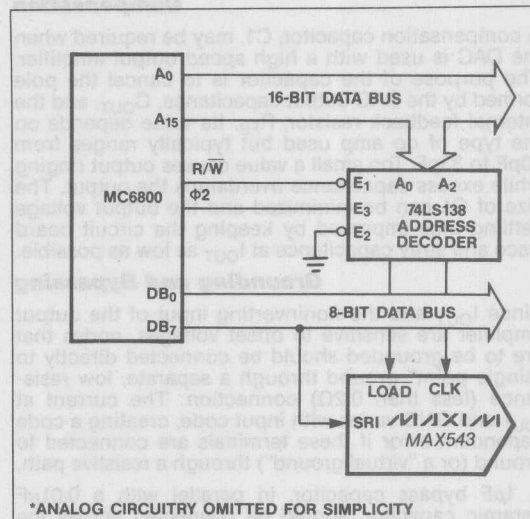


Figure 8. MAX543 - MC6800 Interface

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should, therefore, be much less than the DAC output current for 1 LSB, typically 250nA with $V_{REF} = 10V$. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor." This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} pin to I_{OUT} . This normally is a function of board layout and lead-to-lead package capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF} , and I_{OUT} pins.

The DAC output follows the digital inputs when the LOAD pin is low. In this mode invalid outputs and voltage glitches can appear at the DAC output. Keeping the LOAD input high until all the data is shifted into the MAX543 eliminates this problem.

CMOS 12-Bit Serial Input Multiplying D/A Converter

Compensation

A compensation capacitor, C1, may be required when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT} , and the internal feedback resistor, R_{FB} . Its value depends on the type of op amp used but typically ranges from 10pF to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at I_{OUT} as low as possible.

Grounding and Bypassing

Since I_{OUT} and the noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low resistance (less than 0.2Ω) connection. The current at I_{OUT} and GND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A $1\mu F$ bypass capacitor, in parallel with a $0.01\mu F$ ceramic capacitor, should be connected across the DAC V_{DD} and GND as close to the pins as possible.

The MAX543 has high impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or GND when not used. It is good practice to connect active inputs to V_{DD} or GND through high valued resistors ($1M\Omega$) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected.

Chip Topography

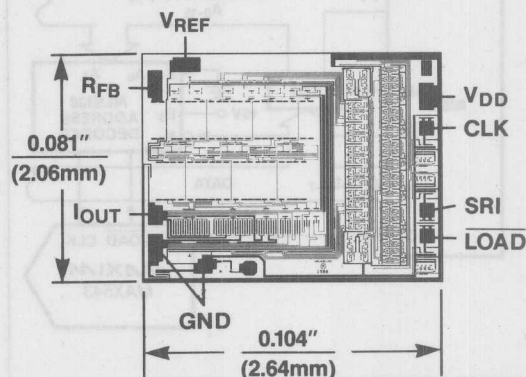


Figure 8 shows the MAX543 interfacing to the MC6800 microprocessor. The data is transferred into the MAX543 by executing successive memory WRITE instructions while changing the data between WRITE to construct the serial data to the DAC. The \overline{CS} data line is used for the SRI signal. The lower half of the memory location 0000 holds the four MSB data bits, and the 0001 location holds the eight LSB data bits. The memory address 0000, R/W, and 02 are decoded to generate the CLK signal for the DAC with each memory WRITE. Similarly a memory WRITE to address 0000 transfers data into the DAC register by changing the MAX543's LOAD input low.

Application Information

Output Amplifier Offset

For best linearity, I_{OUT} and GND should be terminated at exactly 0V in most applications. I_{OUT} is connected to the summing junction of an inverting op amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is

$$\text{Error Voltage} = V_{OS} \left(1 + \frac{R_{FB}}{R_{IN}} \right)$$

where V_{OS} is the op amp's offset voltage and R_{IN} is the output resistance of the DAC. R_{IN} is a function of the digital input code and varies from approximately 1k Ω to 32k Ω . The error voltage range is then typically 1mV to 32mV. A change of 2.5mV in V_{OS} will therefore degrade the linearity by 3mV or offset will therefore degrade the linearity by 3mV almost a full LSS with a 10V reference voltage. For best linearity, a low offset amplifier such as the MAX420 should be used or the amplifier offset must be trimmed to zero. A good rule of thumb is that

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.



Voltage References

MAX674	+10V Precision Voltage Reference	3-1
MAX675	+5V Precision Voltage Reference	3-5

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

+10V Precision Voltage Reference

MAX674

General Description

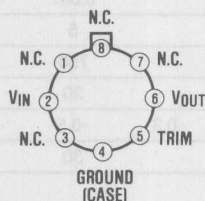
The MAX674 is a precision voltage reference that is pretrimmed to within $\pm 0.15\%$ of 10V. The reference features excellent temperature stability (as low as 12.0ppm/ $^{\circ}\text{C}$ guaranteed), low current drain and low noise. It is supplied in the space-saving narrow Small Outline package, as well as, the standard 8-pin TO-99 Metal Can, Plastic DIP and Cerdip packages.

Applications

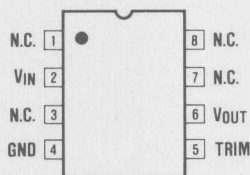
A/D Converters
D/A Converters
Digital Voltmeters
Voltage Regulators
Threshold Detectors

Pin Configuration

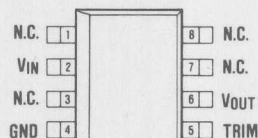
Top View



TO-99 Metal Can



DIP/CERDIP



Small Outline

Features

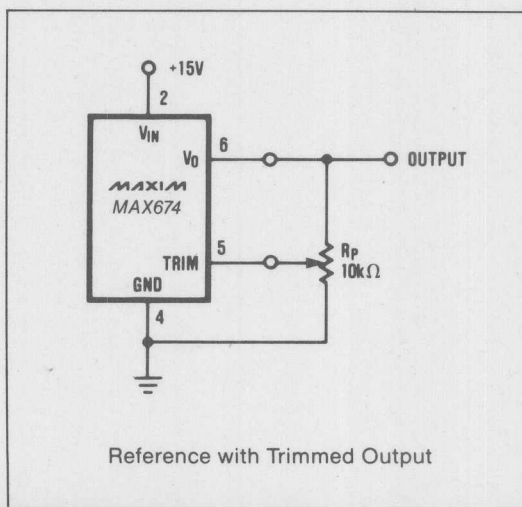
- ◆ Pretrimmed to +10V, $\pm 0.15\%$
- ◆ Excellent Temperature Stability: 12ppm/ $^{\circ}\text{C}$
- ◆ Low Noise: 20 μV p-p
- ◆ Low Supply Current: 1.4mA Max
- ◆ Short-Circuit Proof
- ◆ Load Regulation 0.001%/mA
- ◆ Pin-For-Pin Compatible with REF01

Ordering Information

PART	PACKAGE*	TEMP. COEFFICIENT ppm/ $^{\circ}\text{C}$	INITIAL ERROR mV
TEMP. RANGE: 0°C to $+70^{\circ}\text{C}$			
MAX674CTV	TO-99	12	15
MAX674CPA	Plastic DIP	12	15
MAX674CSA	Narrow SO	12	15
TEMP. RANGE: -40°C to $+85^{\circ}\text{C}$			
MAX674ETV	TO-99	15	15
MAX674EJA	CERDIP	15	15
MAX674EPA	Plastic DIP	15	15
MAX674ESA	Narrow SO	15	15
TEMP. RANGE: -55°C to $+125^{\circ}\text{C}$			
MAX674MTV	TO-99	20	15
MAX674MJA	CERDIP	20	15

*All devices — 8-pin packages

Typical Operating Circuit



MAXIM

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Maxim Integrated Products 3-1

+10V Precision Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V	Operating Temperature Range	
Power Dissipation		MAX674C	0°C to +70°C
TO-99 (TV) (Derate at 7.1mW/°C above +80°C)	500mW	MAX674E	-40°C to +85°C
CERDIP (J) (Derate at 6.7mW/°C above +75°C)	500mW	MAX674M	-55°C to +125°C
Plastic DIP (P) (Derate at 5.6mW/°C above +36°C)	500mW	Lead Temperature (Soldering, 60 sec)	+300°C
Narrow Small Outline (S)		DICE Junction Temperature (T _J)	-65°C to +150°C
(Derate at 5.0mW/°C above +55°C)	300mW	Output Short-Circuit Duration	
Storage Temperature Range	-65°C to +150°C	(to Ground or V _{IN})	Indefinite

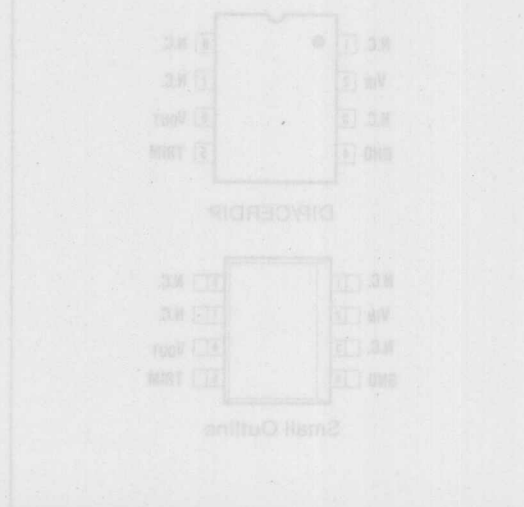
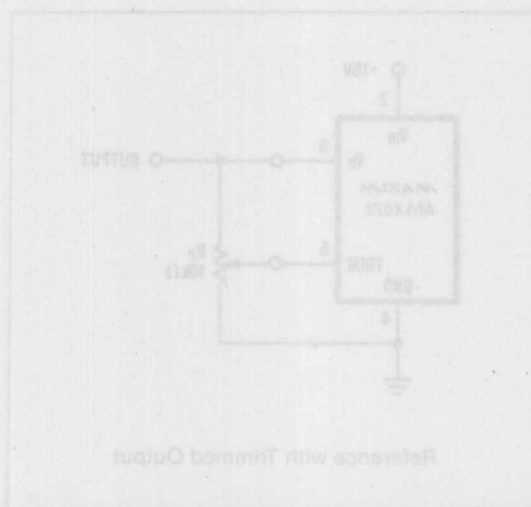
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS (V_{IN} = +15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Tolerance		I _L = 0mA			±15	mV
Output Voltage Change with Temperature	TCV _O	MAX674CTV/CPA/CSA MAX674ETV/EJA/EPA/ESA MAX674MTV/MJA			12 15 20	ppm/°C
Output Adjustment Range	V _{TRIM}	R _p = 10	±300	±600		mV
Line Regulation (Note 1)		V _{IN} = 13V to 33V		0.006	0.01	%/V
Load Regulation (Note 1)		I _L = 0 to 10mA		0.001	0.002	%/mA
Turn-on Settling Time	t _{ON}	To ±0.1% of final value		5		μs
Quiescent Supply Current	I _Q	No load		750	1400	μA
Noise (Note 2)	e _{np-p}	0.1Hz to 10Hz		20	30	μV _{p-p}
Sink Current	I _S		-0.3	-0.5		mA
Short-Circuit Current	I _{SC}	V _O = 0		30		mA

Note 1: Line and Load Regulation specifications include the effect of self heating.

Note 2: Noise is sample tested.



+10V Precision Voltage Reference

MAX674

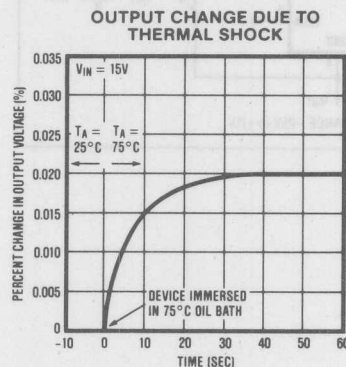
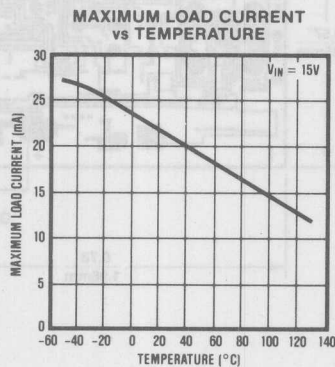
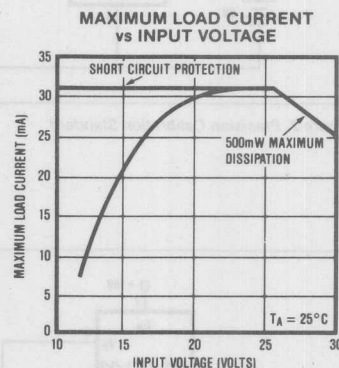
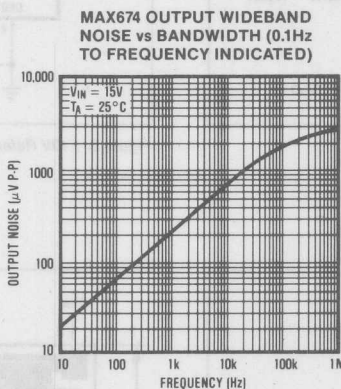
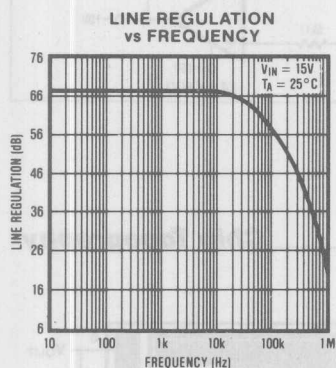
Output Adjustment

The MAX674 trim terminal can be used to adjust the output voltage over a $10V \pm 300mV$ range. This feature allows system errors to be trimmed by setting the reference to a voltage other than 10V such as 10.240V for binary applications (see "Typical Operating Circuit"

on first page). The trim terminal may, of course, be left open if no adjustment is needed.

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7ppm/°C for 100mV of output adjustment from its initial value.

Typical Operating Characteristics



3

+10V Precision Voltage Reference

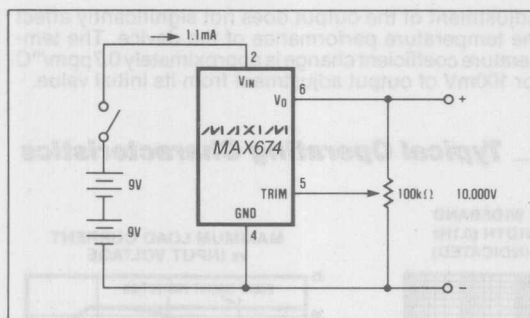


Figure 2. Precision Calibration Standard

Typical Applications

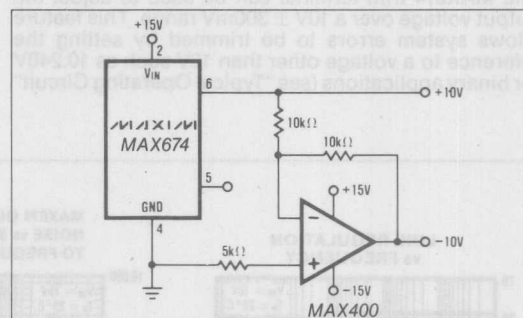


Figure 3. ±10V Reference

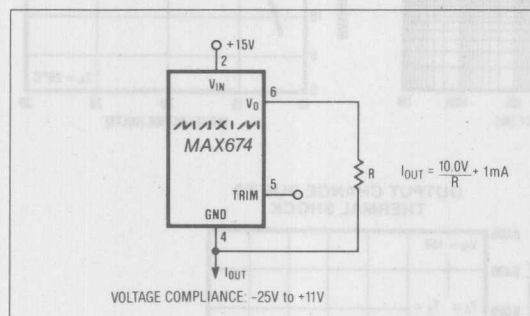
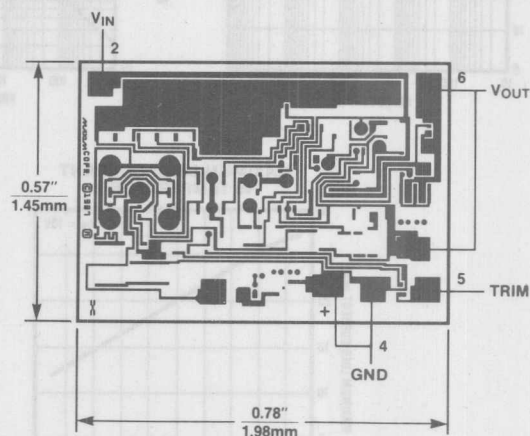


Figure 4. Current Source

Chip Topography



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MAXIM

+5V Precision Voltage Reference

MAX675

General Description

The MAX675 is a precision voltage reference that is pretrimmed to within $\pm 0.15\%$ of 5V. The reference features excellent temperature stability (as low as 12.0ppm/ $^{\circ}\text{C}$ guaranteed), low current drain and low noise. It is supplied in the space-saving narrow Small Outline package, as well as, the standard 8-pin TO-99 Metal Can, Plastic DIP and Cerdip packages.

Features

- ◆ Pretrimmed to +5V, $\pm 0.15\%$
- ◆ Excellent Temperature Stability: 12ppm/ $^{\circ}\text{C}$
- ◆ Low Noise: 10 $\mu\text{V}_{\text{p-p}}$
- ◆ Low Supply Current: 1.4mA Max
- ◆ Short-Circuit Proof
- ◆ Load Regulation 0.001%/mA
- ◆ Pin-For-Pin Compatible with REF02

Applications

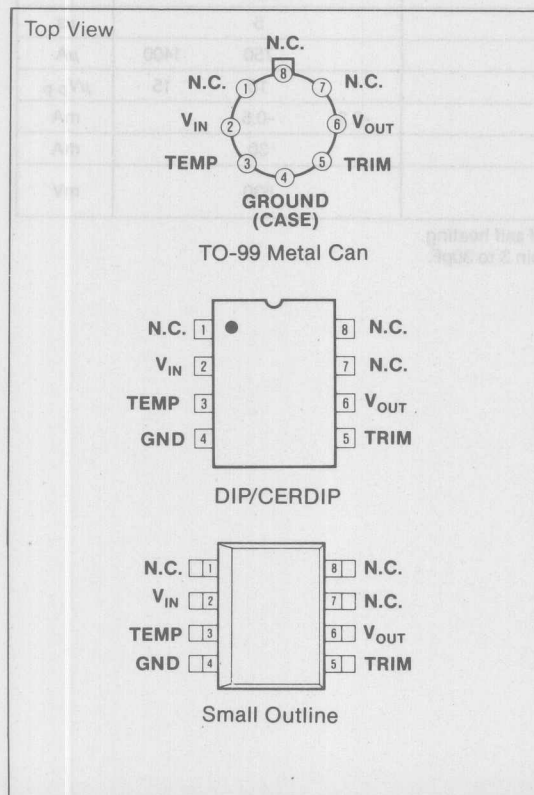
A/D Converters
D/A Converters
Digital Voltmeters
Voltage Regulators
Threshold Detectors

Ordering Information

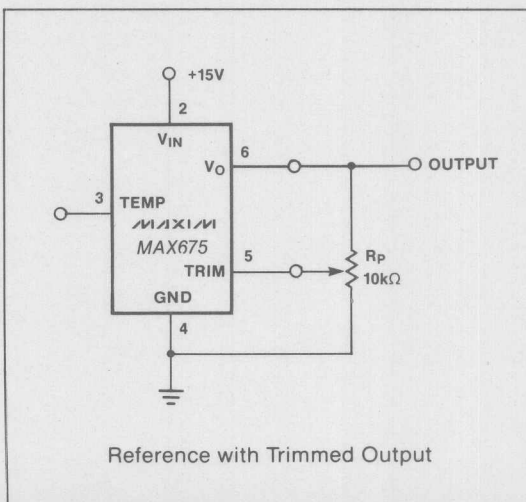
PART	PACKAGE*	TEMP. COEFFICIENT ppm/ $^{\circ}\text{C}$	INITIAL ERROR mV
TEMP. RANGE: 0°C to $+70^{\circ}\text{C}$			
MAX675CTV	TO-99	12	7
MAX675CPA	Plastic DIP	12	7
MAX675CSA	Narrow SO	12	7
TEMP. RANGE: -40°C to $+85^{\circ}\text{C}$			
MAX675ETV	TO-99	15	7
MAX675EJA	CERDIP	15	7
MAX675EPA	Plastic DIP	15	7
MAX675ESA	Narrow SO	15	7
TEMP. RANGE: -55°C to $+125^{\circ}\text{C}$			
MAX675MTV	TO-99	20	7
MAX675MJA	CERDIP	20	7

*All devices — 8-pin packages

Pin Configuration



Typical Operating Circuit



+5V Precision Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V	Operating Temperature Range	
Power Dissipation		MAX675C	0°C to +70°C
TO-99 (TV) (Derate at 7.1mW/°C above +80°C)	500mW	MAX675E	-40°C to +85°C
CERDIP (J) (Derate at 6.7mW/°C above +75°C)	500mW	MAX675M	-55°C to +125°C
Plastic DIP (P) (Derate at 5.6mW/°C above +36°C)	500mW	Lead Temperature (Soldering, 60 sec)	+300°C
Narrow Small Outline (S)		DICE Junction Temperature (T _J)	-65°C to +150°C
(Derate at 5.0mW/°C above +55°C)	300mW	Output Short-Circuit Duration	
Storage Temperature Range	-65°C to +150°C	(to Ground or V _{IN})	Indefinite

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

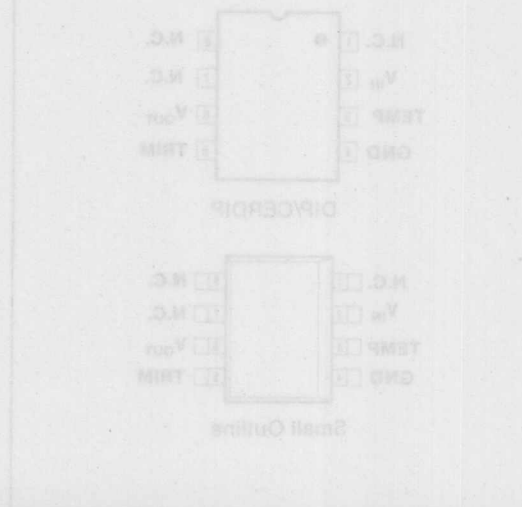
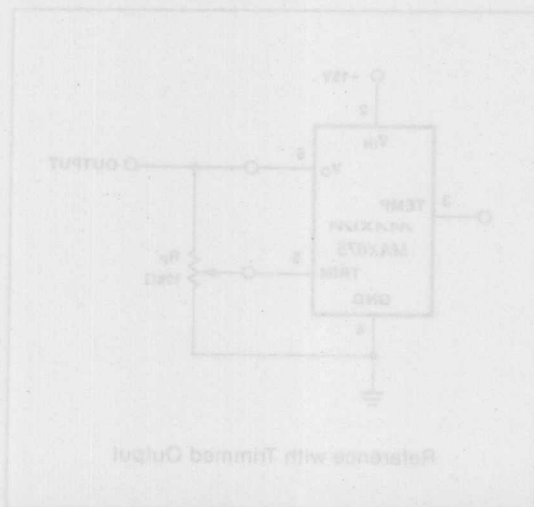
ELECTRICAL CHARACTERISTICS (V_{IN} = +15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Tolerance		I _L = 0mA			±7	mV
Output Voltage Change with Temperature	TCV _O	MAX675CTV/CPA/CSA MAX675ETV/EJA/EPA/ESA MAX675MTV/MJA			12 15 20	ppm/°C
Output Adjustment Range	V _{TRIM}	R _p = 10	±150	±300		mV
Line Regulation (Note 1)		V _{IN} = 8V to 33V		0.006	0.01	%/V
Load Regulation (Note 1)		I _L = 0 to 10mA		0.001	0.002	%/mA
Turn-on Settling Time	t _{ON}	To ±0.1% of final value		5		μs
Quiescent Supply Current	I _Q	No Load		750	1400	μA
Noise (Note 3)	e _n p-p	0.1Hz to 10Hz		10	15	μV _{p-p}
Sink Current	I _S		-0.3	-0.5		mA
Short-Circuit	I _{SC}	V _O = 0		30		mA
Current Temperature Voltage Output	V _T	(Note 2)		630		mV

Note 1: Line and Load Regulation specifications include the effect of self heating.

Note 2: Limit current in or out of pin 3 to 50mA and capacitance on pin 3 to 30pF.

Note 3: Noise is sample tested.



+5V Precision Voltage Reference

MAX675

Output Adjustment

The MAX675 trim terminal can be used to adjust the output voltage over a $5V \pm 150mV$ range. This allows system errors to be trimmed by setting the reference to a voltage other than 5V such as 5.120V for binary applications (see "Typical Operating Circuit" on first page). The trim terminal may, of course, be left open if no adjustment is needed.

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately $0.7ppm/^{\circ}C$ for each 100mV of output adjustment from its initial value.

Temperature Voltage Output

The MAX675 provides a temperature dependent output voltage on the TEMP pin. This voltage is proportional to the absolute temperature, and has a scale factor of approximately $2.1mV/^{\circ}C$ (Figure 2).

Output Voltage = $2.1(T + 273)mV$
where T = Temperature in $^{\circ}C$

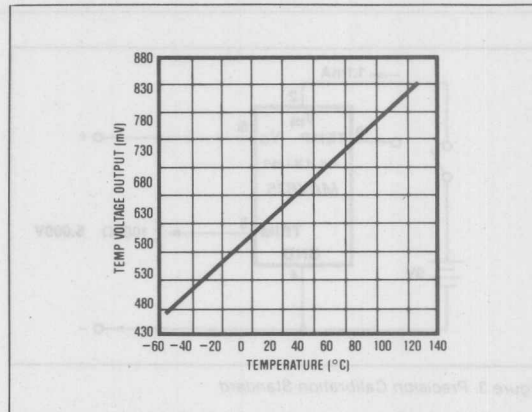
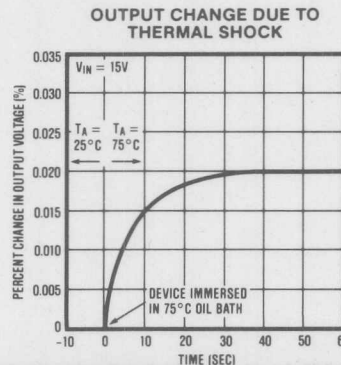
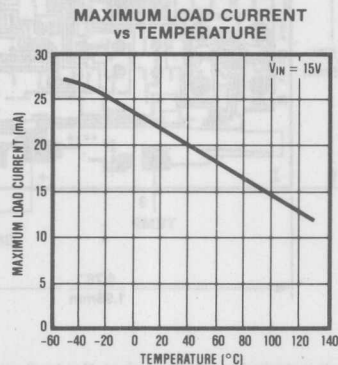
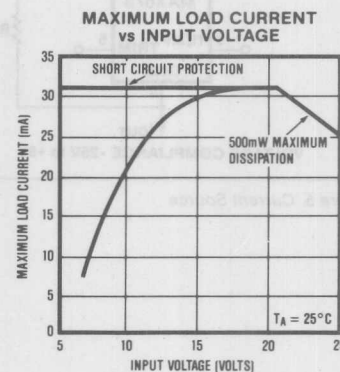
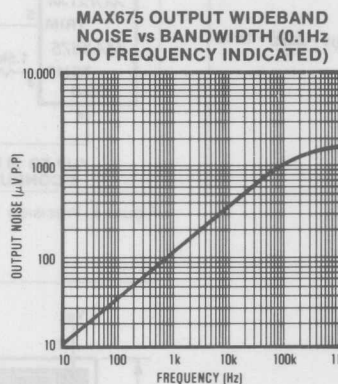
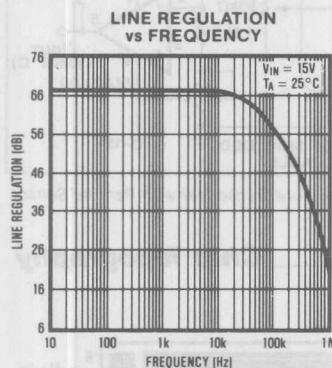


Figure 2. MAX675 Temperature Voltage Output vs. Temperature

Typical Operating Characteristics



+5V Precision Voltage Reference

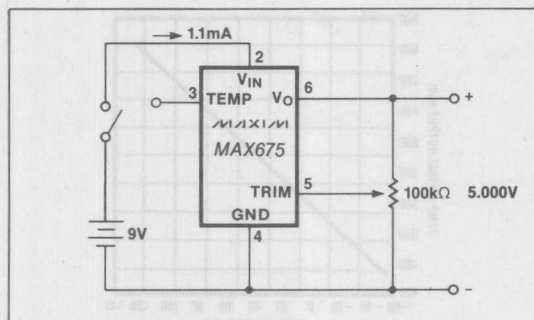


Figure 3. Precision Calibration Standard

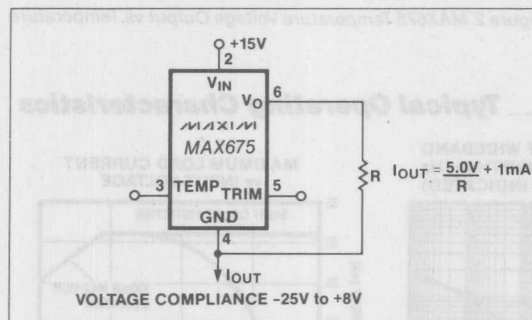


Figure 5. Current Source

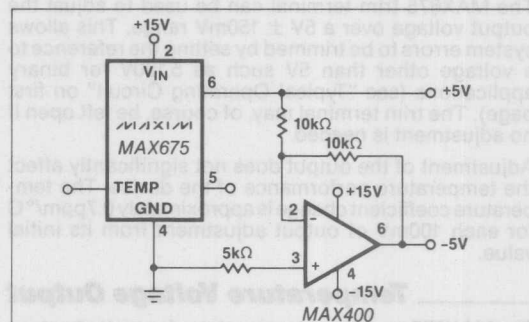


Figure 4. ±5V Reference

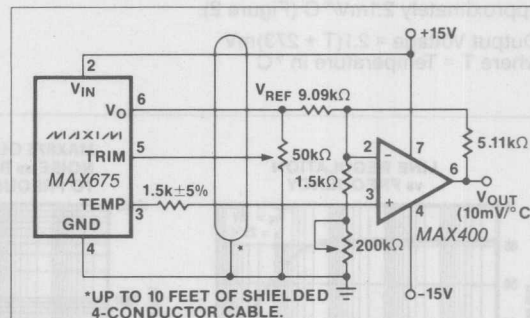
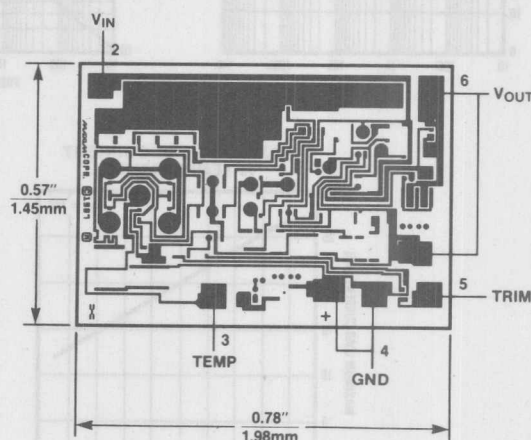


Figure 6. Precision Temperature Transducer with Remote Sensor

Chip Topography



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Op Amps/Buffers/Comparators

MAX9685	Ultra-Fast ECL Output Comparator with Latch Enable	4-1
MAX9686	Very Fast TTL Latched Output Comparator	4-5
MAX9687	Dual Ultra-Fast ECL Output Comparator	4-9
MAX9690	Ultra-Fast ECL Output Comparator	4-13
MAX9698	Very Fast TTL Latched Output Comparator	4-5
MAX402	High-Speed, Low-Power Op Amp	4-17
MAX403	High-Speed, Low-Power Op Amp	4-17
MAX408	Single High-Speed, High Output Current Op Amp	4-19
MAX425	Ultra High-Precision CMOS Op Amp	4-31
MAX426	Ultra High-Precision CMOS Op Amp	4-31
MAX428	Dual High-Speed, High Output Current Op Amp	4-19
MAX430	$\pm 15V$ Chopper Stabilized Operational Amplifier	4-33
MAX432	Low Power, $\pm 15V$ Chopper Stabilized Operational Amplifier	4-33
MAX448	Quad High-Speed, High Output Current Op Amp	4-19
MAX452	50MHz CMOS Video Amplifier	4-41
MAX453	2 Channel 50MHz Video Multiplexer/Amplifier	4-41
MAX454	4 Channel 50MHz Video Multiplexer/Amplifier	4-41
MAX455	8 Channel 50MHz Video Multiplexer/Amplifier	4-41
MAX456	8x8 Crosspoint Video Switch	4-49
MAX457	Dual CMOS Video Amplifier	4-51
MAX480	High-Precision, Low Voltage, Micropower Op Amp	4-55
MAX900	High-Speed, Low-Power Quad Voltage Comparator	4-61
MAX901	High-Speed, Low-Power Quad Voltage Comparator	4-61

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

Ultra-Fast ECL Output Comparator with Latch Enable

General Description

The MAX9685 is an ultra-fast ECL comparator manufactured with a high-frequency bipolar process ($f_T = 6\text{GHz}$), which is capable of very short propagation delays while maintaining the excellent DC matching characteristics normally found only in slower comparators.

The device is pin compatible with the AD9685 and Am6685, but it exceeds the AC characteristics of these devices.

The MAX9685 has differential inputs and complementary outputs fully compatible with ECL logic levels. Output current levels are capable of driving 50Ω terminated transmission lines. The ultra-fast operation makes signal processing possible at frequencies in excess of 600MHz .

A Latch Enable function is provided to allow the comparator to be used in a sample-hold mode. When the Latch Enable is ECL high, the comparator functions normally. When the Latch Enable is driven ECL low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the Latch input transition. If the Latch Enable function is not used, the LE pin must be connected to ground.

Applications

- High-Speed A/D Converters
- High-Speed Line Receivers
- Peak Detectors
- Threshold Detectors
- High-Speed Triggers

Features

- ◆ 1.3ns Propagation Delay
- ◆ 0.5ns Latch Setup Time
- ◆ +5V, -5.2V Power Supplies
- ◆ Pin Compatible with AD9685, Am6685
- ◆ Available in Commercial and Military Temp. Ranges
- ◆ Available in Narrow SO Package

Ordering Information

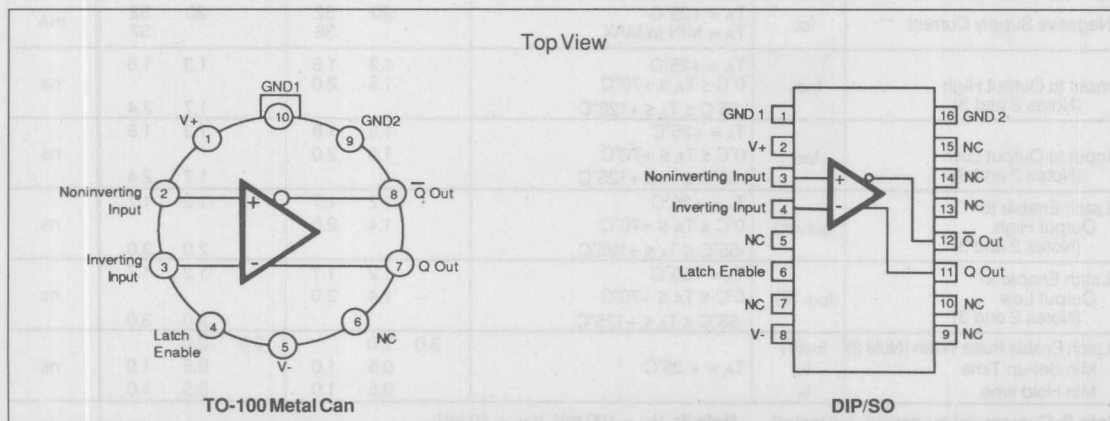
PART	TEMP. RANGE	PIN-PACKAGE*
MAX9685CPE	0°C to +70°C	16 Plastic DIP
MAX9685CSE	0°C to +70°C	16 Narrow SO
MAX9685CJE	0°C to +70°C	16 CERDIP
MAX9685CTW	0°C to +70°C	10 TO-100 Can
MAX9685C/D	0°C to +70°C	Dice
MAX9685MJE	-55°C to +125°C	16 CERDIP
MAX9685MTW	-55°C to +125°C	10 TO-100 Can

*Consult factory for availability of 20 Pin LCC.

MAX9685

4

Pin Configurations



MAXIM

Maxim Integrated Products

4-1

MAXIM is a registered trademark of Maxim Integrated Products.

Ultra-Fast ECL Output Comparator with Latch Enable

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6V
Power Dissipation (Note 1)	336mW
Output Short-Circuit Duration	Indefinite
Input Voltages	±5V
Differential Input Voltages	3.5V
Output Current	30mA

Operating Temperature Range:

Commercial (MAX9685C)	0°C to +70°C
Military (MAX9685M)	-55°C to +125°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Note 1: Power derating above $T_A = 70^\circ\text{C}$ is based on a maximum junction temperature of 150°C and the thermal resistance factors of $\theta_{JC} = 75^\circ\text{C/W}$ and $\theta_{JA} = 145^\circ\text{C/W}$. For SO $\theta_{JC} = 60^\circ\text{C/W}$ and $\theta_{JA} = 110^\circ\text{C/W}$. For TO-100 $\theta_{JC} = 45^\circ\text{C/W}$ and $\theta_{JA} = 150^\circ\text{C/W}$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS (V+ = 5V, V- = -5.2V, $R_L = 50\Omega$, $V_T = -2V$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MAX9685C		MAX9685M		UNITS
				MIN	TYP	MAX	MIN	
Input Offset Voltage	V _{OS}	R _S = 100Ω	T _A = +25°C T _A = MIN to MAX	+5 -7	+5 +7	-5 -8	+5 +8	mV
Temperature Coefficient	ΔV _{OS} /ΔT			10		15		μV/°C
Input Offset Current	I _{OS}	T _A = +25°C T _A = MIN to MAX		5 8		5 12		μA
Input Bias Current	I _B	T _A = +25°C T _A = MIN to MAX		10 20 30		10 20 40		μA
Input Voltage Range	V _{CM}	(Note 2)		-2.5V +2.5V		-2.5V +2.5V		V
Common-Mode Rejection Ratio	CMRR			80		80		dB
Power-Supply Rejection Ratio	PSRR			60		60		dB
Input Resistance	R _{IN}	(Note 2)		60		60		kΩ
Input Capacitance	C _{IN}			3		3		pF
Logic Output High Voltage	V _{OH}	T _A = MIN T _A = MAX T _A = +25°C		-1.05 -0.89 -0.96		-0.87 -0.70 -0.81		V
Logic Output Low Voltage	V _{OL}	T _A = MIN T _A = MAX T _A = +25°C		-1.89 -1.83 -1.85		-1.65 -1.57 -1.65		V
Positive Supply Current	I _{CC}	T _A = +25°C T _A = MIN to MAX		16 22 24		16 22 25		mA
Negative Supply Current	I _{EE}	T _A = +25°C T _A = MIN to MAX		20 32 36		20 32 37		mA
Input to Output High (Notes 2 and 3)	t _{pd+}	T _A = +25°C 0°C ≤ T _A ≤ +70°C -55°C ≤ T _A ≤ +125°C		1.3 1.5		1.8 2.0		ns
Input to Output Low (Notes 2 and 3)	t _{pd-}	T _A = +25°C 0°C ≤ T _A ≤ +70°C -55°C ≤ T _A ≤ +125°C		1.3 1.5		1.8 2.0		ns
Latch Enable to Output High (Notes 2 and 3)	t _{pd+(E)}	T _A = +25°C 0°C ≤ T _A ≤ +70°C -55°C ≤ T _A ≤ +125°C		1.2 1.4		1.7 2.0		ns
Latch Enable to Output Low (Notes 2 and 3)	t _{pd-(E)}	T _A = +25°C 0°C ≤ T _A ≤ +70°C -55°C ≤ T _A ≤ +125°C		1.2 1.4		1.7 2.0		ns
Latch Enable Pulse Width (Note 2)	t _{pw(E)}			3.0		3.0		
Min Set-up Time	t _s	T _A = + 25°C		2.0 0.5		2.0 0.5		ns
Min Hold time	t _h			1.0 0.5		1.0 0.5		

Note 2: Guaranteed by design, not tested.

Note 3: $V_{IN} = 100\text{ mV}$, $V_{OD} = 10\text{ mV}$.

Ultra-Fast ECL Comparator with Latch Enable

MAX9685

Application Information

Layout

Because of the large gain-bandwidth characteristic of the MAX9685, special precautions need to be taken if the high-speed capabilities of the device are to be utilized. A PC board with ground plane should be considered mandatory. All decoupling capacitors should be mounted as close as possible to the power-supply pins, and the ECL outputs should be processed in microstrip fashion consistent with the load termination of 50Ω to 120Ω. For low impedance applications, microstrip layout at the input may also be helpful. Close attention should be paid to the bandwidth of the decoupling and terminating components. Chip components to minimize lead inductance can be used to advantage here. An unused LE pin must be connected to ground.

Input Slew Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices creates oscillation problems when the input traverses through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew rate requirements. The tendency of the part to oscillate is a function of the layout and the source impedance of the circuit employed. Poor layout and larger source impedance will increase the minimum slew rate requirement.

Figure 1 shows a high-speed receiver application with 50Ω input and output termination. With this configuration, in which a ground plane and microstrip PC board were used, the minimum slew rate for clean output switch-

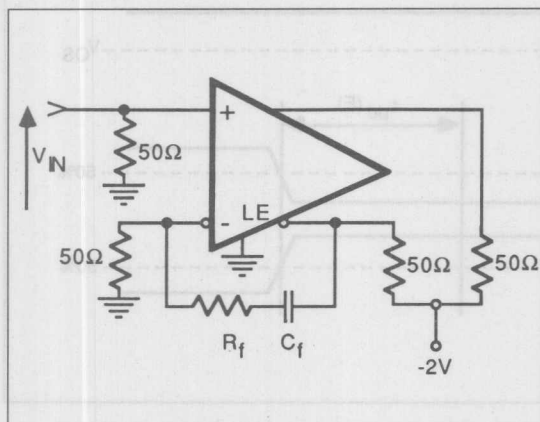


Figure 1. Regenerative Feedback. High-speed receiver with 50Ω input and output termination.

ing is 1.6V/μs. Sine wave inputs imply a minimum signal size of 360mVrms at 500kHz and 90mVrms at 4MHz.

$$E_{RMS} = \frac{\text{SlewRate}}{2\sqrt{2}\pi f}$$

In many applications, the addition of regenerative feedback will assist the input signal through the linear region, which will lower the minimum slew rate requirement considerably. For example, with the addition of positive feedback components $R_f = 1k\Omega$ and $C_f = 10pF$, the minimum slew rate requirement can be reduced by a factor of 4.

The timing diagram (Figure 3) illustrates worst-case conditions in representing the series of events to complete the compare function.

The top line of the diagram illustrates 2 latch enable pulses. Each pulse is high for the compare function and low for the latch function. The first pulse demonstrates the compare function; part of the input action takes place during the compare mode. The second pulse demonstrates a compare function interval during which there is no change in the input.

The leading edge of the input signal, illustrated as a large amplitude, small overdrive pulse, switches the comparator after time interval t_{pd} . Output Q and \bar{Q} transistors are essentially similar in timing. The input signal must occur at time t_s before the latch falling edge, and it must be maintained for the time t_h after the edge to be acquired. After t_h , the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of $t_{pw}(E)$ is needed for the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.

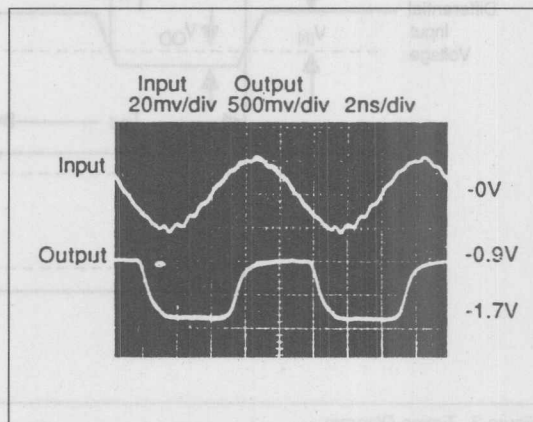


Figure 2. As a high-speed receiver, the MAX9685 is capable of processing signals in excess of 600MHz. Figure 2 is a 100MHz example with an input signal level of 14mVrms.

Ultra-Fast ECL Output Comparator with Latch Enable

Definition of Terms

V_{OS}	Input Offset Voltage -- The voltage required between the input terminals to obtain 0V differential at the output.	$t_{pd-}(E)$	Latch Enable to Output Low Delay -- The propagation delay measured from the 50% point of the Latch Enable signal low to high transition to the 50% point of an output high to low transition.
V_{IN}	Input Voltage Pulse Amplitude	$t_{pw}(E)$	Minimum Latch Enable Pulse Width -- The minimum time the Latch Enable signal must be high to acquire and hold an input signal.
V_{OD}	Input Voltage Overdrive	t_s	Minimum Setup Time -- The minimum time before the negative transition of the Latch Enable pulse that an input signal must be present to be acquired and held at the outputs.
t_{pd+}	Input to Output High Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low to high transition.	t_h	Minimum Hold Time -- The minimum time after the negative transition of the Latch Enable signal that an input signal must remain unchanged to be acquired and held at the output.
t_{pd-}	Input to Output Low Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high to low transition.		
$t_{pd+}(E)$	Latch Enable to Output High Delay -- The propagation delay measured from the 50% point of the Latch Enable signal low to high transition to the 50% point of an output low to high transition.		

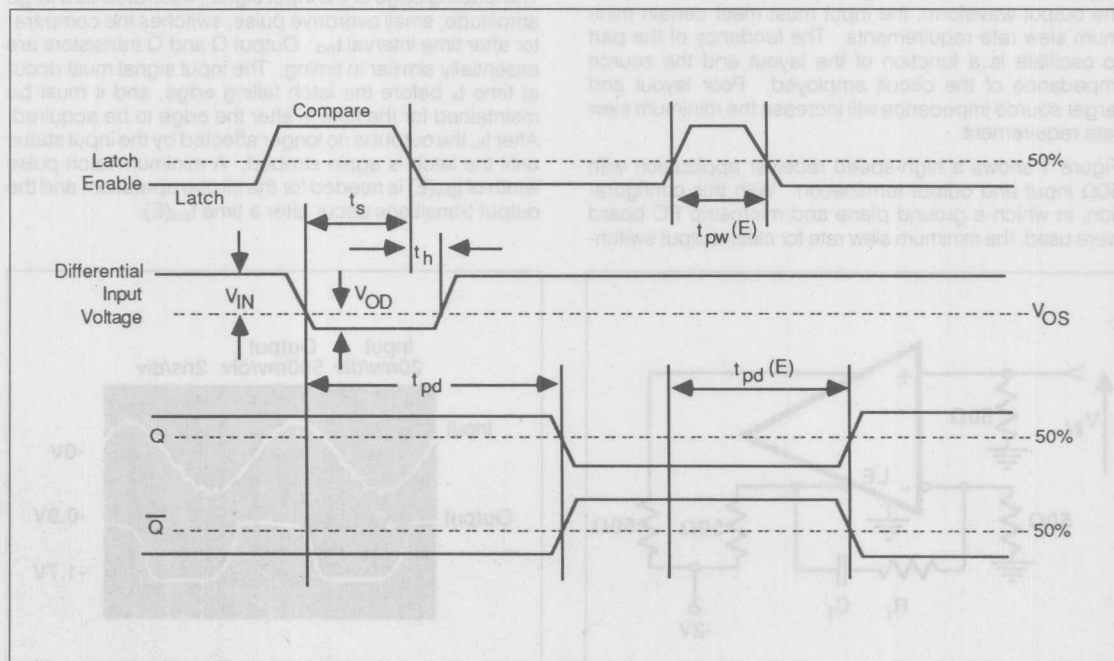


Figure 3. Timing Diagram.

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Very Fast TTL Latched Output Comparators

General Description

The MAX9686 (Single) and MAX9698 (Dual) are very fast latched TTL comparators manufactured with a high-frequency bipolar process ($f_T = 6\text{GHz}$). They are capable of very short propagation delays, yet maintain the excellent DC characteristics normally found only in slower comparators. The MAX9698 is a dual version of the MAX9686.

The MAX9686 is pin compatible with the LT1016 and Am686, but exceeds the AC characteristics of these devices.

The MAX9686/MAX9698 have differential inputs and complementary outputs that are fully compatible with TTL logic levels. Extremely short propagation delays allow signal processing at frequencies in excess of 200MHz.

When the Latch Enable input goes high, the outputs go to the states defined by the inputs at the time of the latch transition. The outputs remain latched as long as the LE pin remains high. If Latch Enable is not used, LE is tied to ground.

Applications

- High-Speed A/D Converters
- High-Speed Line Receivers
- Peak Detectors
- Threshold Detectors
- High-Speed Triggers

Features

- ◆ 6ns Propagation Delay
- ◆ 2ns Latch Setup Time
- ◆ $\pm 5\text{V}$ Power Supplies
- ◆ Pin Compatible to LT1016, Am686 (MAX9686)
- ◆ Available in Commercial and Military Temp. Ranges
- ◆ Available in Narrow SO Package

Ordering Information

PART	TEMP. RANGE	PIN - PACKAGE*
MAX9686BCPA	0°C to +70°C	8 Plastic DIP
MAX9686BCSA	0°C to +70°C	8 Narrow SO
MAX9686CJA	0°C to +70°C	8 CERDIP
MAX9686BC/D	0°C to +70°C	Dice**
MAX9686CTW	0°C to +70°C	10 TO-100 Can
MAX9686MJA	-55°C to +125°C	8 CERDIP
MAX9686MTW	-55°C to +125°C	10 TO-100 Can
MAX9698BCPE	0°C to +70°C	16 Plastic DIP
MAX9698BCSE	0°C to +70°C	16 Narrow SO
MAX9698CJE	0°C to +70°C	16 CERDIP
MAX9698BC/D	0°C to +70°C	Dice**
MAX9698MJE	-55°C to +125°C	16 CERDIP

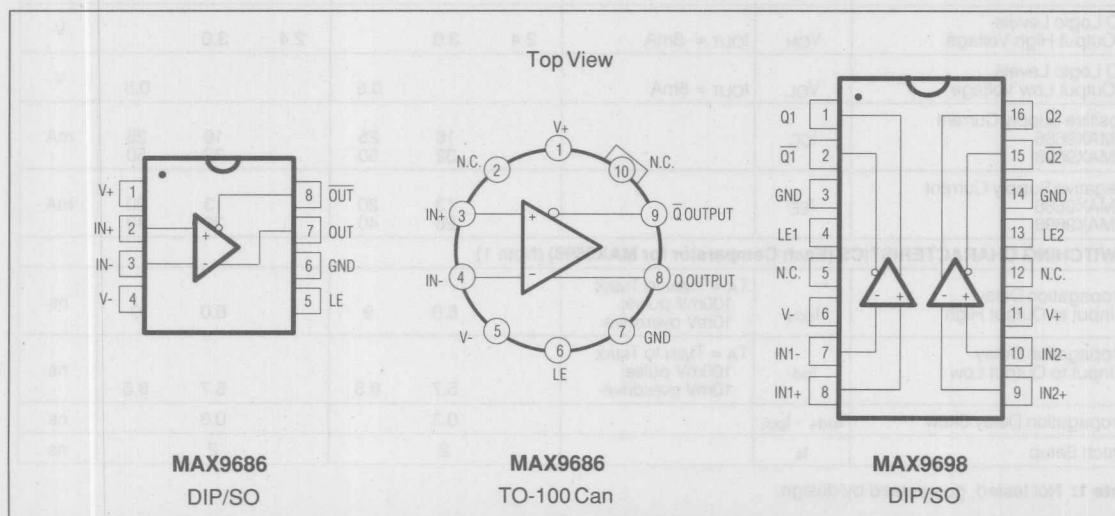
* Contact factory for availability of 20-Pin LCC

** Contact factory for dice specifications.

MAX9686/MAX9698

4

Pin Configurations



Very Fast Latched TTL Output Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6V
Input Voltages	±5V
Differential Input Voltages	3.5V
Output Current	20mA
Operating Temperature Range:	
Commercial (MAX9686C/9698C)	0°C to +70°C
Military (MAX9686M/9698M)	-55°C to +125°C

Continuous Total Power Dissipation at 70°C:	
8-Pin Plastic DIP (derate 8.3mW/°C above 70°C)	660mW
8-Pin SO (derate 5.9mW/°C above 70°C)	470mW
8-Pin Cerdip (derate 8.0mW/°C above 70°C)	640mW
16-Pin Plastic DIP (derate 7.4mW/°C above 70°C)	590mW
16-Pin SO (derate 9.1mW/°C above 70°C)	727mW
16-Pin Cerdip (derate 10mW/°C above 70°C)	800mW
Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±5V, T_A = 25°C, unless otherwise noted.)

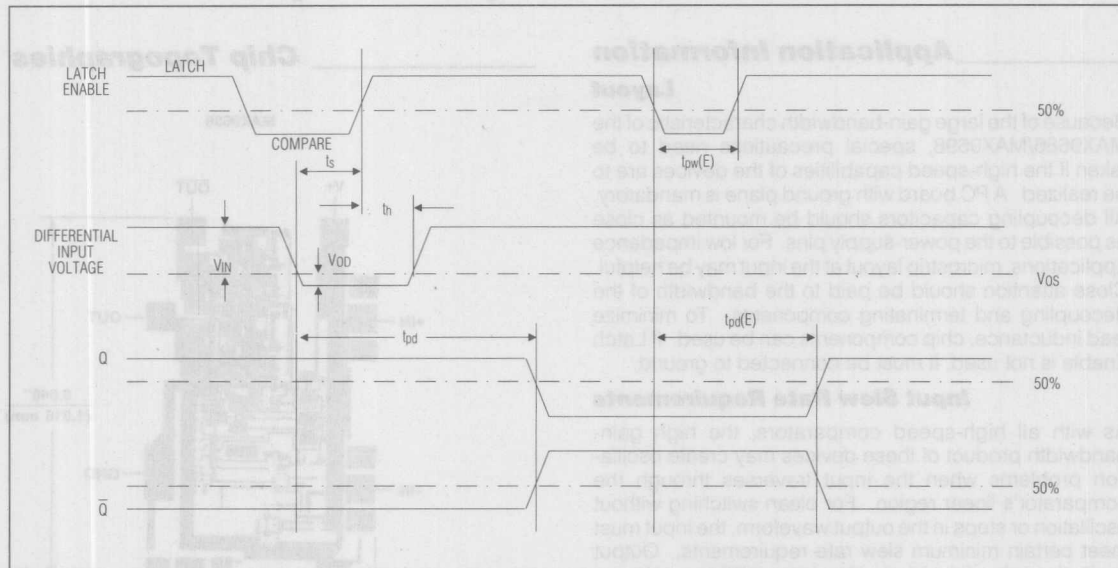
PARAMETER	SYMBOL	CONDITIONS	MAX9686C/9698C			MAX9686M/9698M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage MAX96__J_, MAX9686_TW MAX96__BC_	V _{OS}	R _S = 100Ω		±1 ±6	±3 ±9		±1 ±6	±3 ±9	mV
Temperature Coefficient	ΔV _{OS} /ΔT			4			4		μV/°C
Input Offset Current	I _{OS}				5.0			5.0	μA
Input Bias Current	I _B				25			25	μA
Common-Mode Rejection Ratio	CMRR		80	96		80	96		dB
Power-Supply Rejection Ratio MAX96__J_, MAX9686_TW MAX96__BC_	PSRR		70 50	85 65		70 50	85 65		dB
Input Voltage Range	V _{CM}				±3.0			±3.0	V
Latch High Input Voltage	V _{IH}		2.0			2.0			V
Latch Low Input Voltage	V _{IL}				0.8			0.8	V
Latch Low Input Current	I _{IL}	V _{LE} = 0V			-750			-750	μA
I/O Logic Levels Output High Voltage	V _{OH}	I _{OUT} = -3mA	2.4	3.0		2.4	3.0		V
I/O Logic Levels Output Low Voltage	V _{OL}	I _{OUT} = 8mA			0.5			0.5	V
Positive Supply Current MAX9686 MAX9698	I _{CC}			16 32	25 50		16 32	25 50	mA
Negative Supply Current MAX9686 MAX9698	I _{EE}			13 26	20 40		13 26	20 40	mA

SWITCHING CHARACTERISTICS (Each Comparator for MAX9698) (Note 1)

Propagation Delay Input to Output High	t _{pd+}	T _A = T _{MIN} to T _{MAX} 100mV pulse; 10mV overdrive		6.0	9		6.0	9	ns
Propagation Delay Input to Output Low	t _{pd-}	T _A = T _{MIN} to T _{MAX} 100mV pulse; 10mV overdrive		5.7	8.5		5.7	8.5	ns
Propagation Delay Skew	t _{pd+} - t _{pd-}			0.3			0.3		ns
Latch Setup	t _s			2			2		ns

Note 1: Not tested, guaranteed by design.

Very Fast Latched TTL Output Comparators



MAX9686 and MAX9698 Timing Diagram

Definition of Terms

V_{OS}	Input Offset Voltage	$t_{pd-(E)}$	Latch Enable to Output Low Delay -- The propagation delay measured from the 50% point of the Latch Enable signal high to low transition to the 50% point of an output high to low transition.
V_{OD}	Input Voltage Overdrive	$t_{pw(E)}$	Minimum Latch Enable Pulse Width -- The minimum time the Latch Enable signal must be low to acquire and hold an input signal.
t_{pd+}	Input to Output High Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low to high transition.	t_s	Minimum Setup Time -- The minimum time, before the positive transition of the Latch Enable pulse, that an input signal must be present to be acquired and held at the outputs.
t_{pd-}	Input to Output Low Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high to low transition.	t_h	Minimum Hold Time -- The minimum time, after the positive transition of the Latch Enable signal, that an input signal must remain unchanged to be acquired and held at the output.
$t_{pd+(E)}$	Latch Enable to Output High Delay -- The propagation delay measured from the 50% point of the Latch Enable signal high to low transition to the 50% point of an output low to high transition.		

Very Fast Latched TTL Output Comparators

Application Information

Layout

Because of the large gain-bandwidth characteristic of the MAX9686/MAX9698, special precautions need to be taken if the high-speed capabilities of the devices are to be realized. A PC board with ground plane is mandatory. All decoupling capacitors should be mounted as close as possible to the power-supply pins. For low impedance applications, microstrip layout at the input may be helpful. Close attention should be paid to the bandwidth of the decoupling and terminating components. To minimize lead inductance, chip components can be used. If Latch Enable is not used, it must be connected to ground.

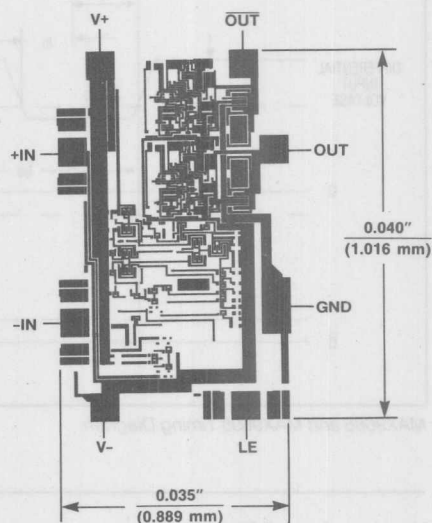
Input Slew Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices may create oscillation problems when the input traverses through the comparator's linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew rate requirements. Output oscillation is best avoided with compact PC board layout and minimum input signal source impedance. Poor layout and larger source impedance will increase the minimum slew rate required to avoid oscillation.

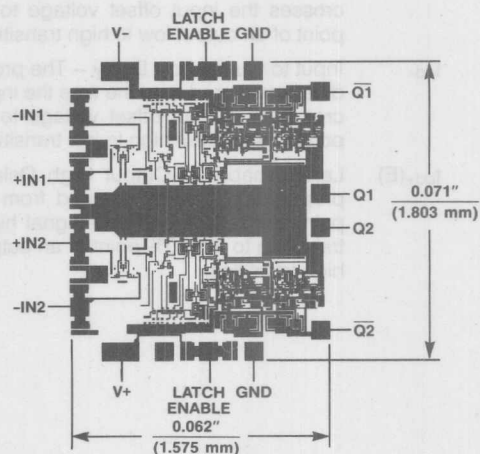
In many applications, the addition of regenerative feedback will assist the input signal through the linear region, which will lower the minimum slew rate requirement considerably. For example, the minimum slew rate can be reduced by a factor of 4 with the addition of positive feedback components $R_f = 1k\Omega$ and $C_f = 100pF$.

Chip Topographies

MAX9686



MAX9698



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Dual Ultra-Fast ECL Output Comparator

General Description

The MAX9687 is a dual ultra-fast ECL comparator manufactured with a high-frequency bipolar process ($f_T = 6\text{GHz}$) that is capable of very short propagation delays, maintaining the excellent DC matching characteristics normally found only in slower comparators.

The device is pin compatible with the AD9687 and Am6687, but it exceeds the AC characteristics of these devices.

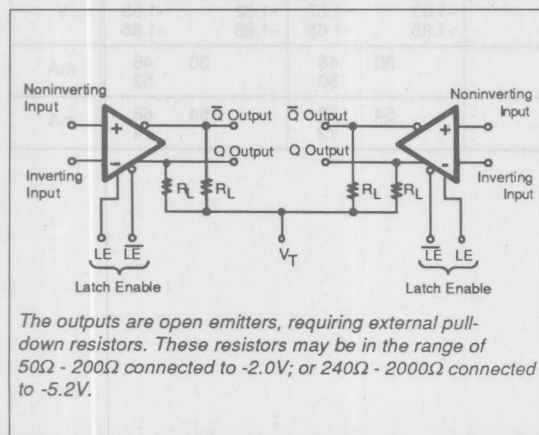
The MAX9687 has differential inputs and complementary outputs fully compatible with ECL logic levels. Output current levels are capable of driving 50Ω terminated transmission lines. The ultra-fast operation makes signal processing possible at frequencies in excess of 600MHz .

A Latch Enable function is provided to allow the comparator to be used in a sample-hold or track-hold mode. The Latch Enable inputs are designed to be driven from the complementary outputs of a standard ECL gate. When LE is high and $\overline{\text{LE}}$ is low, the comparator functions normally. When LE is forced low and $\overline{\text{LE}}$ high, the comparator outputs are locked in the logical states determined by the input conditions at the time of the latch transition. If the Latch Enable function is not used on either of the comparators, the appropriate LE input must be connected to ground; the companion $\overline{\text{LE}}$ input can be left open.

Applications

- High-Speed A/D Converters
- High-Speed Line Receivers
- Peak Detectors
- Threshold Detectors
- High-Speed Triggers

Functional Diagram



Features

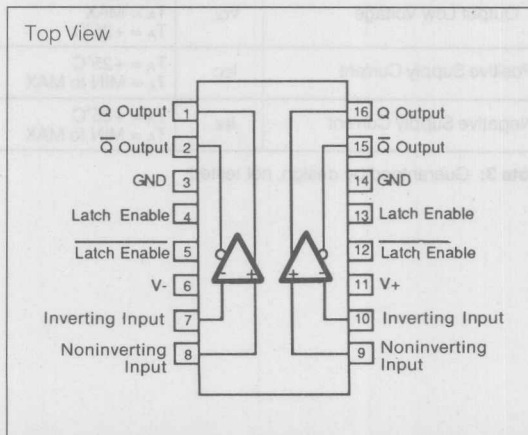
- ◆ 1.4ns Propagation Delay
- ◆ 0.5ns Latch Setup Time
- ◆ 2.0ns Latch Enable Pulse Width
- ◆ $+5\text{V}$, -5.2V Power Supplies
- ◆ Pin Compatible with AD9687, Am6687, SP9687
- ◆ Available in Commercial and Military Temp. Ranges
- ◆ Available in Narrow SO Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE*
MAX9687CPE	0°C to $+70^\circ\text{C}$	16 Plastic DIP
MAX9687CSE	0°C to $+70^\circ\text{C}$	16 Narrow SO
MAX9687CJE	0°C to $+70^\circ\text{C}$	16 CERDIP
MAX9687C/D	0°C to $+70^\circ\text{C}$	Dice
MAX9687MJE	-55°C to $+125^\circ\text{C}$	16 CERDIP

*Contact factory for availability of 20-Pin LCC

Pin Configuration



Dual Ultra-Fast ECL Output Comparator

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6V
Power Dissipation (Notes 1, 2)	700mW
Output Short-Circuit Duration (Note 2)	Indefinite
Input Voltages	±5V
Differential Input Voltages	3.5V
Output Current	30mA

Note 1: Power derating above $T_A = 70^\circ\text{C}$ is based on a maximum junction temperature of 150°C and the thermal resistance factors of $\theta_{JC} = 75^\circ\text{C/W}$ and $\theta_{JA} = 145^\circ\text{C/W}$. For SO package, $\theta_{JC} = 60^\circ\text{C/W}$ and $\theta_{JA} = 110^\circ\text{C/W}$.

Note 2: Continuous short-circuit protection is allowed on 1 comparator per time up to case temperatures of 85°C and ambient temperatures of 30°C .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

($V_+ = +5\text{V}$, $V_- = -5.2\text{V}$, $V_T = -2.0\text{V}$, $R_L = 50\Omega$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX9687C			MAX9687M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$ $T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$	-5 -7		+5 +7	-5 -8		+5 +8	mV
Temperature Coefficient	$\Delta V_{OS}/\Delta T$			10			15		$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$			5 8			5 12	μA
Input Bias Current	I_B	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$		10	20 30		10	20 40	μA
Input Voltage Range	V_{CM}	(Note 3)	-2.5		+2.5	-2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR		80			80			dB
Power-Supply Rejection Ratio	PSRR		60			60			dB
Input Resistance	R_{IN}	(Note 3)	60			60			$k\Omega$
Input Capacitance	C_{IN}		3			3			pF
I/O Logic Levels									
Output High Voltage	V_{OH}	$T_A = \text{MIN}$ $T_A = \text{MAX}$ $T_A = +25^\circ\text{C}$	-1.05 -0.89 -0.96		-0.87 -0.70 -0.81	-1.16 -0.88 -0.96		-0.89 -0.69 -0.81	V
Output Low Voltage	V_{OL}	$T_A = \text{MIN}$ $T_A = \text{MAX}$ $T_A = +25^\circ\text{C}$	-1.89 -1.83 -1.85		-1.65 -1.57 -1.65	-1.90 -1.82 -1.85		-1.65 -1.55 -1.65	V
Positive Supply Current	I_{CC}	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$		30	46 50		30	46 52	mA
Negative Supply Current	I_{EE}	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$		54	68 72		54	68 74	mA

Note 3: Guaranteed by design, not tested.

Dual Ultra-Fast ECL Output Comparator

MAX9687

SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MAX9687C			MAX9687M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input to Output High (Notes 3 and 4)	t_{pd+}	$T_A = +25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		1.4	1.9		1.4	1.9	ns
				1.6	2.2		1.7	2.6	
Input to Output Low (Notes 3 and 4)	t_{pd-}	$T_A = +25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		1.4	1.9		1.4	1.9	ns
				1.6	2.2		1.9	2.6	
Latch Enable to Output High (Notes 3 and 4)	$t_{pd+}(E)$	$T_A = +25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		1.3	1.8		1.3	1.8	ns
				1.4	2.0		1.5	2.0	
Latch Enable to Output Low (Notes 3 and 4)	$t_{pd-}(E)$	$T_A = +25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		1.3	1.8		1.3	1.8	ns
				1.4	1.9		1.7	2.6	
Latch Enable (Note 3) Pulse Width	$t_{pw}(E)$		3.0	2.0		3.0	2.0		
Min Setup Time	t_s			0.5	1.0		0.5	1.0	ns
Min Hold Time	t_h			0.5	1.0		0.5	1.0	

Note 4: $V_{IN} = 100\text{mV}$, $V_{OD} = 10\text{mV}$.

Application Information

Layout

Because of the large gain-bandwidth characteristic of the MAX9687, special precautions need to be taken if the high-speed capabilities of the device are to be utilized. A PC board with ground plane should be considered mandatory. All decoupling capacitors should be mounted as close as possible to the power-supply pins and the ECL outputs processed in microstrip fashion consistent with the load termination of 50Ω to 120Ω . For low impedance applications, microstrip layout at the input may also be helpful. Close attention should be paid to the bandwidth of the decoupling and terminating components. Chip components to minimize lead inductance can be used as an advantage here.

Input Slew Rate Requirement

As with all high-speed comparators, the high gain-bandwidth product of these devices creates oscillation problems when the input traverses through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew rate requirements. The tendency of the part to oscillate is a function of the layout and the source impedance of the circuit employed. Poor layout and larger source impedance will increase the minimum slew rate specification.

In many applications, the addition of regenerative feedback will assist the input signal through the linear region, which will lower the minimum slew rate requirement considerably. For example, with the addition of positive feedback components $R_f = 1\text{k}\Omega$ and $C_f = 10\text{pF}$, the minimum slew rate requirement can be reduced by a factor of 4.

Figure 1 shows a high-speed receiver application with 50Ω input and output termination. With this configuration, in which a ground plane and microstrip PC board were used, the minimum slew rate for clean output switching is $1.6\text{V}/\mu\text{s}$. Sine wave inputs, imply a minimum

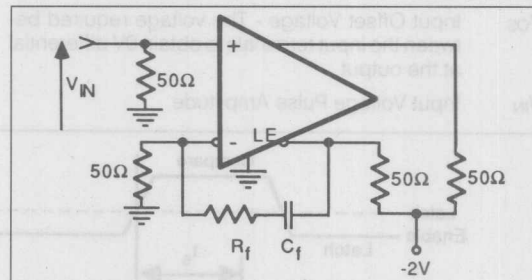


Figure 1. Regenerative Feedback. High-speed receiver with 50Ω input and output termination.

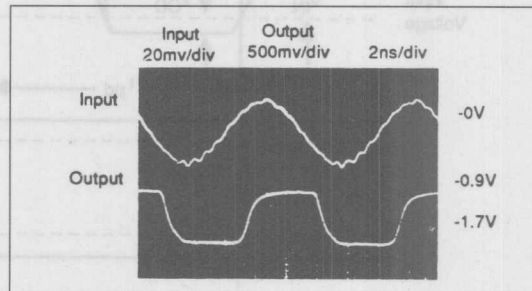


Figure 2. As a high-speed receiver, the MAX9687 is capable of processing signals in excess of 600MHz . Figure 2 is a 100MHz example with an input signal level of 14mV_{rms} .

Dual Ultra-Fast ECL Output Comparator

signal size of 360mVrms at 500kHz and 90mV at 2MHz.

$$E_{RMS} = \frac{\text{SlewRate}}{2\sqrt{2}\pi f}$$

The timing diagram (Figure 3) illustrates worst-case conditions in representing the series of events to complete the compare function.

The top line of the diagram illustrates 2 Latch Enable pulses. Each pulse is high for the compare function and low for the latch function. The first pulse demonstrates the compare function; part of the input action takes place during the compare mode. The second pulse demonstrates a compare function interval during which there is no change in the input.

The leading edge of the input signal, illustrated as a large amplitude, small overdrive pulse, switches the comparator after time interval t_{pd} . Outputs Q and \bar{Q} are essentially similar in timing. The input signal must occur at time t_s before the latch falling edge, and it must be maintained for time t_h after the edge to be acquired. After t_h , the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of $t_{pw}(E)$ is needed for the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.

Definition of Terms

V_{OS} Input Offset Voltage - The voltage required between the input terminals to obtain 0V differential at the output.

V_{IN} Input Voltage Pulse Amplitude

V_{OD} Input Voltage Overdrive

t_{pd+} Input to Output High Delay - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low to high transition.

t_{pd-} Input to Output Low Delay - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high to low transition.

t_{pd+(E)} Latch Enable to Output High Delay - The propagation delay measured from the 50% point of the Latch Enable signal low to high transition to the 50% point of an output low to high transition.

t_{pd-(E)} Latch Enable to Output Low Delay - The propagation delay measured from the 50% point of the Latch Enable signal low to high transition to the 50% point of an output high to low transition.

t_{pw(E)} Minimum Latch Enable Pulse Width - The minimum time the Latch Enable signal must be high to acquire and hold an input signal.

t_s Minimum Setup Time - The minimum time before the negative transition of the Latch Enable pulse that an input signal must be present to be acquired and held at the outputs.

t_h Minimum Hold Time - The minimum time after the negative transition of the Latch Enable signal that an input signal must remain unchanged to be acquired and held at the outputs.

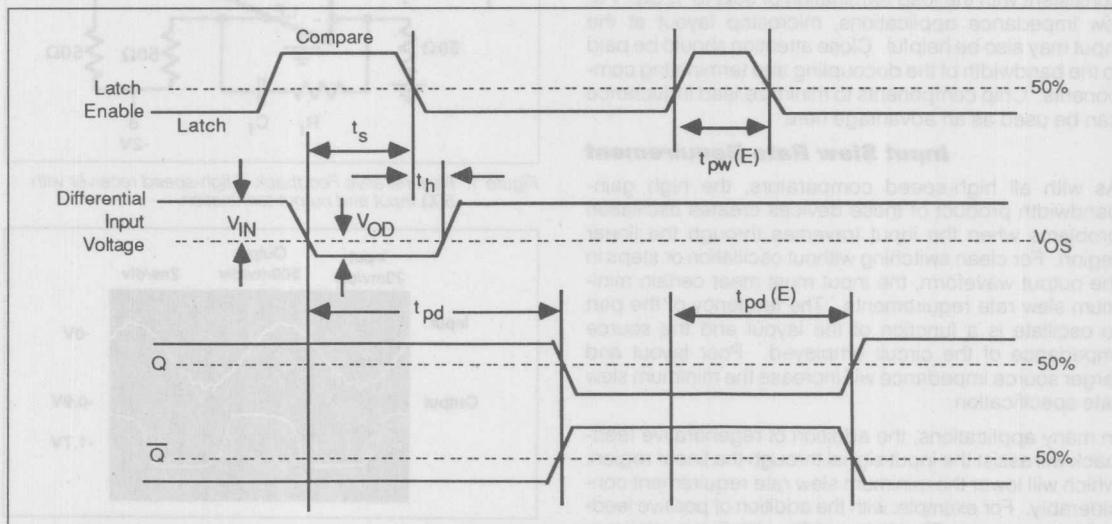


Figure 3. Timing Diagram

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Ultra-Fast ECL Output Comparator

MAX9690

General Description

The MAX9690 is an ultra-fast ECL comparator manufactured with a high-frequency bipolar process ($f_T = 6\text{GHz}$) which is capable of very short propagation delays, while maintaining the excellent DC matching characteristics normally found only in slower comparators. The device is similar in function to the MAX9685, except the Latch Enable input is eliminated.

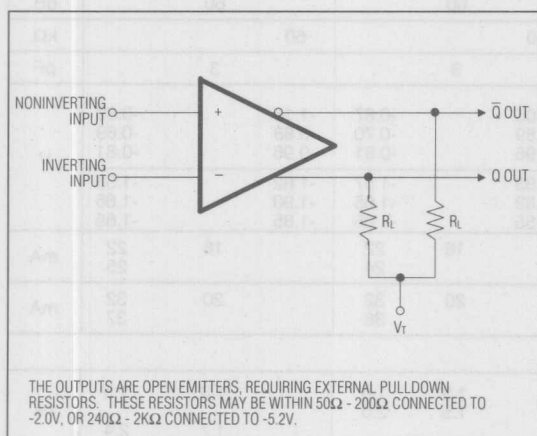
The device is pin compatible with the CMP-08, but it exceeds the AC characteristics of that device.

The MAX9690 has differential inputs and complementary outputs fully compatible with ECL logic levels. Output current levels are capable of driving 50Ω terminated transmission lines. Ultra-fast operation makes signal processing possible at frequencies in excess of 600MHz .

Applications

High-Speed A/D Converters
High-Speed Line Receivers
Peak Detectors
Threshold Detectors

Functional Diagram



Features

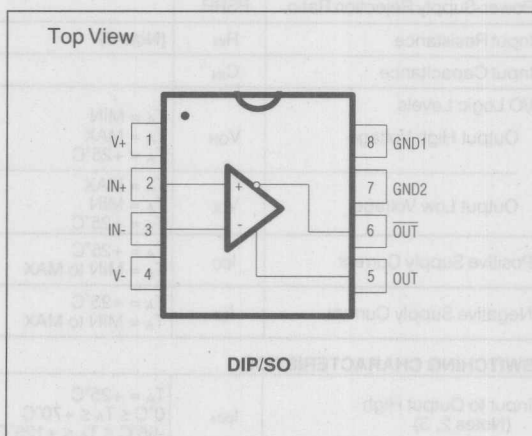
- ◆ 1.3ns Propagation Delay
- ◆ +5V, -5.2V Power Supplies
- ◆ Pin Compatible to CMP-08
- ◆ Available in Commercial and Military Temp. Ranges
- ◆ Available in Narrow SO Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9690CPA	0°C to $+70^\circ\text{C}$	8 Plastic DIP
MAX9690CSA	0°C to $+70^\circ\text{C}$	8 Narrow SO
MAX9690CJA	0°C to $+70^\circ\text{C}$	8 CERDIP
MAX9690C/D	0°C to $+70^\circ\text{C}$	Dice
MAX9690MJA	-55°C to $+125^\circ\text{C}$	8 CERDIP

*Contact factory for availability of 20-pin LCC.

Pin Configuration



4

Ultra-Fast ECL Output Comparator

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±6V
Power Dissipation (Note 1)	336mW
Input Voltages	±5V
Differential Input Voltages	3.5V
Output Current	30mA

Note 1: Power derating above $T_A = 70^\circ\text{C}$ is based on a maximum junction temperature of 150°C and the following thermal resistance factors:

Operating Temperature Range:

Commercial (MAX9690C)	0°C to $+70^\circ\text{C}$
Military (MAX9690M)	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-55°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE	$\theta_{JC} (^{\circ}\text{C}/\text{W})$	$\theta_{JA} (^{\circ}\text{C}/\text{W})$
DIP	75	180
Narrow SO	115	180

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

($V_+ = 5\text{V}$, $V_- = -5.2\text{V}$, $R_L = 50\Omega$, $V_T = -2\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX9690C			MAX9690M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$	-5 -7		+5 +7	-5 -8		+5 +8	mV
Temperature Coefficient	$\Delta V_{OS}/\Delta T$		10			15			$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$			5 8			5 12	μA
Input Bias Current	I_B	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$		10	20 30		10	20 40	μA
Input Voltage Range	V_{CM}	(Note 2)	-2.5		+2.5	-2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR		80			80			dB
Power-Supply Rejection Ratio	PSRR		60			60			dB
Input Resistance	R_{IN}	(Note 2)	60			60			$\text{k}\Omega$
Input Capacitance	C_{IN}		3			3			pF
I/O Logic Levels									
Output High Voltage	V_{OH}	$T_A = \text{MIN}$ $T_A = \text{MAX}$ $T_A = +25^\circ\text{C}$	-1.05 -0.89 -0.96		-0.87 -0.70 -0.81	-1.16 -0.88 -0.96		-0.89 -0.69 -0.81	V
Output Low Voltage	V_{OL}	$T_A = \text{MAX}$ $T_A = \text{MIN}$ $T_A = +25^\circ\text{C}$	-1.83 -1.89 -1.85		-1.57 -1.65 -1.65	-1.82 -1.90 -1.85		-1.55 -1.65 -1.65	
Positive Supply Current	I_{CC}	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$		16	22 24		16	22 25	mA
Negative Supply Current	I_{EE}	$T_A = +25^\circ\text{C}$ $T_A = \text{MIN to MAX}$		20	32 36		20	32 37	mA

SWITCHING CHARACTERISTICS

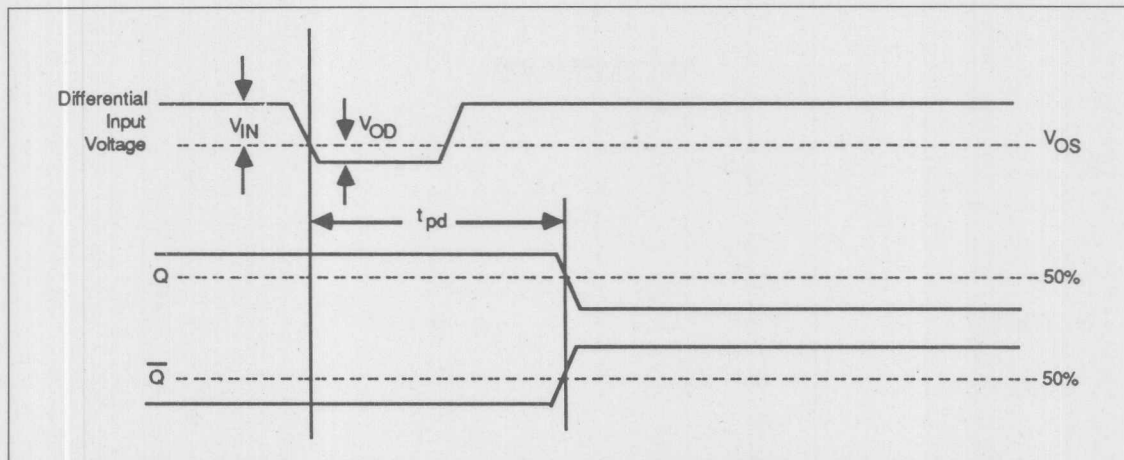
Input to Output High (Notes 2, 3)	t_{pd+}	$T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	1.3 1.5	1.8 2.0	1.3 1.7	1.8 2.4	ns
Input to Output Low (Notes 2, 3)	t_{pd-}	$T_A = +25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	1.3 1.5	1.8 2.0	1.3 1.7	1.8 2.4	ns

Note 2: Guaranteed by design, not tested.

Note 3: $V_{IN} = 100\text{mV}$, $V_{OD} = 10\text{mV}$.

Ultra-Fast ECL Output Comparator

MAX9690



Timing Diagram

Timing Diagram

The timing diagram illustrates worst-case conditions in representing the series of events to complete the compare function.

The leading edge of the input signal, illustrated as a large amplitude, small overdrive pulse, switches the comparator. Outputs \bar{Q} and Q are essentially similar in timing.

Definition of Terms

V_{OS}	Input Offset Voltage -- The voltage required between the input terminals to obtain 0V differential at the output.
V_{IN}	Input Voltage Pulse Amplitude
V_{OD}	Input Voltage Overdrive
t_{pd+}	Input to Output High Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output low to high transition.
t_{pd-}	Input to Output Low Delay -- The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output high to low transition.

Application Information

Layout

Because of the large gain-bandwidth characteristic of the MAX9690, special precautions need to be taken if the high-speed capabilities of the device are to be utilized. A PC board with ground plane should be considered mandatory. All decoupling capacitors should be mounted as close as possible to the power-supply pins, and the ECL outputs should be processed in microstrip fashion consistent with the load termination of 50Ω to 120Ω . For low impedance applications, microstrip layout at the input may also be helpful. Close attention should be paid to the bandwidth of the decoupling and terminating components. Chip components to minimize lead inductance can be used as an advantage here.

Input Slew Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices creates oscillation problems when the input traverses through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew rate requirements. The tendency of the part to oscillate is a function of the layout and the source impedance of the circuit employed. Poor layout and larger source impedance will increase the minimum slew rate requirement.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

ADVANCE INFORMATION

FIRST SHEET OF DATA SHEET IN PREPARATION

MAXIM

High-Speed, Low-Power Op Amps

General Description

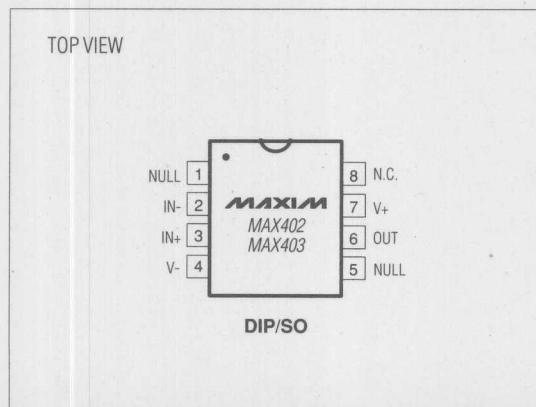
The MAX402/MAX403 are high-speed, low-power op amps fabricated with Maxim's high-frequency Complementary Bipolar (CB) process. The MAX402 draws less than 60 μ A of supply current while maintaining an 8V/ μ s (typical) slew rate and a 2MHz (typical) bandwidth. For applications requiring increased speed, the MAX403 draws a maximum supply current of 300 μ A and offers a 50V/ μ s (typical) slew rate and a 10MHz (typical) bandwidth. Both op amps are unity gain stable.

The combination of high-speed performance and low-power operation, unobtainable in existing op amps, makes the MAX402/MAX403 ideal for high-speed, battery-powered applications.

Applications

Low-Power Signal Processing
Portable Instruments
Remote Sensors

Pin Description



Features

- ◆ Low-Power Consumption:
MAX402: 0.6mW Max
MAX403: 3.0mW Max
- ◆ High Speed:
MAX402: 5V/ μ s Min
MAX403: 25V/ μ s Min
- ◆ Unity Gain Stable
- ◆ Single-Supply Capability
- ◆ Wide Unity Gain Bandwidth:
MAX402: 1.4MHz Min
MAX403: 7MHz Min

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX402CPA	0°C to +70°C	8 Plastic DIP
MAX402CSA	0°C to +70°C	8 Narrow SO
MAX402C/D	0°C to +70°C	Dice*
MAX402EPA	-40°C to +85°C	8 Plastic DIP
MAX402EJA	-40°C to +85°C	8 CERDIP
MAX402MJA	-55°C to +125°C	8 CERDIP
MAX403CPA	0°C to +70°C	8 Plastic DIP
MAX403CSA	0°C to +70°C	8 Narrow SO
MAX403C/D	0°C to +70°C	Dice*
MAX403EPA	-40°C to +85°C	8 Plastic DIP
MAX403EJA	-40°C to +85°C	8 CERDIP
MAX403MJA	-55°C to +125°C	8 CERDIP

*Consult factory for dice specifications.

MAX402/MAX403

4

MAXIM

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Maxim Integrated Products 4-17

Single/Dual/Quad High-Speed, Fast-Settling, High Output Current Operational Amplifier

General Description

The MAX408/428/448 are high speed general purpose monolithic operational amplifiers in a single, dual or quad package, that are useful for signal frequencies extending into the video range. These Op Amps function in gain configurations greater-than or equal-to 3. High output current allows large capacitive loads to be driven at high speeds.

Open-loop voltage gain of 10k V/V and high slew rate of 90V/ μ s make the MAX408/428/448 ideal for analog amplification and high speed signal processing. 100MHz gain bandwidth and a $\pm 0.1\%$ settling time of 150ns make each amplifier ideal for fast data conversion systems.

± 50 mA output current capability allows the amplifiers to drive terminated transmission lines of 50 Ω with amplitudes of 5V peak-to-peak.

Along with the high speed and output drive capability, a 35nA offset current and trimmable offset voltage make the MAX408/428/448 optimal for signal conditioning applications where accuracy must be maintained.

Applications

Video Amplifiers
Test Equipment
Waveform Generators
Video Distribution
Pulse Amplifiers

Features

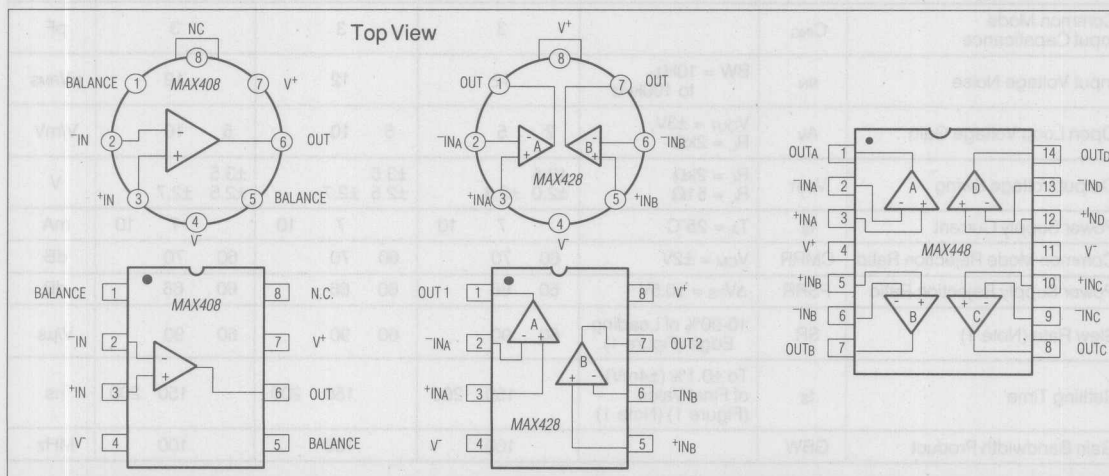
- ◆ Fast Settling Time: $\pm 0.1\%$ in 150ns
- ◆ High Slew Rate: 90V/ μ s
- ◆ Large Gain Bandwidth: 100MHz
- ◆ Full Power Bandwidth: 4.8MHz at 6V p-p
- ◆ Ease of Use: Internally Compensated for $A_{CL} \geq 3$ with 50° - 60° Phase Margin
- ◆ Large Output Current: ± 50 mA
- ◆ Low Supply Voltage Operation: ± 4 V
- ◆ Wide Input Voltage Range: Within 1.5V of V^+ and 0.5V of V^-
- ◆ Minimal Crosstalk: >90dB Separation (MAX428/448)
- ◆ Short Circuit Protection

Ordering Information

PART	TEMP. RANGE	PACKAGE*
MAX408ACPA	0°C to +70°C	8 Lead Plastic DIP
MAX408ACJA	0°C to +70°C	8 Lead Cerdip
MAX408ACSA	0°C to +70°C	8 Lead Small Outline
MAX408ACTV	0°C to +70°C	8 Lead TO-99 Metal Can
MAX408CPA	0°C to +70°C	8 Lead Plastic DIP
MAX408CJA	0°C to +70°C	8 Lead Cerdip
MAX408CSA	0°C to +70°C	8 Lead Small Outline
MAX408CTV	0°C to +70°C	8 Lead TO-99 Metal Can
MAX408C/D	0°C to 70°C	Dice
MAX408MJA	-55°C to +125°C	8 Lead Cerdip
MAX408MTV	-55°C to +125°C	8 Lead TO-99 Metal Can

(Ordering Information continued on last page.)
*Contact factory for availability of 20 Lead LCC

Pin Configurations



Single/Dual/Quad High Speed, Fast Settling, High Output Current Operational Amplifier

ABSOLUTE MAXIMUM RATINGS - MAX408

Supply Voltages	±6V
Differential Input Voltage	±9V
Common Mode Input Voltage	$V_{ISL} - 0.5V$
Power Dissipation (Note 1)	450mW
Output Short Circuit Current Duration (Note 2)	Indefinite

Note 1: Power derating above $T_A = 70^\circ\text{C}$ to be based on a maximum junction temperature of 150°C and the thermal resistance factors in the chart below

PKG	$\theta_{JC} (^{\circ}\text{C/W})$	$\theta_{JA} (^{\circ}\text{C/W})$	$T_C (^{\circ}\text{C})$	$T_A (^{\circ}\text{C})$
DIP, CERDIP	75	180	110	70
SOIC	115	180	95	70
TO-99	115	150	95	30

Operating Temperature Range:

Commercial (MAX408AC, C)	0°C to $+70^\circ\text{C}$
Military (MAX408M)	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 seconds)	300°C

Note 2: Continuous short circuit protection is allowed for the case and ambient temperatures in the chart below.

ELECTRICAL CHARACTERISTICS - MAX408 ($V_S = \pm 5V$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX408C			MAX408AC			MAX408M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	5	12		3	6		3	6		mV
			8	16		5	10		6	12		
Average Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	20			20			15			$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B		650	1100		650	1100		650	1100		nA
Input Offset Current	I_{OS}	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	35	120		35	120		35	120		nA
			70	200		70	200		70	300		
Input Common Mode Range	V_{CM}		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		V
Differential Input Resistance	R_{IND}	(Note 1)	3	10		3	10		3	10		$\text{M}\Omega$
Common Mode Input Resistance	R_{INC}	(Note 1)	4	8		4	8		4	8		$\text{M}\Omega$
Differential Input Capacitance	C_{IND}		2			2			2			pF
Common Mode Input Capacitance	C_{INC}		3			3			3			pF
Input Voltage Noise	e_N	$\text{BW} = 10\text{Hz}$ to 100kHz	12			12			12			μV_{RMS}
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm 3V$, $R_L = 2\text{k}\Omega$	2	5		5	10		5	10		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2\text{k}\Omega$ $R_L = 51\Omega$	± 3.5 ± 2.0	± 2.4		± 3.5 ± 2.5	± 2.7		± 3.5 ± 2.5	± 2.7		V
Power Supply Current	I_S	$T_A = 25^\circ\text{C}$	7	10		7	10		7	10		mA
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2V$	60	70		60	70		60	70		dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm 0.5V$	60	66		60	66		60	66		dB
Slew Rate (Note 1)	SR	10-90% of Leading Edge (Figure 1)	60	90		60	90		60	90		V/ μs
Settling Time	t_s	To $\pm 0.1\%$ ($\pm 4\text{mV}$) of Final Value (Figure 1) (Note 1)	150	200		150	200		150	200		ns
Gain Bandwidth Product	GBW		100			100			100			MHz

Note 1: Not tested, guaranteed by design.

Single/Dual/Quad High Speed, Fast Settling, High Output Current Operational Amplifier

ABSOLUTE MAXIMUM RATINGS - MAX428

Supply Voltages	±6V
Differential Input Voltage	±9V
Common Mode Input Voltage	IVS-1.0V
Power Dissipation (Note 1)	450mW
Output Short Circuit Current Duration (Note 2)	Indefinite

Note 1: Power derating above $T_A = 70^\circ\text{C}$ to be based on a maximum junction temperature of 150°C and the following thermal resistance factors:

PKG	$\theta_{JC} (^{\circ}\text{C}/\text{W})$	$\theta_{JA} (^{\circ}\text{C}/\text{W})$
DIP	75	180
TO-99	115	150

Operating Temperature Range:

Commercial (MAX428AC, C)	0°C to $+70^\circ\text{C}$
Military (MAX428M)	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 seconds)	300°C

Note 2: Continuous short circuit protection is allowed on one amplifier per time up to the following case and ambient temperatures:

PKG	$T_C (^{\circ}\text{C})$	$T_A (^{\circ}\text{C})$
DIP	100	30
TO-99	75	(Note 3)

Note 3: Long duration shorts (>5 sec) will result in junction temperature exceeding 150°C which may result in part damage.

ELECTRICAL CHARACTERISTICS - MAX428 ($V_S = \pm 5\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX428C			MAX428AC			MAX428M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	5	12		3	6		3	6		mV
			8	16		5	10		6	12		
Average Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	20			20			15			$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	650	1100		650	1100		650	1100		mA
				1700			1700			1700		
										2200		
Input Offset Current	I_{OS}		35	120		35	120		35	120		nA
Input Common Mode Range	V_{CM}		+3	+3.5		+3	+3.5		+3	+3.5		V
			-4	-4.5		-4	-4.5		-4	-4.5		
Differential Input Resistance	R_{IND}	(Note 1)	3	10		3	10		3	10		$\text{M}\Omega$
Common Mode Input Resistance	R_{INC}	(Note 1)	4	8		4	8		4	8		$\text{M}\Omega$
Differential Input Capacitance	C_{IND}		2			2			2			pF
Common Mode Input Capacitance	C_{INC}		3			3			3			pF
Input Voltage Noise	e_N	$\text{BW} = 10\text{Hz}$ to 100kHz	12			12			12			μV_{RMS}
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm 3\text{V}$, $R_L = 2\text{k}\Omega$	2	5		5	10		5	10		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2\text{k}\Omega$ $R_L = 51\Omega$	± 3.5 ± 2.0	± 2.4		± 3.5 ± 2.5	± 2.7		± 3.5 ± 2.5	± 2.7		V
Power Supply Current	I_S	$T_A = 25^\circ\text{C}$	15	20		15	20		15	20		mA
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2\text{V}$	60	70		60	70		60	70		dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm 0.5\text{V}$	60	66		60	66		60	66		dB
Slew Rate (Note 1)	SR	10-90% of Leading Edge (Figure 1)	60	90		60	90		60	90		V/ μs
Settling Time	t_S	To $\pm 0.1\%$ ($\pm 4\text{mV}$) of Final Value (Figure 1) (Note 1)	150	200		150	200		150	200		ns
Gain Bandwidth Product	GBW		100			100			100			MHz

Note 1: Not tested, guaranteed by design.

Single/Dual/Quad High Speed, Fast Settling, High Output Current Operational Amplifier

ABSOLUTE MAXIMUM RATINGS - MAX448

Supply Voltages	±6V
Differential Input Voltage	±9V
Common Mode Input Voltage	IV _{sl} -0.5V
Power Dissipation (Note 1)	550mW
Output Short Circuit Current Duration (Note 2)	Indefinite

Note 1: Power derating above $T_A = 70^\circ\text{C}$ to be based on a maximum junction temperature of 150°C and the thermal resistance factors of $\theta_{JC} = 75^\circ\text{C/W}$ and $\theta_{JA} = 150^\circ\text{C/W}$.

Operating Temperature Range:

Commercial (MAX448AC, C)	0°C to $+70^\circ\text{C}$
Military (MAX448M)	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 seconds)	300°C

Note 2: Continuous short circuit protection is allowed on one amplifier per time up to case temperatures of 85°C and ambient temperatures of 30°C .

ELECTRICAL CHARACTERISTICS - MAX448 ($V_S = \pm 5\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX448C			MAX448AC			MAX448M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	5	12		3	6		3	6		mV
			8	16		5	10		6	12		
Average Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	20			20			15			$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	650	1100		650	1100		650	1100		nA
				1700			1700			2200		
Input Offset Current	I_{OS}		35	120		35	120		35	120		nA
Input Common Mode Range	V_{CM}		+3	+3.5		+3	+3.5		+3	+3.5		V
			-4	-4.5		-4	-4.5		-4	-4.5		
Differential Input Resistance	R_{IND}	(Note 1)	3	10		3	10		3	10		$\text{M}\Omega$
Common Mode Input Resistance	R_{INC}	(Note 1)	4	8		4	8		4	8		$\text{M}\Omega$
Differential Input Capacitance	C_{IND}		2						2			pF
Common Mode Input Capacitance	C_{INC}		3			3			3			pF
Input Voltage Noise	e_N	$\text{BW} = 10\text{Hz}$ to 100kHz	12			12			12			μVRMS
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm 3\text{V}$, $R_L = 2\text{k}\Omega$	2	5		4	10		4	10		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2\text{k}\Omega$ $R_L = 51\Omega$	± 3.5 ± 2.0	± 2.4		± 3.5 ± 2.5	± 2.7		± 3.5 ± 2.5	± 2.7		V
Power Supply Current (All four amplifiers)	I_S	$T_A = 25^\circ\text{C}$	30	40		30	40		30	40		mA
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm 0.5\text{V}$	60	66		60	66		60	66		dB
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2\text{V}$	60	70		60	70		60	70		dB
Slew Rate (Note 1)	SR	10-90% of Leading Edge (Figure 1)	60	90		60	90		60	90		V/ μs
Settling Time	t_S	To $\pm 0.1\%$ ($\pm 4\text{mV}$) of Final Value (Figure 1) (Note 1)	150	200		150	200		150	200		ns
Gain Bandwidth Product	GBW		100			100			100			MHz

Note 1: Not tested, guaranteed by design.

Single/Dual/Quad High Speed, Fast Settling, High Output Current Operational Amplifier

AC CHARACTERISTICS - MAX408/428/448 ($V_S = \pm 5V$, $T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MAX4XXC			MAX4XXAC			MAX4XXM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Small Signal Rise/Fall Time	t_r/t_f	$e_o = \pm 100mV$ 10-90% (Figure 1)	7			7			7			ns
Full Power Bandwidth	BW_{FP}	$R_L = 2k\Omega$, $C_L = 50pF$ $V_{OUT} = 6V_{p-p}$	4.8			4.8			4.8			MHz
Amp-Amp Crosstalk (MAX428/448)		Input Referenced $f = 10kHz$	-96			-96			-96			dB

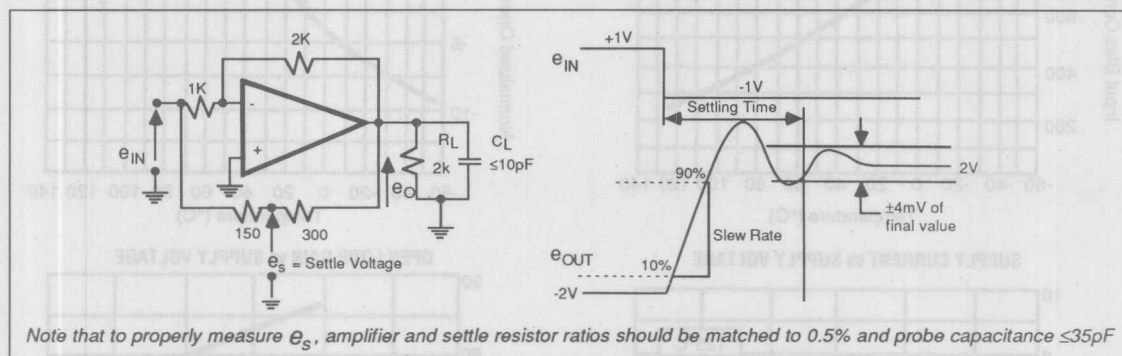


Figure 1A. Settling Time and Slew Rate Test Circuit

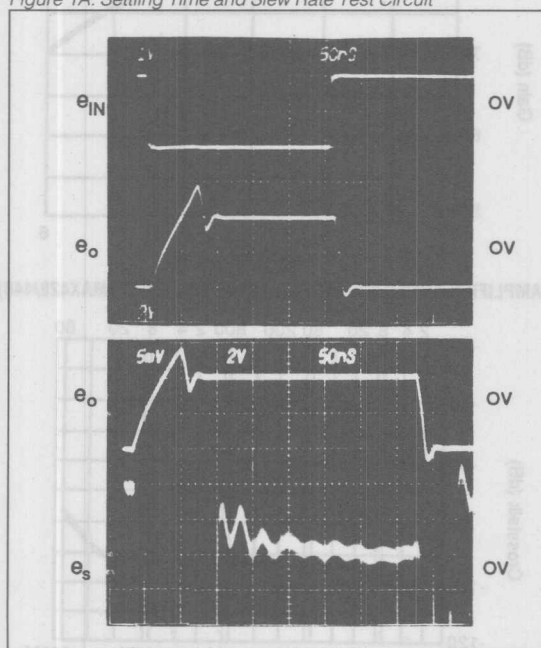


Figure 1B. Large Signal Response

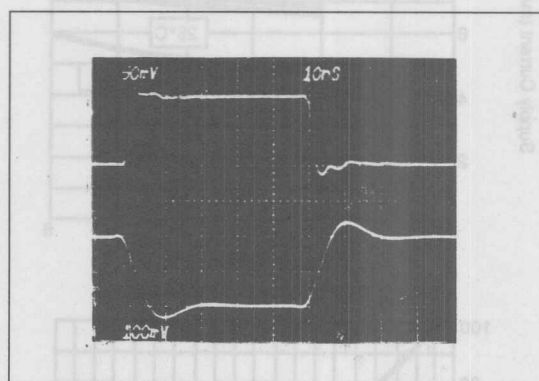


Figure 1C. Small Signal Response

MAX408/428/448

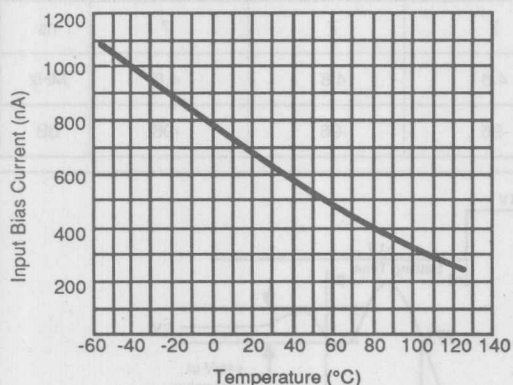
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Single/Dual/Quad High Speed, Fast Settling, High Output Current Operational Amplifier

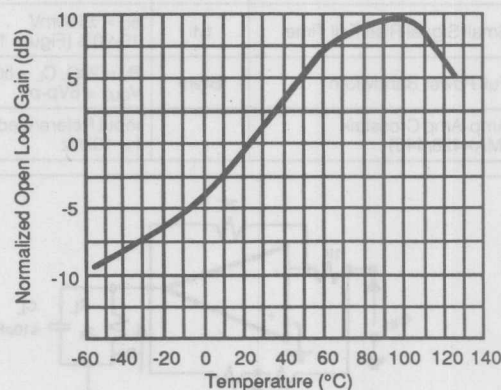
Typical Operating Characteristics

($V_S = \pm 5V$, $T_A = 25^\circ C$ unless otherwise stated and apply for each individual op amp where applicable)

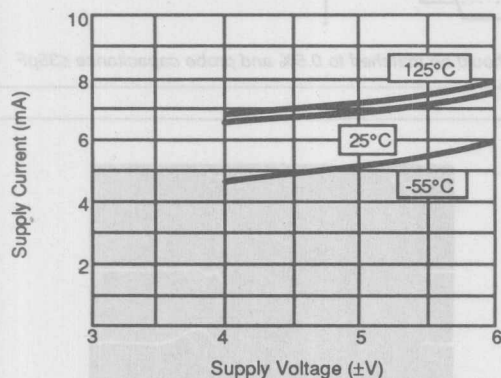
INPUT BIAS CURRENT vs TEMPERATURE



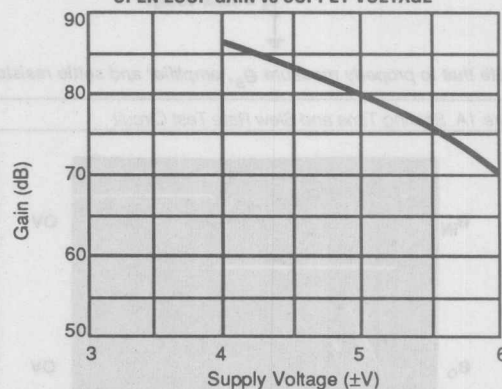
NORMALIZED OPEN LOOP GAIN vs TEMPERATURE



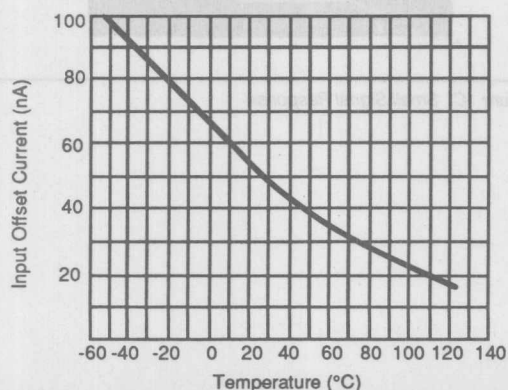
SUPPLY CURRENT vs SUPPLY VOLTAGE



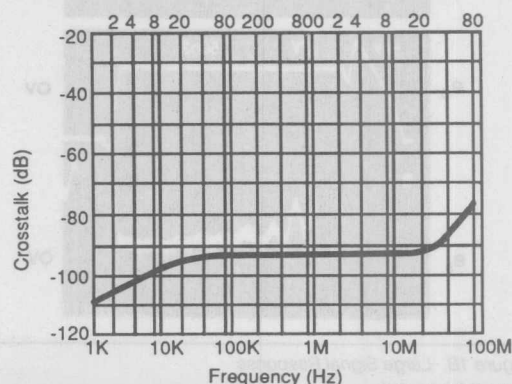
OPEN LOOP GAIN vs SUPPLY VOLTAGE



INPUT OFFSET CURRENT vs TEMPERATURE



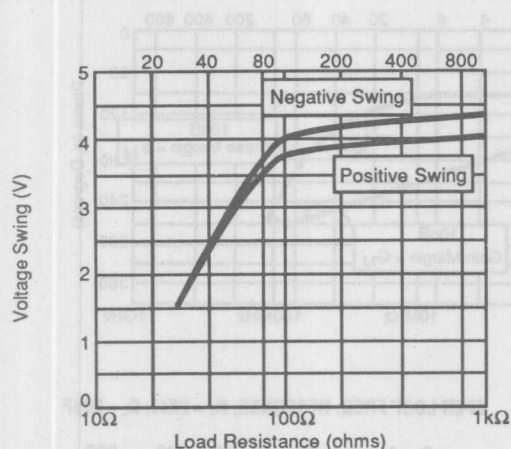
AMPLIFIER/AMPLIFIER CROSSTALK vs FREQUENCY (MAX428/448)



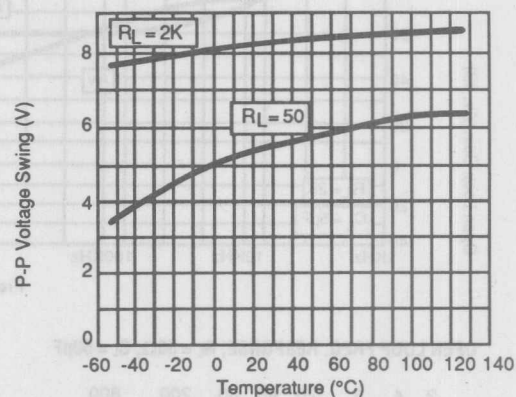
Single/Dual/Quad High Speed, Fast Settling, High Output Current Operational Amplifier

Typical Operating Characteristics (continued)

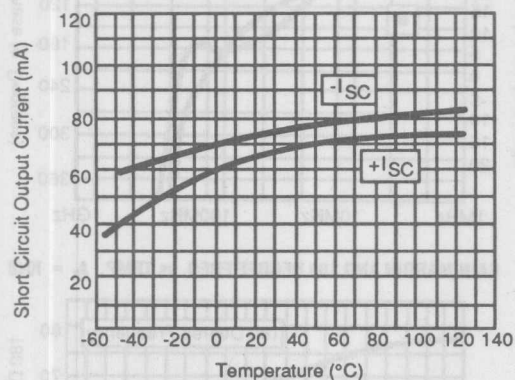
MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



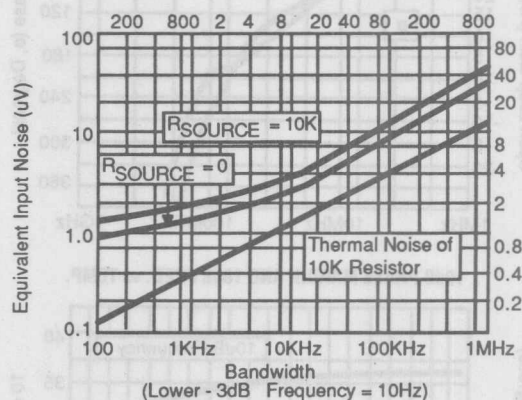
MAXIMUM OUTPUT VOLTAGE SWING vs TEMPERATURE



SHORT CIRCUIT OUTPUT CURRENT vs TEMPERATURE



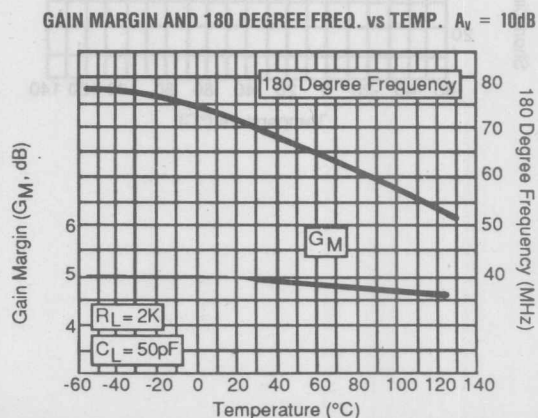
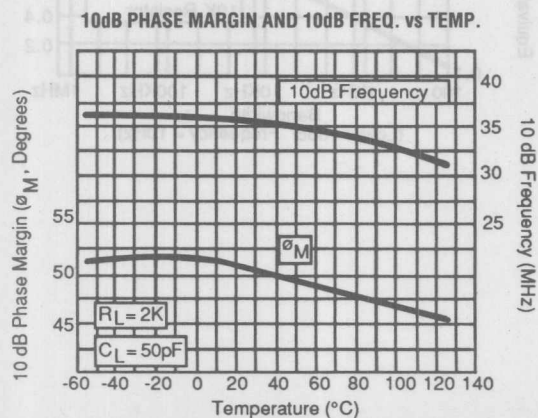
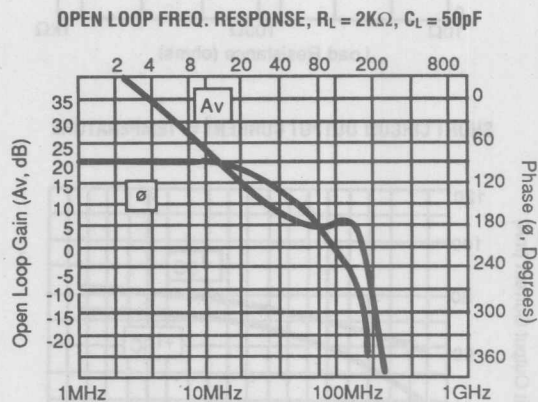
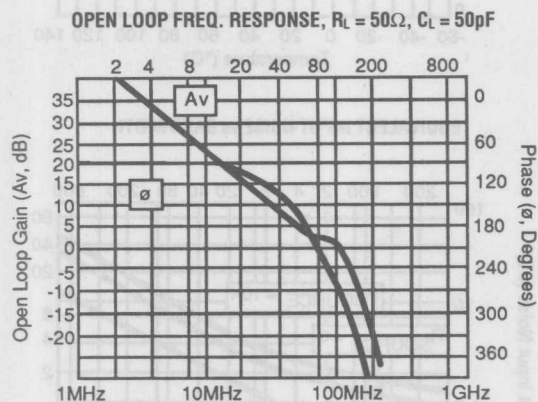
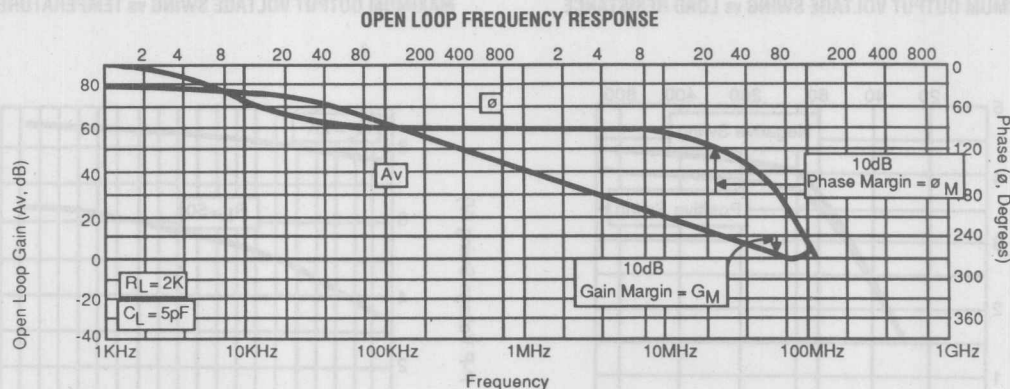
EQUIVALENT INPUT NOISE vs BANDWIDTH



MAX408/428/448

Single/Dual/Quad High-Speed, Fast-Settling, High Output Current Operational Amplifier

Typical Operating Characteristics (continued)



Single/Dual/Quad High-Speed, Fast-Settling, High Output Current Operational Amplifier

Application Information

AC Characteristics

The 35MHz 10dB crossover point of the MAX408/428/448 is achieved without feed forward compensation, a technique which can produce long tails in the recovery characteristic. The single pole rolloff follows the classic 20dB/decade slope to frequencies approaching 50MHz. The 10dB (3.2V/V) phase margin of 50°, even with a capacitive load of 50pF, gives stable and predictable performance down to non-inverting gain configurations of approximately 3V/V (inverting gains of -2V/V). At frequencies beyond 50MHz, the 20dB/decade slope is disturbed by an output stage zero, the damping factor of which is dependent upon the R_L , C_L load combination. This results in loss of gain margin (gain at loop phase = 360°) at frequencies of 70 to 100MHz which at a gain margin of 5dB ($R_L = 2K$, $C_L = 5pF$) results in a peak in the gain of 3 amplifier configurations as shown in Figures 3 and 4.

Figure 3 shows a blow up of the open loop characteristics in the 10MHz to 200MHz frequency range, as well as the corresponding closed loop characteristics for a gain of 3 non-inverting amplifier at similar load conditions. It should be noted that the open loop characteristic does not show the additional phase shift covered by the input capacitance pole. This is why the closed loop peaking at 30 to 40MHz is greater than what would be expected from the 50 to 60 degrees of phase margin indicated by the open loop characteristics. Corresponding small signal step response characteristics show well-behaved pulse waveforms with 16-33% overshoot.

The input capacitive pole can be neutralized by adding a feedback capacitor to R_2 . The value of capacitance is selected according to $R_1 C_{IN} = R_2 C_{FB}$, where C_{IN} is the

sum of the common mode and differential input capacitance $\approx 5pF$. For $R_2 = 2R_1$, $C_{FB} = C_{IN}/2 \approx 2.5pF$.

Figure 4 shows the results of this feedback capacitor addition. Neutralizing the input capacitance demonstrates the peaking that can result from the loss of gain margin at 70 to 100MHz. As the load time constant ($R_L C_L$) increases the peaking gets progressively worse $\approx 6dB$ at $R_L = 2K$, $C_L = 50pF$. The step response waveforms are as expected with a very strong 88MHz ring being exhibited at $R_L = 2K$, $C_L = 50pF$ and no overshoot at $R_L = 50\Omega$, $C_L = 5pF$.

Layout Considerations

As with any high-speed wideband amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should remain as short as possible, and the power supplies bypassed with 0.1 μF capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

MAX408 Offset Voltage Nulling

The configuration of Figure 2 will give a typical V_{OS} nulling range of $\pm 15mV$. If a smaller adjustment range is desired, resistor values R_1 and R_2 can be increased accordingly. For example, at $R_1 = 3.6k\Omega$, the adjustment range is $\pm 5mV$. Since pins 1 and 5 are not part of the signal path, AC characteristics are left undisturbed.

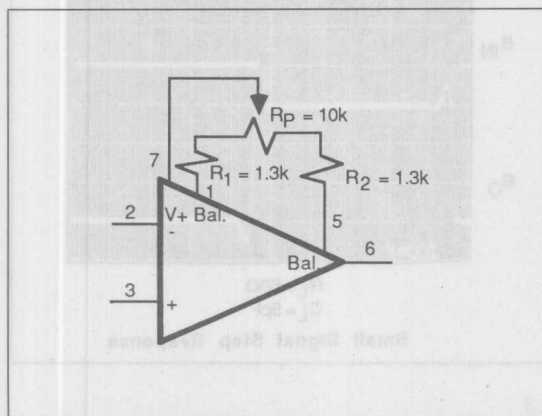
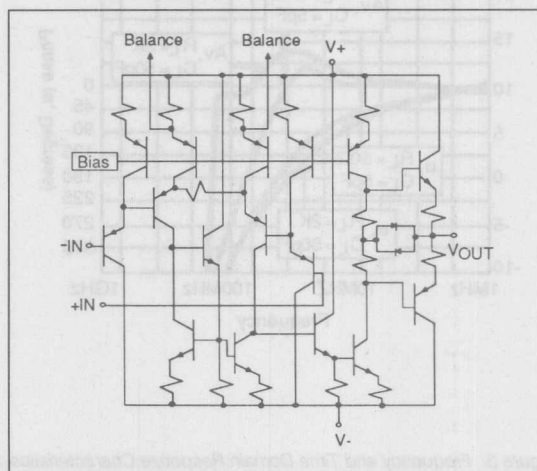


Figure 2. V_{OS} Nulling Method for MAX408



Simplified Schematic. For MAX428/448 omit balance pins.

MAX408/428/448

4

Single/Dual/Quad High-Speed, Fast-Settling, High Output Current Operational Amplifier

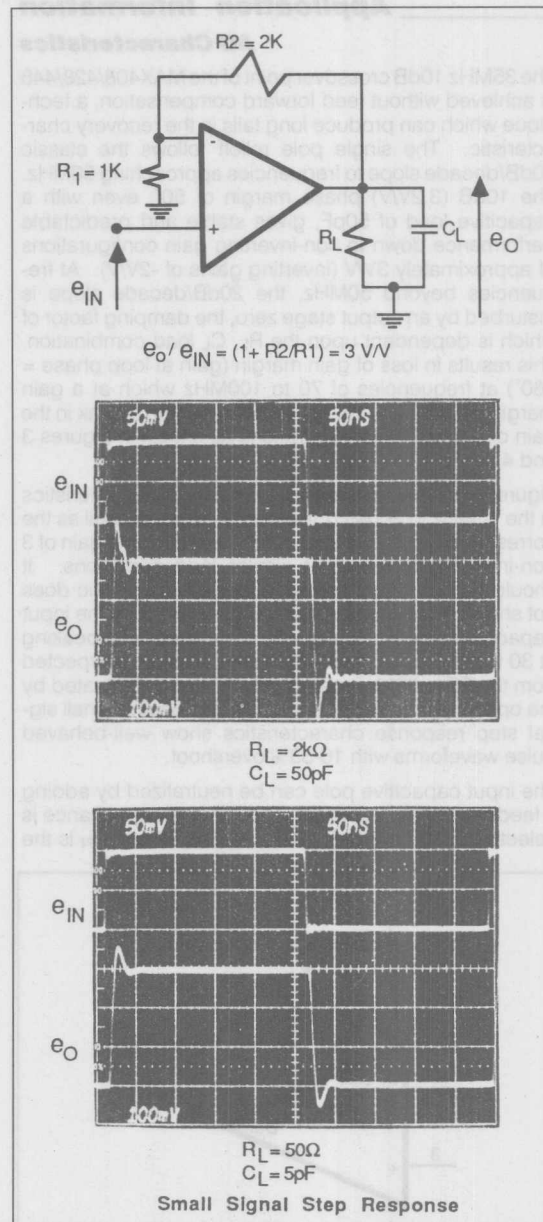
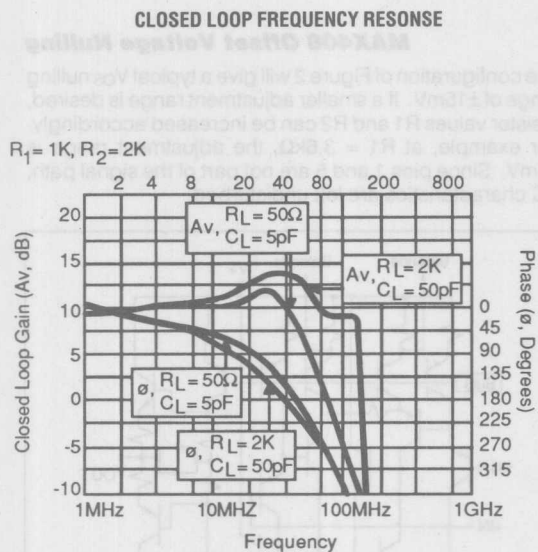
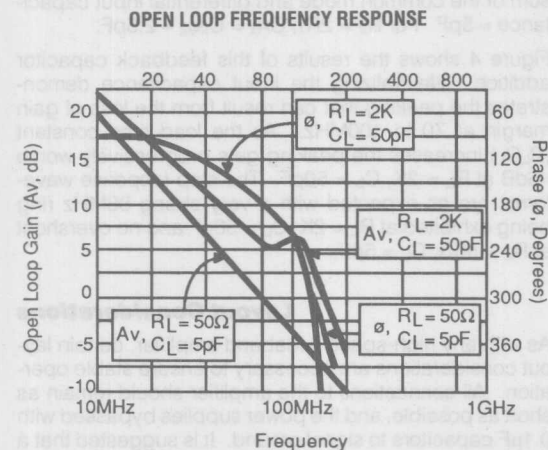


Figure 3. Frequency and Time Domain Response Characteristics, $A_v = 3$

Single/Dual/Quad High-Speed, Fast-Settling, High Output Current Operational Amplifier

MAX408/428/448

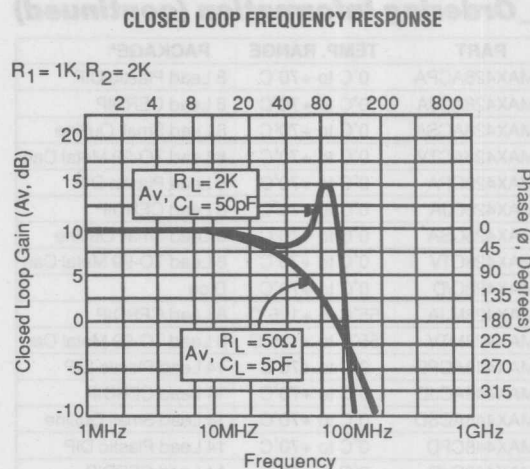
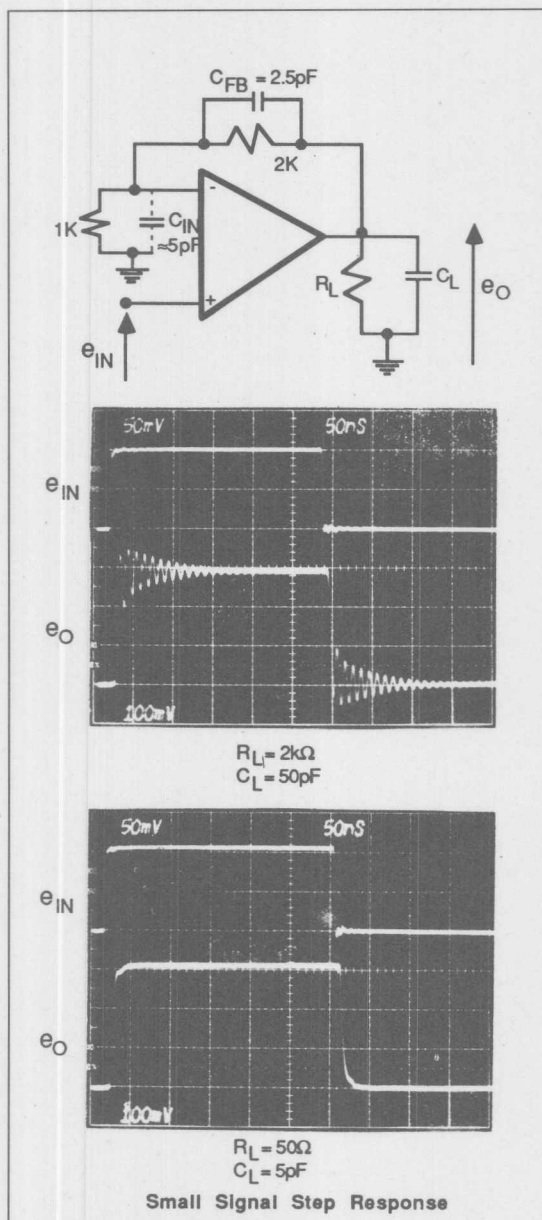


Figure 4. Response Characteristics with Input Pole Cancellation, $A_v = 3$

Single/Dual/Quad High-Speed, Fast-Settling, High Output Current Operational Amplifier

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*
MAX428ACPA	0°C to +70°C	8 Lead Plastic DIP
MAX428ACJA	0°C to +70°C	8 Lead CERDIP
MAX428ACSA	0°C to +70°C	8 Lead Small Outline
MAX428ACTV	0°C to +70°C	8 Lead TO-99 Metal Can
MAX428CPA	0°C to +70°C	8 Lead Plastic DIP
MAX428CJA	0°C to +70°C	8 Lead CERDIP
MAX428CSA	0°C to +70°C	8 Lead Small Outline
MAX428CTV	0°C to +70°C	8 Lead TO-99 Metal Can
MAX428C/D	0°C to +70°C	Dice
MAX428MJA	-55°C to +125°C	8 Lead CERDIP
MAX428MTV	-55°C to +125°C	8 Lead TO-99 Metal Can
MAX448ACPD	0°C to +70°C	14 Lead Plastic DIP
MAX448ACJD	0°C to +70°C	14 Lead CERDIP
MAX448ACSD	0°C to +70°C	14 Lead Small Outline
MAX448CPD	0°C to +70°C	14 Lead Plastic DIP
MAX448CJD	0°C to +70°C	14 Lead CERDIP
MAX448CSD	0°C to +70°C	14 Lead Small Outline
MAX448C/D	0°C to +70°C	Dice
MAX448MJD	-55°C to +125°C	14 Lead CERDIP

*Contact factory for availability of 20 Lead LCC

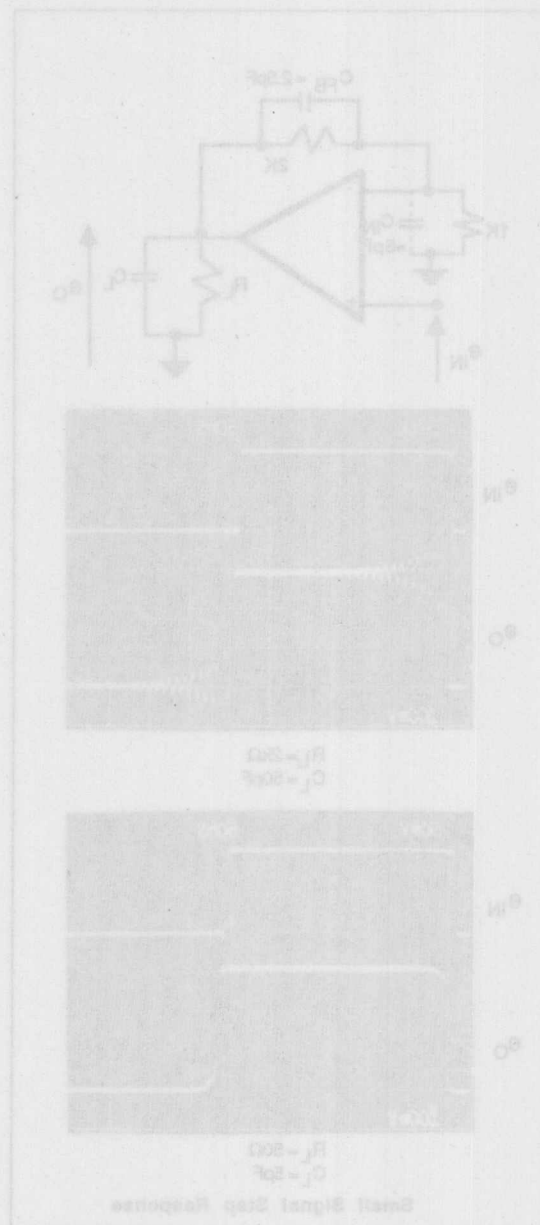


Figure 4: Typical Output Characteristics with Load Regulation

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MAXIM

Ultra High-Precision CMOS Op Amps

MAX425/MAX426

General Description

The MAX425/MAX426 precision CMOS amplifiers provide input offset and noise specifications superior to chopper stabilized amplifiers while using no external capacitors. Two independent error correction schemes operate on-chip: A unique input switching design reduces input offset voltage (V_{OS}) to $1\mu V$, while offsets inside the amplifier are removed with digital correction to reduce common-mode errors and minimize clock ripple. The MAX425 is unity gain stable and has a 350kHz gain-bandwidth product. The MAX426 is uncompensated with a gain-bandwidth product of 12MHz.

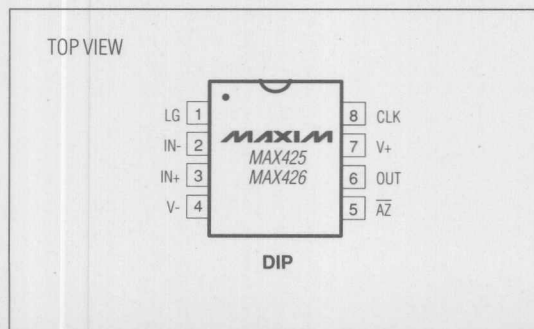
The error correction design of the MAX425/MAX426 is completely different from chopper stabilized amplifiers. Superior V_{OS} is achieved with negligible clock noise, fast overload recovery, improved high-frequency performance, and reduced $1/f$ noise. 1Hz bandwidth noise is typically $1/5$ that of monolithic chopper op amps. The amplifiers are ideal for precision measurement applications where large, accurate gains and low noise are required. Additionally, the MAX426 is optimal where wide bandwidth is required.

Signal input and power-supply connections conform to the standard op amp pin configuration. Auto-zero and clock pins are limited to LG, AZ, and CLK. pins. Both devices operate from $\pm 2.5V$ to $\pm 7.5V$ or from single supplies ranging from $+5V$ to $+15V$. They are supplied in 8-pin plastic DIP and CERDIP and 16-pin Wide SO packages.

Applications

Low-Noise DC Amplifiers
Weigh Scales
Thermocouple Amplifiers
Strain Gauge Vibration Analysis

Pin Configuration



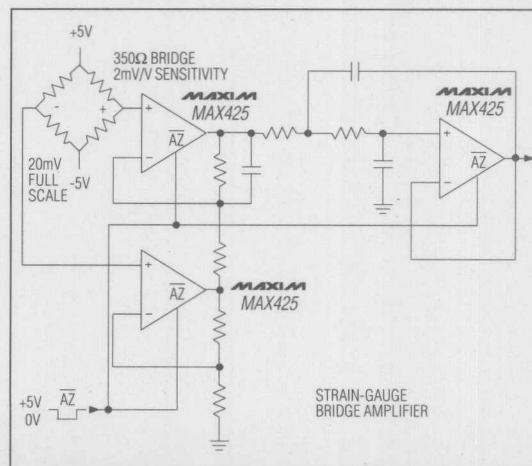
Features

- ◆ $1\mu V$ Maximum V_{OS}
- ◆ $300nV_{p-p}$ Noise (0.1Hz to 10Hz BW)
- ◆ $0.01\mu V/^{\circ}C$ Max Offset Drift
- ◆ No External Components
- ◆ Controllable Auto-Zero
- ◆ 180dB Open Loop Gain
- ◆ 12MHz Gain-Bandwidth (MAX426)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX425CPA	$0^{\circ}C$ to $+70^{\circ}C$	8 Plastic DIP
MAX425CWE	$0^{\circ}C$ to $+70^{\circ}C$	16 Wide SO
MAX425C/D	$0^{\circ}C$ to $+70^{\circ}C$	Dice
MAX425EPA	$-40^{\circ}C$ to $+85^{\circ}C$	8 Plastic DIP
MAX425EWE	$-40^{\circ}C$ to $+85^{\circ}C$	16 Wide SO
MAX425EJA	$-40^{\circ}C$ to $+85^{\circ}C$	8 CERDIP
MAX425MJA	$-55^{\circ}C$ to $+125^{\circ}C$	8 CERDIP
MAX426CPA	$0^{\circ}C$ to $+70^{\circ}C$	8 Plastic DIP
MAX426CWE	$0^{\circ}C$ to $+70^{\circ}C$	16 Wide SO
MAX426C/D	$0^{\circ}C$ to $+70^{\circ}C$	Dice
MAX426EPA	$-40^{\circ}C$ to $+85^{\circ}C$	8 Plastic DIP
MAX426EWE	$-40^{\circ}C$ to $+85^{\circ}C$	16 Wide SO
MAX426EJA	$-40^{\circ}C$ to $+85^{\circ}C$	8 CERDIP
MAX426MJA	$-55^{\circ}C$ to $+125^{\circ}C$	8 CERDIP

Typical Operating Circuit



MAXIM

Maxim Integrated Products 4-31

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MAXIM

± 15 Volt Chopper Stabilized Operational Amplifier

MAX430/432

General Description

The MAX430 and MAX432 are CMOS ± 15 V chopper-stabilized amplifiers designed for high accuracy signal conditioning, amplification, and instrumentation applications. They offer input offset and drift specifications superior to previous "precision" bipolar op-amps and monolithic chopper amplifiers. External capacitors, required with previous CMOS chopper amplifiers, are NOT needed with the MAX430/432. Both amplifiers are packaged in 8 pin plastic DIPs.

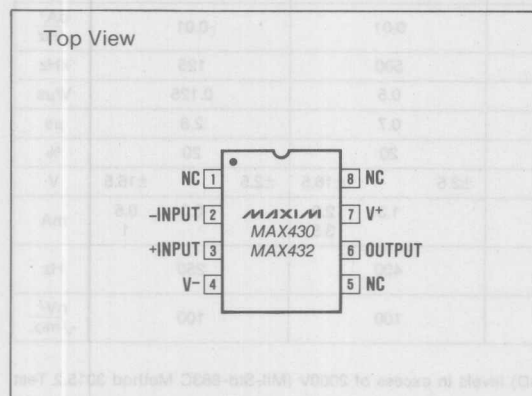
The combination of ± 15 V operation, low power, and standard op-amp pin configuration allows these devices to plug directly into almost any OP07/OP77/LM108/ μ A741 socket regardless of what offset balancing or frequency compensation circuitry might be present. A wide input voltage range that includes the negative supply allows applications not possible with most conventional operational amplifiers.

The MAX430 has a maximum supply current of 2mA and a unity gain frequency of 500kHz; the MAX432 has a maximum supply current of 0.5mA and a unity gain frequency of 125kHz.

Applications

- Precision Amplifiers
- Signal Conditioning for:
 - Thermocouples
 - Strain Gauges, Load Cells
 - Resistance Temperature Devices (RTDs)
- High Accuracy Data Acquisition
- D.C. Stabilization of Amplifiers and Systems
- 4-20mA process control transmitters

Pin Configuration



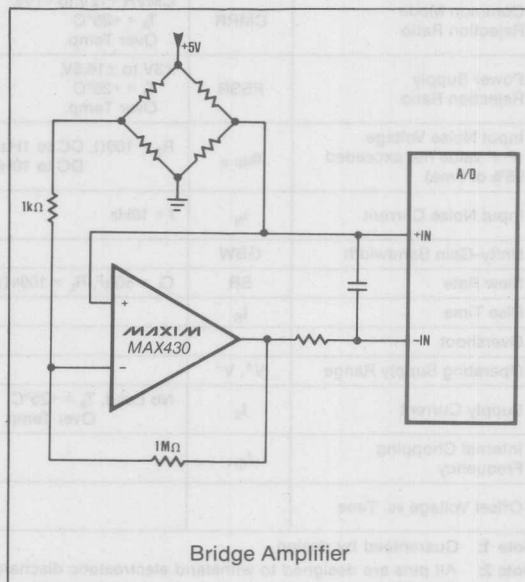
Features

- No External Capacitors Required
- 5 μ V Max Offset Voltage
- 30pA Input Bias Current
- Low Input Voltage Noise 0.3 μ Vp-p (DC-1Hz)
- Low Input Current Noise 0.01pA/ $\sqrt{\text{Hz}}$ at 10Hz
- ± 15 V Supply Operation
- Input Voltage Range Includes V⁻
- Low Power CMOS Design

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX430CPA	0°C to +70°C	8 Lead Plastic DIP
MAX430EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX432CPA	0°C to +70°C	8 Lead Plastic DIP
MAX432EPA	-40°C to +85°C	8 Lead Plastic DIP

Typical Operating Circuit



MAXIM

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Maxim Integrated Products 4-33

±15 Volt Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	+36V
Input Voltage	($V^+ + 0.3V$) to ($V^- - 0.3V$)
Storage Temperature Range	-65°C to +160°C
Operating Temperature Range	
MAX430C, MAX432C	0°C to +70°C
MAX430E, MAX432E	-40°C to +85°C

Lead Temperature (Soldering 10 sec)	+300°C
Duration of Output Short Circuit	Indefinite
Current into Any Pin	10mA
Continuous Total Power Dissipation	375mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V^- = -15V$, $T_A = +25^\circ C$, Test circuit unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MAX430			MAX432			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$+V_{OS}$	$T_A = +25^\circ C$		1 2	5 10		1 2	5 10	μV
Average Temperature Coefficient of Input Offset Voltage		Over Temperature Range (Note 1)		0.02	0.05		0.02	0.05	$\mu V/^\circ C$
Input Bias Current (Doubles every 10°C above about 60°C)	I_B	$T_A = +25^\circ C$ Over Temp.		10 35	100		10 35	100	pA
Input Offset Current (Doubles every 10°C above about 60°C)	I_B	$T_A = +25^\circ C$ Over Temp.		15 50	200		15 50	200	pA
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	$R_L = 10k\Omega$, $V_{OUT} = \pm 10V$	120	150		120	150		dB
Output Voltage Swing	V_{OUT}	$R_L = 10k\Omega$ $R_L = 100k\Omega$	± 12	± 14.5 ± 14.95		± 14	± 14.6		V
Common Mode Voltage Range	CMVR	Positive Negative	+12 -15	+12.5 -15.1		+12 -15	+12.5 -15.1		V
Common Mode Rejection Ratio	CMRR	CMVR +12V to -15V, $T_A = +25^\circ C$ Over Temp.	120 110	140 140		120 110	140 140		dB
Power Supply Rejection Ratio	PSSR	$\pm 3V$ to $\pm 16.5V$, $T_A = +25^\circ C$ Over Temp.	120 110	140 140		120 110	140 140		dB
Input Noise Voltage (P-P value not exceeded 95% of time)	e_{NP-p}	$R_S = 100\Omega$, DC to 1Hz DC to 10Hz		0.3 1.1			0.4 1.2		μV_{p-p}
Input Noise Current	i_N	$f = 10Hz$		0.01			0.01		pA/\sqrt{Hz}
Unity-Gain Bandwidth	GBW			500			125		kHz
Slew Rate	SR	$C_L = 50pF$, $R_L = 100k\Omega$		0.5			0.125		V/ μs
Rise Time	t_R			0.7			2.8		μs
Overshoot				20			20		%
Operating Supply Range	V^+ , V^-		± 2.5		± 16.5	± 2.5		± 16.5	V
Supply Current	I_S	No Load, $T_A = +25^\circ C$ Over Temp.		1.3 2.0 3.5			0.3 0.5 1		mA
Internal Chopping Frequency	f_{CH}			400			250		Hz
Offset Voltage vs. Time				100			100		$nV/\sqrt{mo.}$

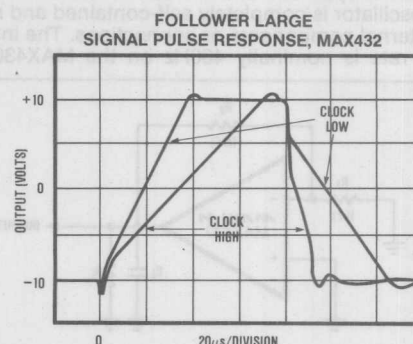
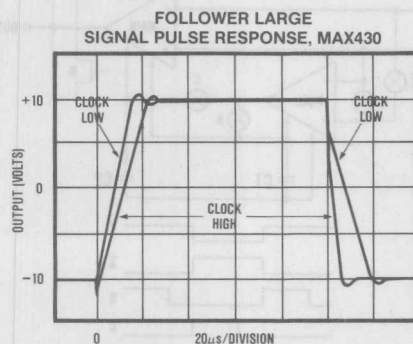
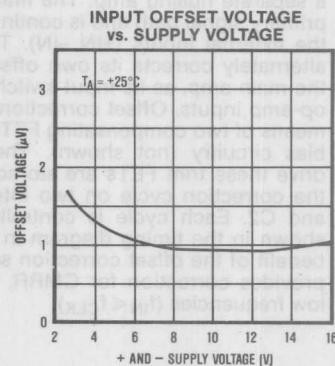
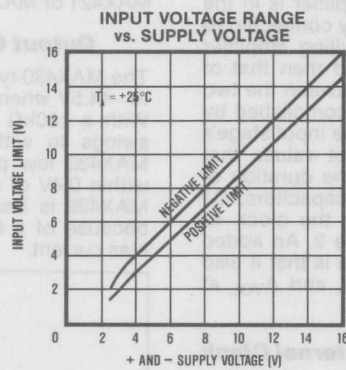
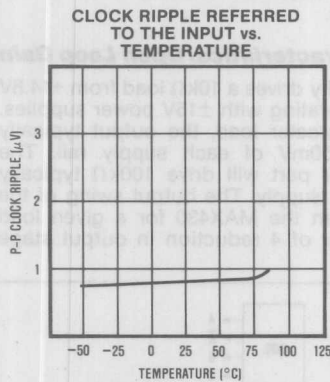
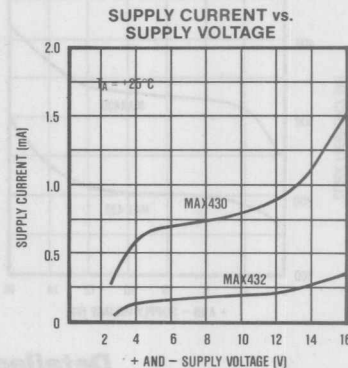
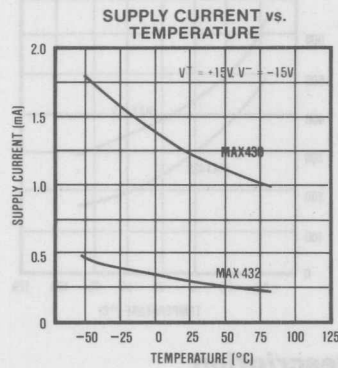
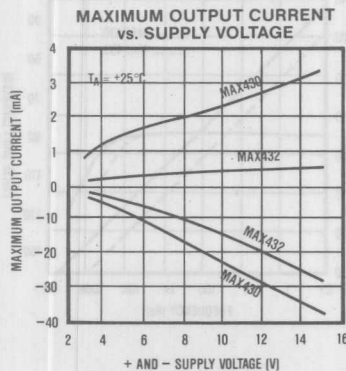
Note 1: Guaranteed by design.

Note 2: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil-Std-883C Method 3015.2 Test Circuit)

± 15 Volt Chopper Stabilized Operational Amplifier

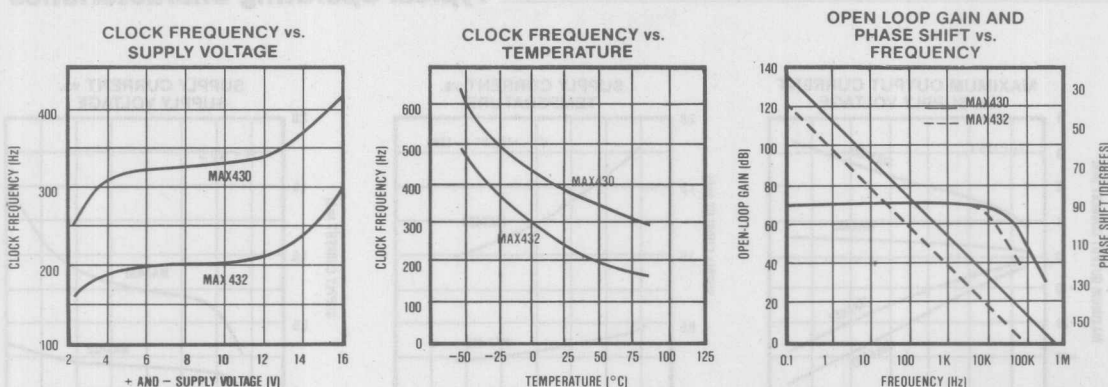
Typical Operating Characteristics

MAX430/432



±15 Volt Chopper Stabilized Operational Amplifier

Typical Operating Characteristics



Detailed Description

Amplifier Operation

A block diagram of a MAX430/432 is shown in Figure 2. Internally there is a main signal path amplifier and a separate nulling amp. The main amplifier is in the primary signal path and is continuously connected to the external inputs (+IN, -IN). The nulling amplifier alternately corrects its own offset, and then that of the main amp, as its input switches between the two op-amp inputs. Offset correction is accomplished by means of two compensating FETs in the input stage's bias circuitry (not shown). The offset values that drive these trim FETs are stored for the duration of the correction cycle on two internal capacitors, C1 and C2. Each cycle is controlled by the clock as shown in the timing diagram in Figure 2. An added benefit of the offset correction scheme is that it also provides correction for CMRR, PSRR, and A_{VOL} at low frequencies ($f_{IN} \ll f_{CLK}$).

Internal Clock

An on-chip clock is included on the MAX430/432 to control the operation of the offset correction circuitry. This oscillator is completely self-contained and needs no external components or connections. The internal clock rate is nominally 400Hz on the MAX430 and

250Hz on the MAX432 and cannot be adjusted. If other clock frequencies are desired, refer to the MAX421 or MAX423.

Output Characteristics/Open Loop Gain

The MAX430 typically drives a 10k Ω load from +14.8V to -14.5V when operating with $\pm 15V$ power supplies. With a 100k Ω or greater load, the output typically swings to within 50mV of each supply rail. The MAX432 low power part will drive 100k Ω typically within 0.4V of each supply. The output swing of the MAX432 is less than the MAX430 for a given load because of a factor of 4 reduction in output stage bias current.

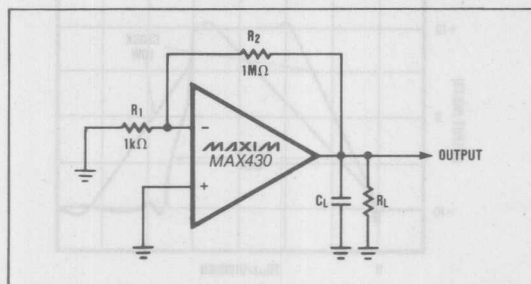


Figure 1. Test Circuit.

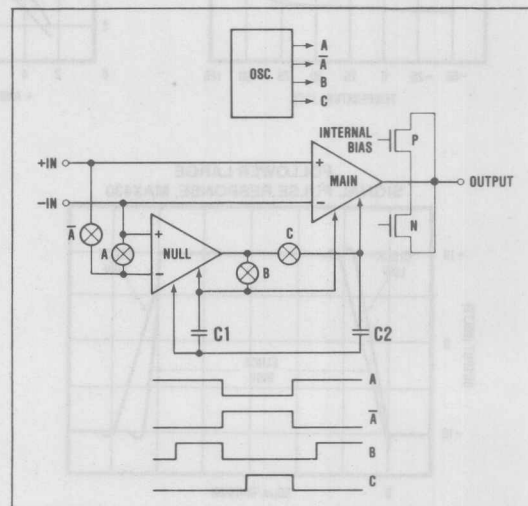


Figure 2. Maxim MAX430 Series Amplifier Block Diagram.

±15 Volt Chopper Stabilized Operational Amplifier

MAX430/432

The open loop gain of a MAX430 is load dependent for resistances which are less than 10k Ω . The effect is largely due to the impedance of the amplifier's output stage. The gain is about 17dB lower with a 1k Ω load than it is with 10k Ω (MAX430). Even with 1k Ω the gain is typically 120dB, the reduction is insignificant for low frequency applications. In wide-band circuits, however, the best results are achieved with loads of 10k Ω or more where the amplifier's open loop response is a smooth 6dB/octave slope from 0.1Hz to 0.5MHz. Additionally, there is negligible phase shift at the frequency where the null amp is rolled off.

Clock Ripple and Noise

There are two components to MAX430/432 amplifier noise: wide-band noise and clock-related ripple. With conventional op-amps, 1/f noise is often a problem in low level applications. This is the case, even with filtering in low frequency applications, because 1/f noise is difficult to remove. Chopper stabilization techniques eliminate 1/f noise in the MAX430/432 to provide superior low frequency performance.

The chopper generates a small amount of ripple at the internal clock frequency. Typically its peak-to-peak input referred amplitude is 15 μ V. This signal is easily reduced by band limiting the amplifier's response to below the internal oscillator frequency. In wide band limiting the amplifier's response to below the internal oscillatory frequency. In wide band applications, positive and negative going 5 μ s pulses, with a typical output amplitude of 15mV, also appear. In circuits which are band limited to 5kHz or less, this noise will not be seen and averages to zero. However,

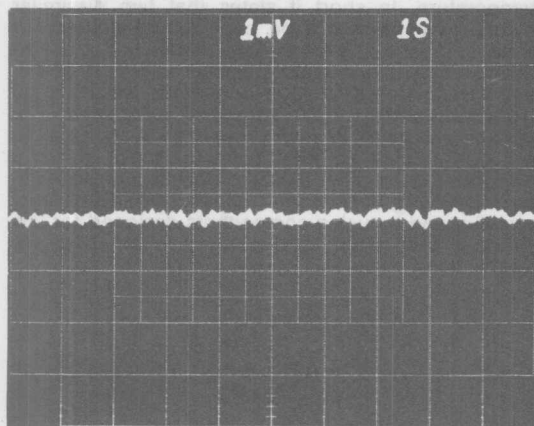


Figure 3. D.C. to 1Hz Noise, 1 μ V/vert. div. referred to input, 1 second/horiz. div.

since the pulses are output related, they have little dependence on closed loop gain and are only partially filtered with feedback capacitance around the amplifier. Filtering or band limiting in the circuitry following the amplifier removes this noise.

Intermodulation

In some chopper-stabilization amplifier designs, interaction between the input signal and the chopper frequency sometimes produces intermodulation products in the form of sum and difference signals. If the input frequency and the chop rate are close enough to each other, a difference signal may appear as a DC error at the output. The MAX430 series minimizes these problems with active compensation circuitry that virtually eliminates intermodulation effects and controls the amplifier's open loop gain-phase characteristics as well. With well-behaved open loop parameters, the chopper's circuitry impact on the amplifier's dynamic performance can be ignored in most applications. If chopper oscillator interaction is a problem, then the MAX421/423, which has an externally controllable oscillator, should be used.

Overload Recovery

The MAX430/432 like most chopper-stabilized amplifiers takes more time to recover from input overloads than a conventional op-amp. The reason for this is that the internal offset nulling capacitors are overcharged during input overloads as the amplifier attempts to "correct" the overload condition via the nulling circuitry. Once these capacitors are overcharged, some time is needed for them to return to the proper level. The length of this delay depends on the duration and amplitude of the overload. The worst case time is about 4 seconds for a severely over-driven MAX430. If the recovery takes too long then a MAX421/423 which provides a "Clamp" input to speed overload recovery, should be used.

Application Hints

Plugging Into A Conventional Op-Amp Socket

The MAX430/432 can be powered from supplies ranging from +5V to \pm 15V. It can therefore plug into most conventional "741 pinout" op-amp applications. On other op-amps, pins 1, 5, and 8 are used for a variety of functions specific to the amplifier: typically frequency compensation, setting bias, or offset correction. Since the MAX430/432 is internally compensated and its internal chopper removes substantially all of the offset voltage and drift, no connections are required to pins 1, 5 and 8. These pins are not internally connected on the MAX430/432 so that external connections from existing designs will not affect the op-amp's operation.

±15 Volt Chopper Stabilized Operational Amplifier

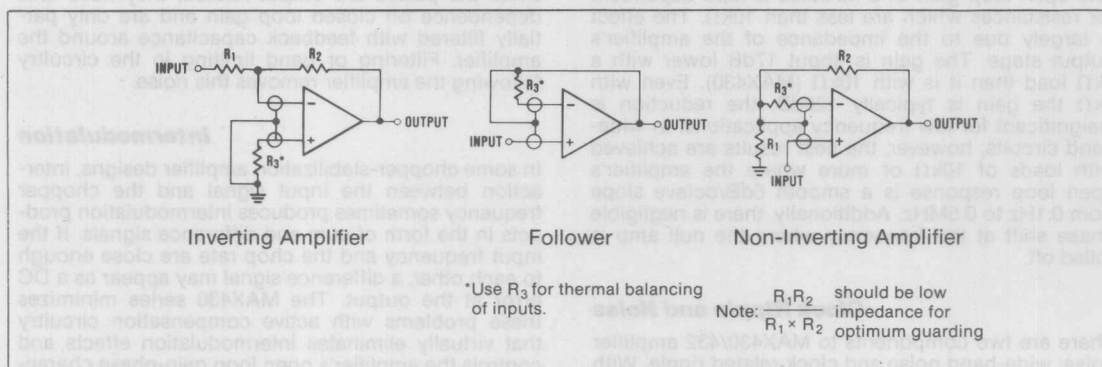


Figure 4. Input Guard Connections.

The MAX432 has the same offset and drift specifications as the MAX430 but is designed for low power operation. As a low power op-amp it has been optimized for driving relatively light loads. With output currents above several hundred microamps, there will be some reduction in open loop gain and output swing. The MAX430, however, is guaranteed to swing $\pm 12V$ into a $10k\Omega$ load. The MAX432's load driving limitations should, in general, not be a problem in replacement applications because conventional precision amplifiers are not normally used where they must drive heavy loads. This is because the resulting output stage power dissipation often generates thermally induced error voltages elsewhere in the amplifier.

Single Supply Operation

The MAX430/432 is well suited for operation in single power supply applications, i.e. circuits that have system ground connected to V^- . With supply voltages of 10 volts or above, the input range is typically from Ground to $V^+ - 1.5V$. At lower supply voltages the lower input range limit is higher (approx. $GND + 0.5V$ at 5V supply). With a single power supply, the amplifier's output will swing to within approximately 50mV of ground and V^+ when driving a $100k\Omega$ load.

Low Voltage Signals

Realizing microvolt offset and nanovolt drift performance goes beyond the selection of a precision amplifier (though it's not a bad start). When trying to amplify very low level signals any number of outside error sources can confuse the measurement. These errors are often indistinguishable from real signal or amplifier error, which of course is why they are a problem.

Thermo-Electric Effect

This property describes how thermocouples measure temperature. In short it states that two dissimilar metals in contact can be expected to generate a voltage. This is fine for thermocouples but is not so useful when pin-to-socket, socket-to-circuit board, and circuit board-to-edge connector junctions all generate signals which can add to input error. The voltage generated in such situations can range from 0.1 to 10's of $\mu V/^\circ C$, many times the offset drift of a MAX430/432. In general such problems are dealt with by minimizing sockets and connectors in low level circuitry and by using components designed for low thermal EMF when connectors, relays, etc. are unavoidable.

±15 Volt Chopper Stabilized Operational Amplifier

MAX430/432

Gradients

The presence of heat in low level circuitry is often not so much a problem as are thermal gradients. Gradients can, for example, cause normally balanced amplifier input connections to be at different temperatures. These connections then generate different thermoelectric voltages that can no longer be completely cancelled by the balanced inputs. The moral then is to minimize thermal gradients by keeping power dissipation and air currents in and around low level circuitry and connections at a minimum.

Thermal Symmetry

Another useful low level technique is to design thermal "symmetry" into the layout. This may mean adding dummy resistors and connections so that the thermal mass, as well as the number of thermoelectric error sources, in an input pair will cancel. It may also involve running input traces near each other and keeping their size the same as well. Thermal "filtering" with small enclosures or even insulation for sensitive areas can also be helpful.

Low Current Signals, Input Guards

Low leakage, high impedance CMOS inputs allow the MAX430 amplifier family to amplify the signals of very high impedance sources. Though the amplifier's input bias current is measured in picoamps, getting the surrounding connections to live up to that specification requires some attention. In applications where picoamp or nanoamp errors can be significant, board leakage either from surface contamination or through the board material itself may be a problem.

Controlling Leakage

Using low leakage board materials and proper cleaning methods after assembly can provide marked reductions in leakage induced errors. Beyond this, conformal coatings can be used to control later surface contamination. In some cases, Teflon insulators and/or circuit board guard rings may be necessary to protect very high impedance nodes. Guard connections for various amplifier configurations are shown in Figure 4. In each case the guard is connected to a low impedance point that is approximately at the same potential as the inputs. Leakage currents from other points on the board are then absorbed by the guard. For best results, guard rings should be used on both sides of the circuit board.

Typical Applications

4

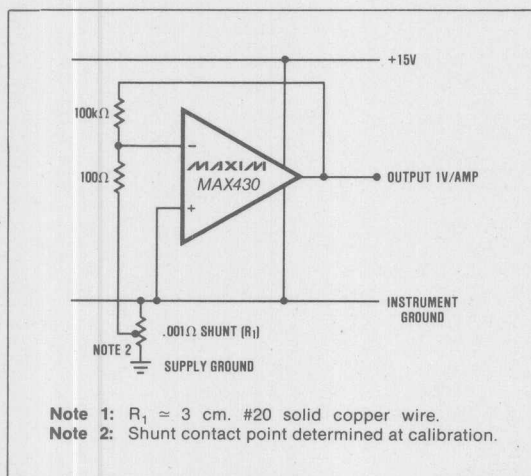
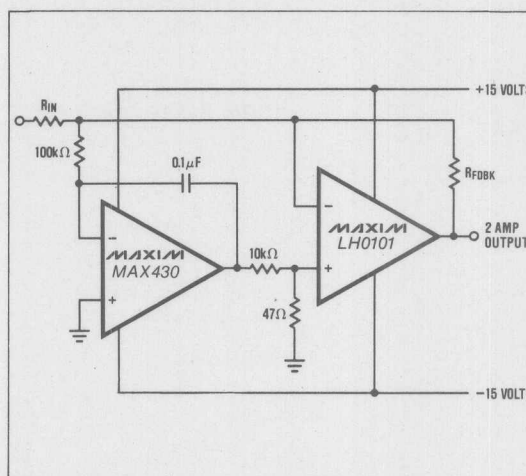


Figure 5. Ultra-low Current Shunt Amp.



D.C. Stabilized Power Op-Amp. Main amp has 5MHz unity-gain point.

±15 Volt Chopper Stabilized Operational Amplifier

Typical Applications

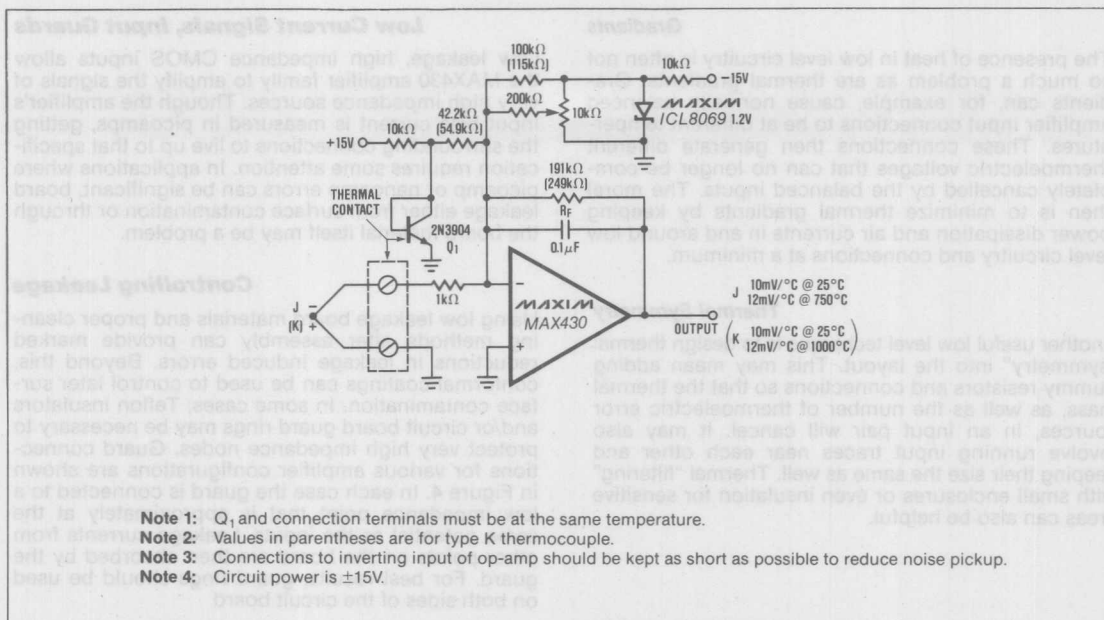
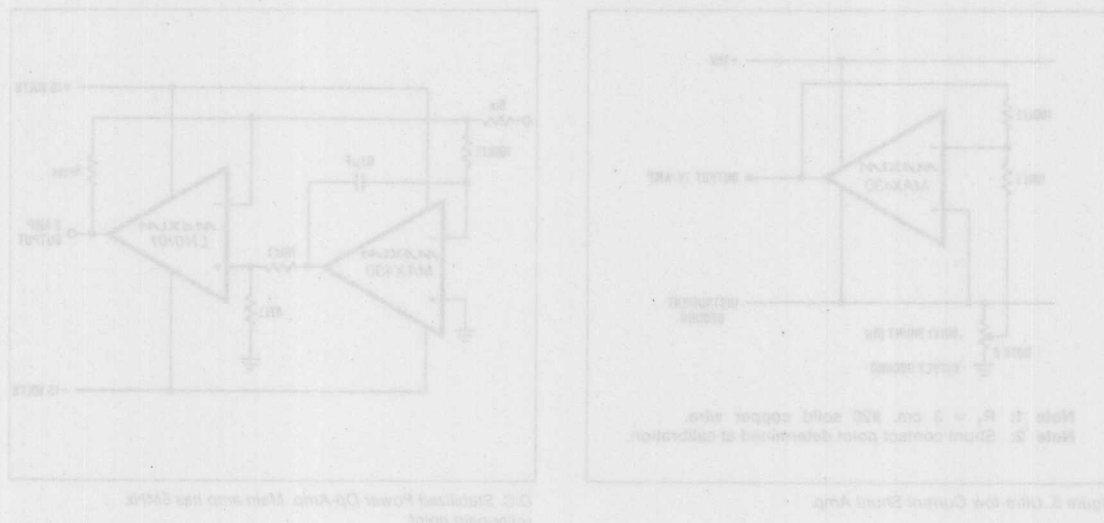


Figure 7. Amplifier with Cold-Junction Compensation for Grounded Thermocouples.



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MAXIM

CMOS Video Multiplexer/Amplifier

MAX452/3/4/5

General Description

The MAX452 is a unity-gain stable, 50MHz video amplifier capable of driving a 75 ohm load directly. The MAX453, MAX454, and MAX455 combine the 50MHz video amplifier, of the MAX452, with an on-board multiplexer offering 2, 4, or 8 channels respectively. All of the MAX452 family devices operate from $\pm 5V$ supplies and typically consume only 250mW.

Optimized for video applications, these amplifiers will directly drive a 150 ohm load to $\pm 2V$, and will swing $\pm 1V$ into a 75 ohm load. All amplifiers are unity-gain stable and do not require external frequency compensation components. The MAX453/454/455 operate as positive-gain amplifiers, gain being set by two external resistors. Since they are connected as non-inverting amplifiers, their minimum closed-loop gain is 0dB. In most applications the amplifier's closed-loop gain will be set at 0dB or +6dB (1 V/V or 2 V/V), which guarantees a minimum bandwidth of 25MHz.

Applications

Video signal multiplexing
75 ohm cable drivers
Driving flash converters
Video Crosspoint Switches

Features

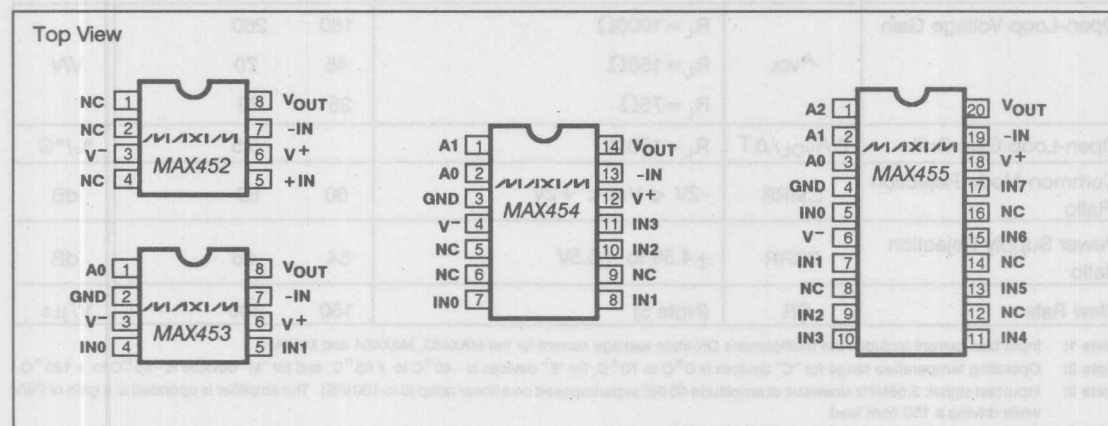
- ◆ Unity-gain bandwidth of 50MHz typ.
- ◆ Low input capacitance: 7pF typ.
- ◆ No frequency-compensation required
- ◆ Low power operation: 250mW typ.
- ◆ Low bias current: 10pA typ.
- ◆ Directly drives 75 ohm cable
- ◆ 70 dB typical OFF isolation at 4 MHz

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX452CPA	0°C to +70°C	8 lead plastic DIP
MAX452CSA	0°C to +70°C	8 lead small-outline
MAX452C/D	0°C to +70°C	Dice
MAX452EPA	-40°C to +85°C	8 lead plastic DIP
MAX452EJA	-40°C to +85°C	8 lead CERDIP
MAX452MJA	-55°C to +125°C	8 lead CERDIP
MAX453CPA	0°C to +70°C	8 lead plastic DIP
MAX453CSA	0°C to +70°C	8 lead small-outline
MAX453EPA	-40°C to +85°C	8 lead plastic DIP
MAX453EJA	-40°C to +85°C	8 lead CERDIP
MAX453MJA	-55°C to +125°C	8 lead CERDIP
MAX454CPD	0°C to +70°C	14 lead plastic DIP
MAX454CSD	0°C to +70°C	14 lead small-outline
MAX454EPD	-40°C to +85°C	14 lead plastic DIP
MAX454EJD	-40°C to +85°C	14 lead CERDIP

(Ordering Information Continued on Last Page.)

Pin Configurations



MAXIM

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Maxim Integrated Products 4-41

CMOS Video Multiplexer/Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	12 V
Positive Supply Voltage, V^+ (rel. GND)	+12V
Negative Supply Voltage, V^- (rel. GND)	-12V
Analog Input Voltage	(V^+) +0.3 V to (V^-) -0.3 V
Digital Input Voltage	-0.3 V to (V^+) +0.3 V
Storage Temperature Range	-65°C to +160°C
Operating Temperature Range	
MAX452C, MAX453C,	
MAX454C, MAX455C	0°C to +70°C
MAX452E, MAX453E,	
MAX454E, MAX455E	-40°C to +85°C
MAX452M, MAX453M,	
MAX454M, MAX455M	-55°C to +125°C

Lead temperature (Soldering, 10 sec)	300°C
Duration of Output Short-Circuit to ground	Indefinite
Input Current, power on or off	
Digital Inputs	+20 mA
All other pins	±50 mA
Continuous Total Power Dissipation ($T_A = +70^\circ\text{C}$)	
8 Pin CERDIP (derate 8.0mW/°C above 70°C)	640mW
14 Pin CERDIP (derate 9.5mW/°C above 70°C)	760mW
20 Pin CERDIP (derate 11.1mW/°C above 70°C)	890mW
8 Pin Plastic DIP (derate 8.3mW/°C above 70°C)	660mW
14 Pin Plastic DIP (derate 10.0mW/°C above 70°C)	800mW
20 Pin Plastic DIP (derate 11.1mW/°C above 70°C)	890mW
8 Pin Small-Outline (derate 5.9mW/°C above 70°C)	320mW
14 Pin Small-Outline (derate 8.7mW/°C above 70°C)	480mW
20 Pin Small-Outline (derate 10.0mW/°C above 70°C)	550mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS MAX452/3/4/5

($V^+ = +5\text{V}$, $V^- = -5\text{V}$, $-2\text{V} \leq V_{\text{IN}} \leq +2\text{V}$, Output Load Resistor = 150Ω , $T_A = +25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VIDEO AMPLIFIER (MAX452/3/4/5)						
Input Voltage Range	V_{IN}	Over Temperature Range (Note 2)	-2		2	V
Input Offset Voltage	V_{OS}			2	5	mV
Offset Voltage Drift	$\Delta V_{\text{OS}}/\Delta T$	(Note 5)		20	100	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_{B}	$T_A = +25^\circ\text{C}$ (Note 1) Over Temperature Range (Notes 1,2) C E M		0.01 1 3 50	10 10 30 500	nA
Input Resistance	R_{IN}			10^{11}		Ω
Open-Loop Voltage Gain	A_{VOL}	$R_L = 1000\Omega$ $R_L = 150\Omega$ $R_L = 75\Omega$	180 45 25	260 70 38		mV/gt V/V
Open-Loop Gain Drift	$\Delta A_{\text{VOL}}/\Delta T$	$R_L = 150\Omega$		0.5		%/°C
Common-Mode Rejection Ratio	CMRR	$-2\text{V} \leq V_{\text{IN}} \leq +2\text{V}$	60	80		dB
Power Supply Rejection Ratio	PSRR	$\pm 4.5\text{V}$ to $\pm 5.5\text{V}$	54	66		dB
Slew Rate	SR	(Note 5)	150	300		V/ μs

Note 1: Input bias current includes the multiplexer's ON-state leakage current for the MAX453, MAX454 and MAX455.

Note 2: Operating temperature range for "C" devices is 0°C to 70°C , for "E" devices is -40°C to $+85^\circ\text{C}$, and for "M" devices is -55°C to $+125^\circ\text{C}$.

Note 3: Input test signal: 3.58MHz sinewave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.

Note 4: Guaranteed over the voltage range, $V^- < V_{\text{IN}} < V^+$.

Note 5: Guaranteed by design.

(Continued on next page)

CMOS Video Multiplexer/Amplifier

ELECTRICAL CHARACTERISTICS MAX452/3/4/5 (Continued)

($V^+ = +5V$, $V^- = -5V$, $-2V < V_{IN} < +2V$, Output Load Resistor = 150Ω , $T_A = +25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VIDEO AMPLIFIER (MAX452/3/4/5)						
-3dB Bandwidth	GBW1	$A_V = 0dB$, $R_L = 75\Omega$ (Note 5)	30	50		MHz
-3dB Bandwidth	GBW2	$A_V = 6dB$, $R_L = 150\Omega$ (Note 5)	25	40		MHz
Differential Phase Error	DP	MAX452 (Notes 3, 5) MAX453/4/5 (Notes 3, 5)		0.2 1.2		deg
Differential Gain Error	DG	(Notes 3, 5)		0.5		%
Settling-Time to 1%	t_S	$\Delta V = 1V$, $R_L = 150\Omega$, $A_V = 6dB$		50		ns
Output Impedance	R_{OUT}	$f = 100kHz$, $A_V = 0dB$		2		Ω
Full-Scale Output Current	I_{OUT}	$R_L = 150\Omega$	± 14	± 20		mA
Output Voltage Swing	V_{OUT}	$R_L = 150\Omega$	± 2.1	± 3.0		V
Input Noise, dc to 40MHz	V_n	(Note 5)		0.15	0.5	mV_{rms}
Operating Supply Voltage	V^+, V^-		± 4.5		± 5.5	V
Supply Current	I_S	$V_{IN} = 0V$	20	25	30	mA
MULTIPLEXER (MAX453/4/5)						
Input Voltage Range	V_{IN}	Over Temperature	-2		2	V
OFF Input Leakage Current	I_{OFF}	$T_A = +25^\circ C$ (Note 4) Over Temperature Range (Notes 2, 4) C E M		0.01 1 3 50	10 10 30 500	nA
Logic Low Threshold	V_{IL}				0.8	V
Logic High Threshold	V_{IH}		2.4			V
Input Pullup/down Current	$I_{IL/IH}$			5	20	μA
Turn-ON Time	t_{ON}	(Note 5)		75	120	ns
Turn-OFF Time	t_{OFF}	(Note 5)		25	60	ns
Break-Before-Make Delay	t_D	(Note 5)	10	50		ns
Channel "ON" Capacitance	C_{ON}	(Note 5)		7	15	pF
Channel "OFF" Capacitance	C_{OFF}	(Note 5)		3.5	12	pF
Channel "OFF" Isolation	OIRR	$f_{IN} = 4MHz$, $R_S = 75\Omega$ (Note 5) Channel 2 to Channel 3 All other Channels	45 60	55 70		dB

Note 1: Input bias current includes the multiplexer's ON-state leakage current for the MAX453, MAX454 and MAX455.

Note 2: Operating temperature range for "C" devices is $0^\circ C$ to $70^\circ C$, for "E" devices is $-40^\circ C$ to $+85^\circ C$, and for "M" devices is $-55^\circ C$ to $+125^\circ C$.

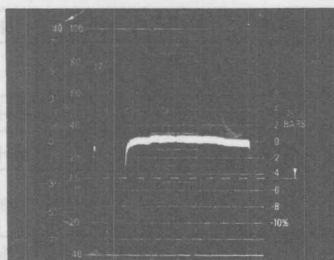
Note 3: Input test signal: 3.58MHz sinewave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.

Note 4: Guaranteed over the voltage range, $V^- < V_{IN} < V^+$.

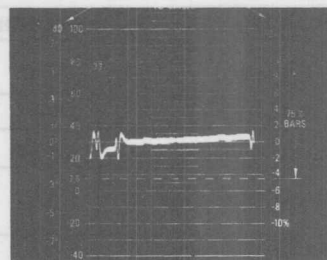
Note 5: Guaranteed by design.

CMOS Video Multiplexer/Amplifier

MAX452 AND MAX455 DIFFERENTIAL GAIN

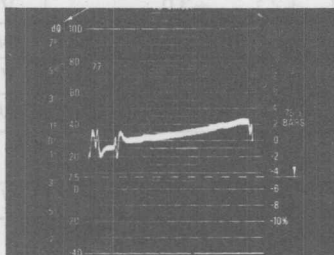


MAX452 DIFFERENTIAL PHASE

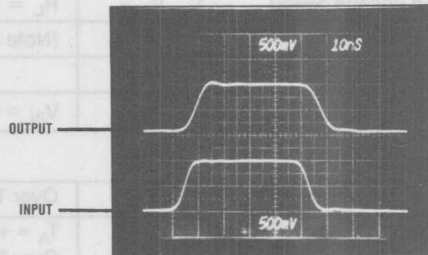


Input test signal: 3.58MHz sine wave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 ohm load.

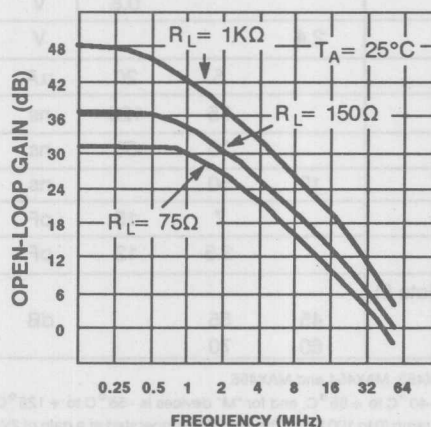
MAX455 DIFFERENTIAL PHASE



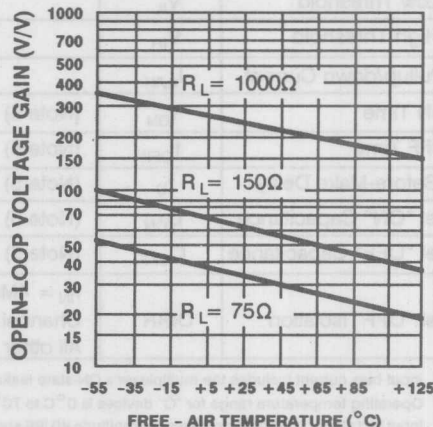
MAX455 PULSE RESPONSE



OPEN-LOOP GAIN vs. FREQUENCY



OPEN-LOOP GAIN vs. TEMPERATURE



CMOS Video Multiplexer/Amplifier

Pin Description

PIN NAME	PIN NUMBER				FUNCTION
	MAX452	MAX453	MAX454	MAX455	
V ⁺	6	6	12	18	Positive Supply, +5V
V ⁻	3	3	4	6	Negative Supply, -5V
V _{OUT}	8	8	14	20	Amplifier output
-IN	7	7	13	19	Amplifier's inverting input
+IN	5	-	-	-	Amplifier's non-inv. input
IN0	-	4	7	5	Analog input, channel 0
IN1	-	5	8	7	Analog input, channel 1
IN2	-	-	10	9	Analog input, channel 2
IN3	-	-	11	10	Analog input, channel 3
IN4	-	-	-	11	Analog input, channel 4
IN5	-	-	-	13	Analog input, channel 5
IN6	-	-	-	15	Analog input, channel 6
IN7	-	-	-	17	Analog input, channel 7
A2	-	-	-	1	Channel select, MSB
A1	-	-	1	2	Channel select
A0	-	1	2	3	Channel select, LSB
GND	-	2	3	4	Logic Ground

Detailed Description

The video amplifier is a low gain, wideband op-amp optimized for driving low impedance loads. Open-loop gain is about 40V/V with a 75 ohm load which introduces a small gain error. However, this can readily be trimmed by adjusting the gain-setting resistors.

The MAX452/3/4/5 series are unity-gain stable when driving resistive loads. They are optimized for driving 75 ohms at unity gain or 150 ohms at a gain of 2V/V with no frequency compensation components required. Generally, for the best transient response, the load resistance should be (in ohms) $75 \times \text{GAIN(V/V)}$. Thus, at a gain of +6dB (2V/V), the amplifier's optimal load is 150 ohms. If a higher resistive load is used, the amplifier will show peaking near its -3dB frequency. If a capacitive load is being driven, such as the input to a flash converter, the load should be "isolated" by a series resistor to limit amplifier ringing, see Figure 4.

The bandwidth of the amplifier is affected by both the closed-loop gain and the load resistor. Table 1 lists the -3dB rolloff frequency for a MAX453/4/5 with different gains and optimal resistive loads. The MAX452, which doesn't have the input multiplexer, runs about 20% higher in bandwidth.

Table 1.
Gain and Load Resistor Selection

GAIN (V/V)	f-3dB (MHz)	R1 (Ω)	R2 (Ω)	R _{load} (Ω)
1	50	0	∞	75
2	40	1k	1k	150
5	30	4k	1k	390
10	18	9k	1k	750

The multiplexers feature break-before-make switches to insure that no two channels are ever connected together. Low DC offset voltage and high bandwidth allow the MAX455 to be cascaded to form a 64 channel system while retaining video signal fidelity.

Figure 1 shows a typical application of the MAX455. The circuit is being used to drive a back terminated 75 ohm cable. R3 and R4 terminate the cable at both ends. R3 also attenuates the signal by a factor of two, so to make up for the signal loss, the amplifier is run at a gain of 2V/V. This arrangement provides unity gain from signal input to

CMOS Video Multiplexer/Amplifier

cable output. Amplifier closed-loop gain is set by R1 and R2 giving,

$$\frac{V_{OUT}}{V_{IN}} = \frac{G \times (R1 + R2)}{(G \times R2) + (R1 + R2)}$$

Where G is the open-loop gain of the amplifier, about 70V/V with a 150 ohm load. Capacitors C1 and C2 are power supply bypass capacitors.

Multiplexer channels are selected by the A0, A1, and A2 pins. These logic pins are compatible with either TTL or

CMOS logic. The GND pin (which is a logic ground, NOT an analog ground) should be connected to digital ground. Table 2 shows selected channels for the different states of the control lines. If A0, A1, and A2 are left floating, internal pullup/pulldown sources will hold A0 and A1 low, and A2 high. Thus, channel 0 is the default channel for the MAX453 and MAX454, while channel 4 is the default channel for the MAX455. Pullup/pulldown currents are typically around 5µA.

Table 2.
Channel Selection

MAX453		MAX454			MAX455			
A0	Channel	A1	A0	Channel	A2	A1	A0	Channel
L	0*	L	L	0*	L	L	L	0
H	1	L	H	1	L	L	H	1
		H	L	2	L	H	L	2
		H	H	3	L	H	H	3
					H	L	L	4*
					H	L	H	5
					H	H	L	6
					H	H	H	7

*Default channel if selection pins are left floating.

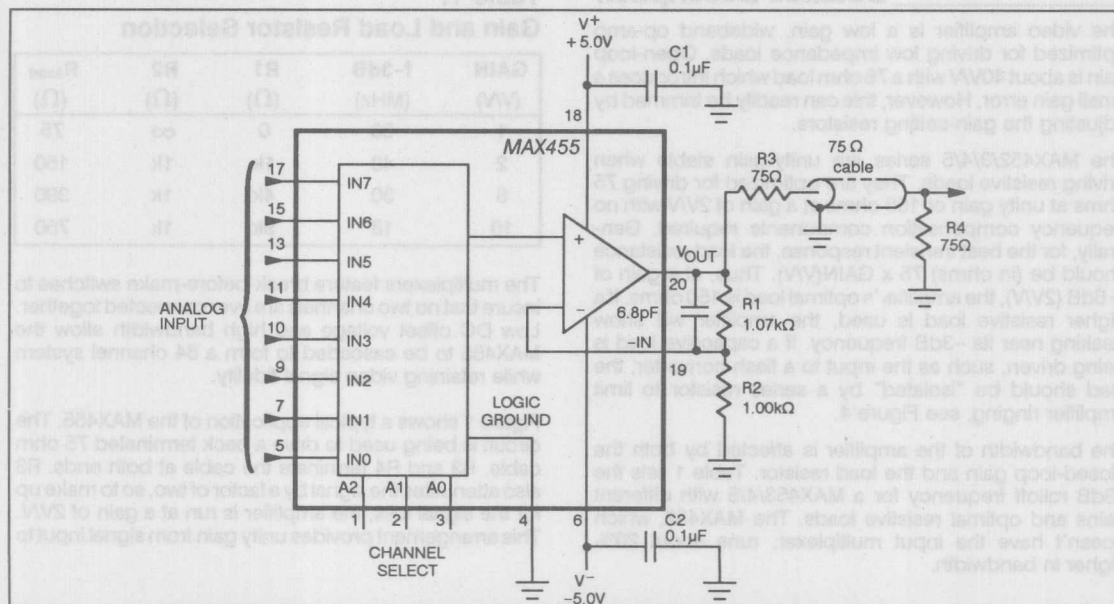


Figure 1. Typical Application

CMOS Video Multiplexer/Amplifier

MAX452/3/4/5

Typical Applications

Figure 2 shows the connections for a unity-gain amplifier. R1 and R2 adjust the gain to be nominally 1.00V/V. R3 is a 75 ohm load resistor. If precise unity-gain is not needed, R1 and R2 can be omitted and -IN can be connected directly to V_{OUT}.

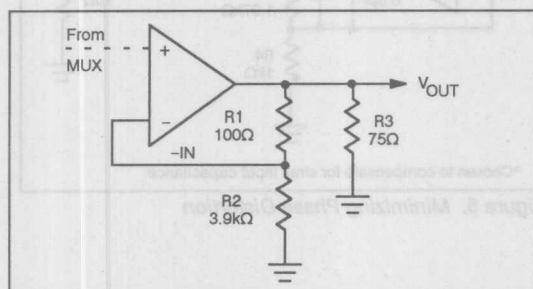


Figure 2. Unity-Gain Connections

Figure 3 shows how 64 channels can be multiplexed together. Eight MAX455s select 8 out of 64 channels, and a final MAX455 selects one of the 8 intermediate channels. The first eight MAX455s are connected as unity-gain amplifiers with 150 ohm load resistors. This results in a voltage gain of about 0.99V/V. The 150 ohm loads will also cause these unity-gain amplifiers to peak around 40MHz which tends to cancel the rolloff of the final amplifier running at a gain of 2V/V. The overall gain is adjusted by R1. The -3dB frequency is about 35MHz.

Figure 4 shows the amplifier driving a capacitive load. The 27 ohm resistor provides isolation between the capacitive

load and the amplifier output. This minimizes signal peaking at high frequencies. As a rule, the resistor should be chosen such that the RC product is 10ns or longer. This scheme shouldn't be used if R is greater than 150 ohms (or C is less than 100pF). The amplifier can drive 100pF directly without an isolation resistor.

The video amplifier is similar to a transconductance amplifier in that the output is a current proportional to the difference of the input voltage and the feedback voltage. G_m is about 0.5 mA/mV. The output impedance of the amplifier is around 1k ohms. This gives an unloaded voltage gain of,

$$G_m \times R_o = 500 \text{ V/V}$$

or about 54 dB.

Video signals are often of one polarity, e.g., ranging from 0 to +1V full scale. When amplifying these signals, phase distortion can be reduced by biasing the output stage of the video amplifier as shown in Figure 5. Here a signal is driven 0 to +2V into a 150 ohm load. R2 provides 6.5 mA of drive to the load at mid scale (1V). The amplifier, instead of supplying 0 to 13mA, supplies a more symmetric $\pm 8\text{mA}$ which reduces phase distortion to about 1 degree at 4 MHz. Because of the amplifier's finite gain of 0.5mA/mV, the current from R2 introduces an offset voltage. Adding R1 compensates for this offset. R3 and R4 set the closed-loop gain of the amplifier.

Care should be taken in laying out the printed circuit board connections to minimize cross-talk between channels. This can be augmented by using ground traces between the signal paths.

4

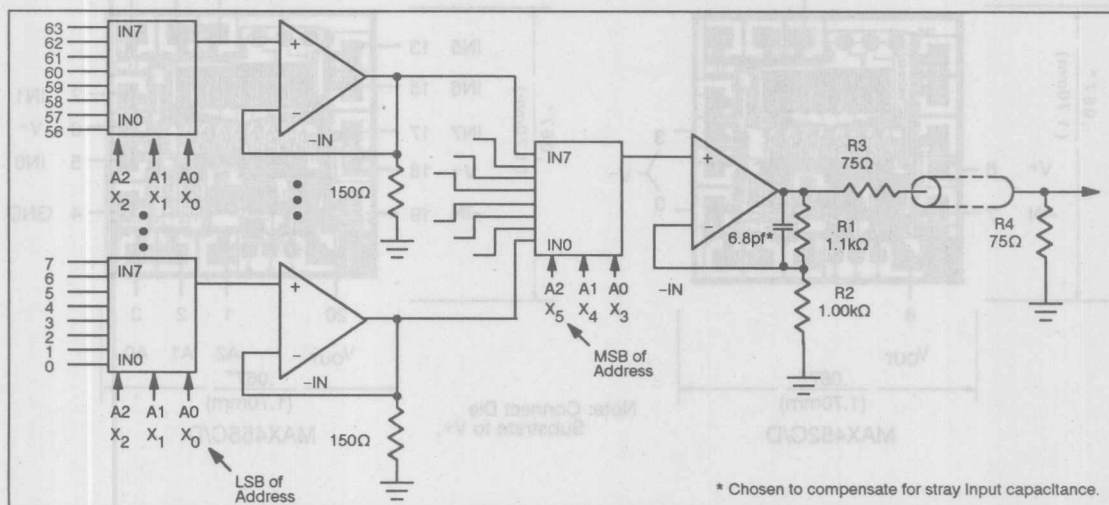


Figure 3. Nine MAX455s Used to Multiplex 64 Channels.

CMOS Video Multiplexer/Amplifier

Power supply voltages should be maintained to within $\pm 5\%$ of the nominal $\pm 5.00V$ values for optimum performance.

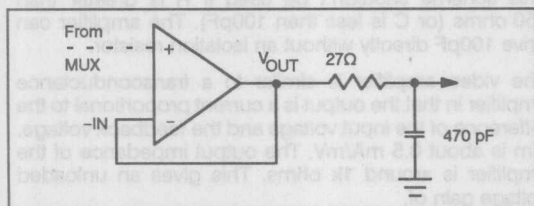


Figure 4. Isolating a Large Capacitive Load.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX454MJD	-55°C to +125°C	14 lead CERDIP
MAX455CPP	0°C to +70°C	20 lead plastic DIP
MAX455CWP	0°C to +70°C	20 lead small-outline
MAX455C/D	0°C to +70°C	Dice
MAX455EPP	-40°C to +85°C	20 lead plastic DIP
MAX455EJP	-40°C to +85°C	20 lead CERDIP
MAX455MJP	-55°C to +125°C	20 lead CERDIP

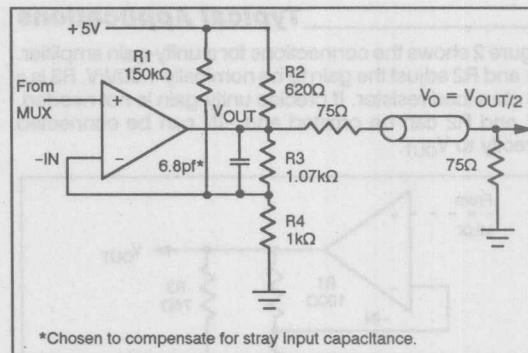
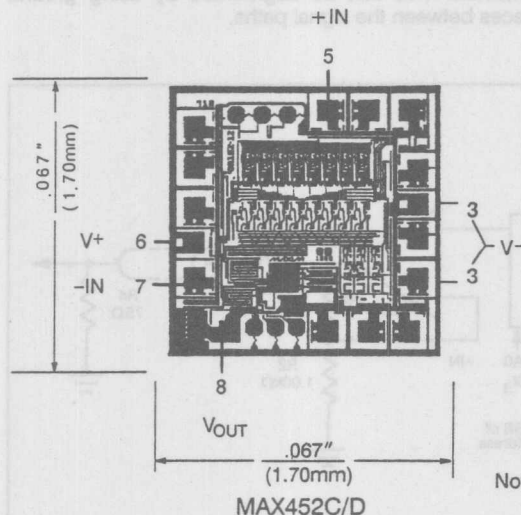
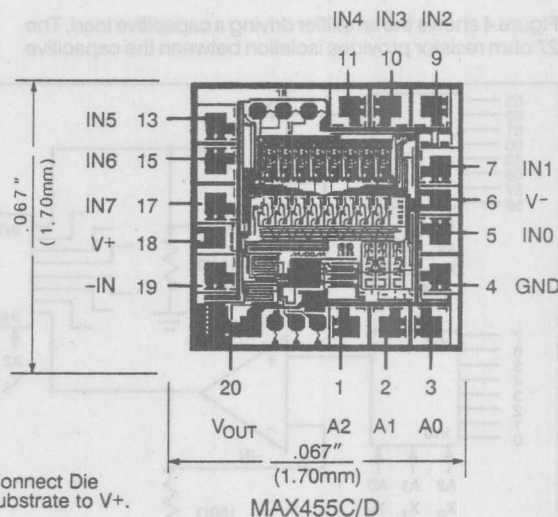


Figure 5. Minimizing Phase Distortion

Chip Topographies



Note: Connect Die Substrate to V+.



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MAXIM

Crosspoint Video Switch

MAX456

General Description

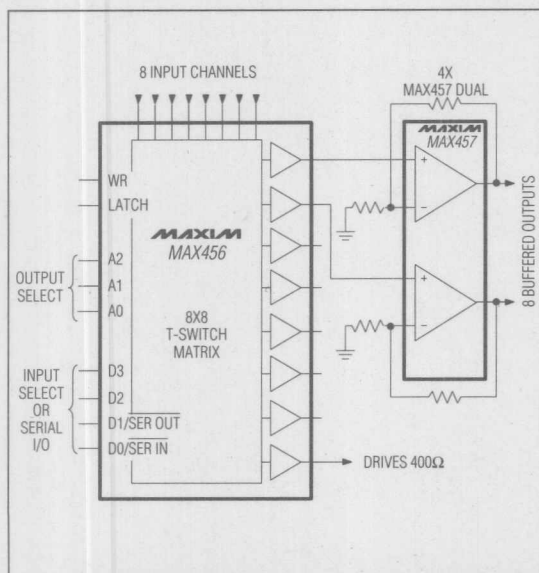
The MAX456 features a 64 T-switch matrix arranged for 8 input channels and 8 output channels. Each of the 8 matrix outputs drives an internal video amplifier that is capable of driving a load of 400Ω and 20pF to $\pm 1.2\text{V}$. Configuration data is entered into the MAX456 by a 7-bit parallel word, a 7-bit serial word, or a 32-bit serial stream. This data controls the T-switches, which allow each of the 8 output channels to be connected to any one of the 8 input analog channels.

The MAX456 pin out is arranged in a straight-through architecture. The analog inputs are on one side, and the outputs are on the other side with either a power-supply line or a "quiet" digital logic line positioned between each channel to minimize crosstalk. Furthermore, the outputs line up with 4 MAX457s (dual-video amplifiers), which drive 75Ω cables.

Applications

- Video Test Equipment
- Video Security Systems
- Video Editing

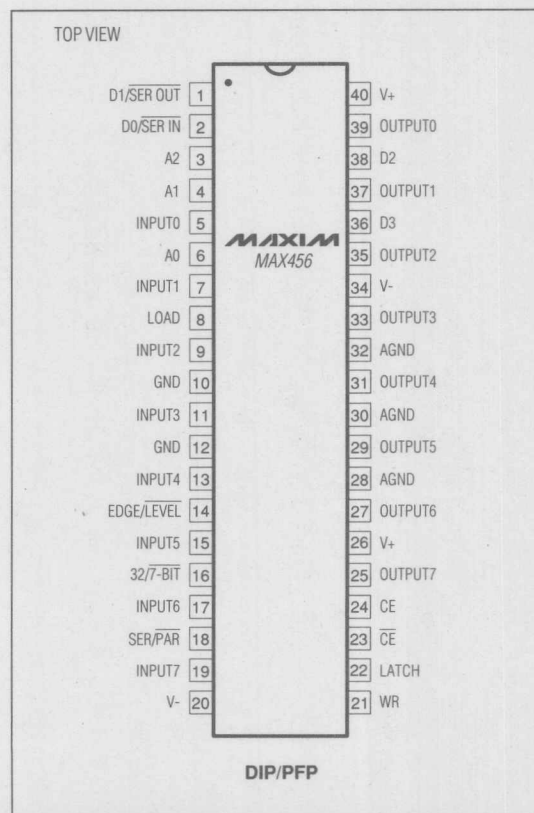
Functional Diagram



Features

- ◆ Programmability
- ◆ 3 Interface Modes - Serial or Parallel Digital Interface
- ◆ $250\text{V}/\mu\text{s}$ Slew Rate
- ◆ Internal 400Ω Load Terminations
- ◆ 0.3° Diff. Phase
- ◆ 60dB Off Isolation at 5MHz

Pin Configuration



MAXIM

Maxim Integrated Products 4-49

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Dual CMOS Video Amplifier

MAX457

General Description

The MAX457 contains two unity-gain stable video amplifiers that are capable of driving 75Ω loads with a -3dB bandwidth of 70MHz. The amplifiers operate from $\pm 5V$ supplies and together consume about 350mW of power. Closed loop gain is set by two external resistors. The pinout of the MAX457 follows that of conventional 8-pin, dual op amps.

The amplifiers require no external compensation and because of the CMOS process offer low input bias current of typically 100pA. The isolation between the amplifiers is typically 72dB at 5MHz and differential phase and gain are 0.2 degrees and 0.5% respectively.

Features

- ◆ Unity-Gain Bandwidth of 70MHz
- ◆ Low Input Capacitance: 4pF
- ◆ No Frequency Compensation Required
- ◆ Low Input Bias Current: 100pA
- ◆ Directly Drives 75Ω Cables
- ◆ High Isolation Between Amplifiers: 72dB at 5MHz
- ◆ Low Offset Voltage: 2mV

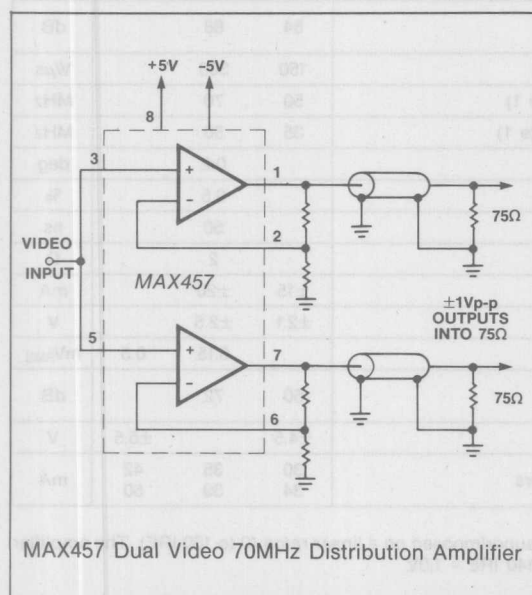
Applications

75 Ω Cable Drivers
Output Amplifiers for Video Crosspoint Switches
High Speed, Low Gain Applications
Driving Flash Converters
Video Distribution Amplifiers

Ordering Information

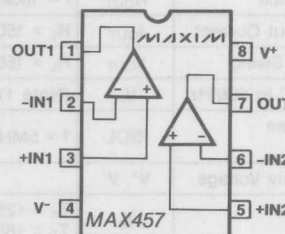
PART	TEMP. RANGE	PACKAGE
MAX457CPA	0°C to +70°C	8 Lead Plastic DIP
MAX457CSA	0°C to +70°C	8 Lead SO
MAX457C/D	0°C to +70°C	Dice
MAX457EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX457EJA	-40°C to +85°C	8 Lead Cerdip

Typical Operating Circuit



Pin Configuration

Top View



Dual CMOS Video Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	12V	Lead temperature (Soldering 10 sec)	+300°C
Analog Input Voltage	($V^+ + 0.3V$) to ($V^- - 0.3V$)	Duration of Output Short Circuit to Ground	Indefinite
Storage Temperature Range	-65°C to +150°C	Input Current, power on or off	$\pm 50mA$
Operating Temperature Range		Continuous Total Power Dissipation at 70°C	
MAX457CPA, MAX457CSA,		Plastic DIP (derate 8.3mW/°C above 70°C)	660mW
MAX457C/D	0°C to +70°C	CERDIP (derate 8.0mW/°C above 70°C)	640mW
MAX457EPA, MAX457EJA	-40°C to +85°C	Small Outline (derate 5.9mW/°C above 70°C)	470mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V^+ = +5V$, $V^- = -5V$, $-2V \leq V_{IN} \leq +2V$, Output Load Resistor = 150 Ω , $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Over Temperature Range	-2		+2	V
Input Offset Voltage	V_{OS}		-5	± 2	+5	mV
Offset Voltage Drift	dV_{OS}/dT			20	100	$\mu V/^\circ C$
Input Bias Current	I_B	$T_A = +25^\circ C$ $T_A = +70^\circ C$ $T_A = +85^\circ C$		0.1 5 15	1 40 100	nA
Input Resistance	R_{IN}	$T_A = +25^\circ C$		10		G Ω
Input Capacitance	C_{IN}	Plastic Package		4		pF
Open Loop Voltage Gain	A_{VOL}	$R_L = 1000\Omega$ $R_L = 150\Omega$ $R_L = 75\Omega$	200 45 25	300 65 35		V/V
Open Loop Gain Drift Temperature Coefficient	dA_{VOL}/dT	$R_L = 150\Omega$		-0.6		%/ $^\circ C$
Common Mode Rejection Ratio	CMRR	$-2V \leq V_{IN} \leq +2V$	54	66		dB
Power Supply Rejection Ratio	PSRR	$\pm 4.5V$ to $\pm 5.5V$	54	66		dB
Slew Rate	SR	(Note 1)	150	300		V/ μs
-3dB Bandwidth	GBW1	$A_V = 0dB$, $R_L = 75\Omega$ (Note 1)	50	70		MHz
-3dB Bandwidth	GBW2	$A_V = 6dB$, $R_L = 150\Omega$ (Note 1)	35	50		MHz
Differential Phase Error	DP	(Notes 1, 2)		0.2		deg
Differential Gain Error	DG	(Notes 1, 2)		0.5		%
Settling Time to 1%	t_S	$R_L = 150\Omega$, $A_V = 6dB$		50		ns
Output Impedance	R_{OUT}	$f = 100kHz$, $A_V = 0dB$		2		Ω
Full Scale Output Current	I_{OUT}	$R_L = 150\Omega$	± 15	± 20		mA
Output Voltage Swing	V_{OUT}	$R_L = 150\Omega$	± 2.1	± 2.5		V
Input Noise, DC to 50MHz	V_N	(Note 1)		0.15	0.5	mV _{RMS}
Isolation Between Amplifiers	ISOL	$f = 5MHz$ (Note 1)	60	72		dB
Operating Supply Voltage	V^+ , V^-		± 4.5		± 5.5	V
Supply Current	I_S	$T_A = +25^\circ C$ $T_A = +85^\circ C$ Both Amplifiers	30 34	35 39	42 50	mA

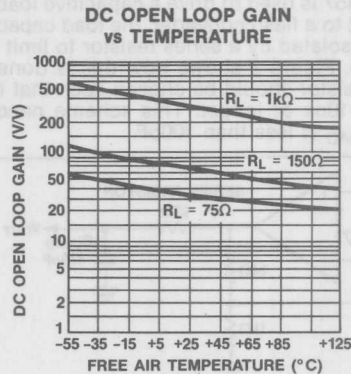
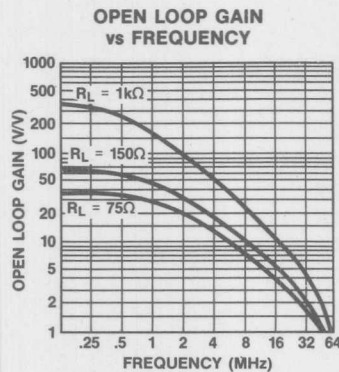
Note 1: Guaranteed by design.

Note 2: Input test signal: 3.58MHz sine wave of amplitude 40 IRE superimposed on a linear ramp (0 to 100 IRE). The amplifier is operated at a gain of 2V/V while driving a 150 Ω load. 140 IRE = 1.0V.

Dual CMOS Video Amplifier

Typical Operating Characteristics

MAX457



Detailed Description

The MAX457's dual video amplifiers are similar in design to the MAX452 single video amplifier, however, improvements have been made in gain linearity and bandwidth. The MAX457 video amplifier is similar to a transconductance amplifier that has an output current proportional to the difference of the voltages at the input terminals. That is,

$$I_{OUT} = G_m \times [(V_{IN}^+) - (V_{IN}^-)]$$

where G_m is about 0.6 amps/V. The output impedance of the amplifier is about 1.1kΩ. This gives an unloaded voltage gain of $G_m \times R_{OUT} = 660V/V$. This open loop gain is drastically reduced when driving conventional loads of 75 or 150Ω.

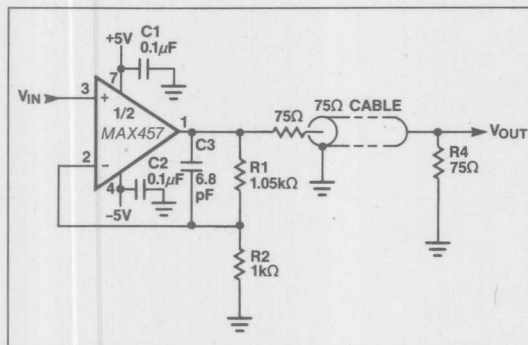


Figure 1. Typical Application

Figure 1 shows a typical application of one of the amplifiers of a MAX457 being used to drive a doubly terminated 75Ω cable. The closed loop gain of the amplifier is 2.00V/V. R_1 is 1.05kΩ instead of 1kΩ to make up for the low open loop gain of the MAX457. R_1 can be calculated from the following equation:

$$R_1 = [(AG + A - G)/(G - A)] \times R_2$$

where A is the closed loop gain of the amplifier, and G is the open loop gain of the amplifier (approximately equal to $G_m \times R_{LOAD}$). In this particular example, G_m is 0.6, R_{LOAD} is about 124Ω [$(R_{OUT}$ paralleled with $(R_1 + R_2)$ paralleled with 150Ω load)], and R_2 is 1kΩ. Thus, G is $0.6 \times 124 = 74.4V/V$, and A is 2V/V (the targeted closed loop gain value). This gives a value of 1.05kΩ for R_1 . C_1 and C_2 are power supply bypass capacitors. C_3 helps prevent peaking at high frequencies. This peaking results from the input capacitance of the amplifier which is driven by the relatively high impedance of the feedback resistors, R_1 and R_2 . At 50MHz, the feedback resistors cause a substantial phase delay. Adding C_3 eliminates this delay. At higher closed loop gains (about 5V/V or more), C_3 serves little purpose and should be omitted.

The MAX457 is unity gain stable when driving a 75Ω load. To insure that the amplifier doesn't oscillate, the load resistor should be nominally $75 \times A_{VCL}$, where A_{VCL} is the closed loop gain of the amplifier. Following this rule will result in a minimum amount of ringing or overshoot. Higher values may be used, but peaking of the output signal may occur in the 30 to 60MHz range. It is generally safe to use loads less than $150 \times A_{VCL}$. Table 1 gives suggested loads for various closed loop gains. R_2 is arbitrarily chosen to be 1kΩ. R_1 is calculated to give the nominal closed loop gain with the specified load. Note that the gain-bandwidth product increases as R_{LOAD} increases.

Table 1. Gain and Load Resistor Selection

GAIN (V/V)	f-3dB (MHz)	R1 (Ω)	R2 (Ω)	Rload (Ω)
1	70	39	1000	75
2	50	1050	1000	150
5	40	4170	1000	390
10	25	9420	1000	750

Dual CMOS Video Amplifier

If the MAX457 is used to drive a capacitive load, such as the input to a flash converter, the load capacitance should be isolated by a series resistor to limit amplifier ringing. Figure 2 shows how this is done. As a rule, the resistor should be chosen such that the RC product is 10ns or longer. This scheme needn't be used if C_{LOAD} is less than 100pF.

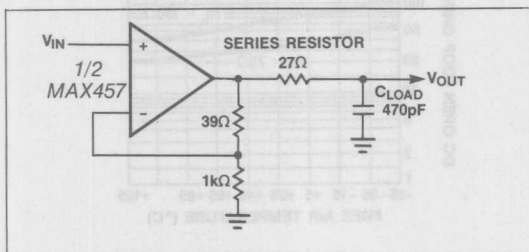
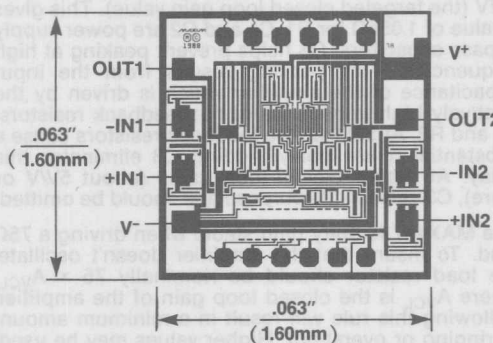


Figure 2. Isolating a Capacitive Load

Chip Topography



where A is the closed loop gain of the amplifier and G is the open loop gain of the amplifier (approx. 1000). In the particular case of the MAX457, $A = 1/2$ and $G = 1000$. Thus $R_2 = 100 \Omega$. This R_2 is chosen to give the nominal closed loop gain with the specified load. Note that the gain-bandwidth product increases as R_2 increases.

Table 1. Gain and Load Resistor Selection

Gain (V/V)	R_2 (Ω)	R_1 (Ω)	R_1 (k Ω)	R_1 (M Ω)
1	100	30	30	70
2	200	100	100	80
3	300	150	150	40
4	400	200	200	30
5	500	250	250	25

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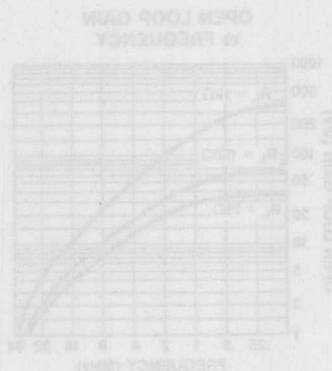


Figure 4. Typical Application

The MAX457's dual video amplifier is similar in design to the MAX455 single amplifier. However, improvements have been made in gain frequency and bandwidth. The MAX457 video amplifier is similar to a transconductance amplifier that has an output current proportional to the difference of the voltages at the input terminals. That is:

$$I_{OUT} = G_m \cdot (V_{IN1} - V_{IN2})$$

where G_m is about 0.5 amp/V. The output impedance of the amplifier is about 1.5k Ω . This gives an unloaded voltage gain of $G_m \cdot R_{OUT} = 800V/V$. The open loop gain is drastically reduced when driving conventional loads of 75 or 150 Ω .

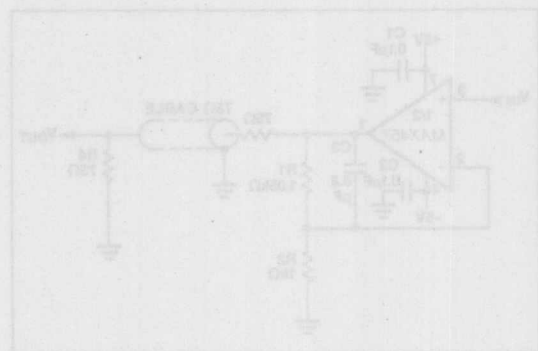


Figure 5. Typical Application

Figure 1 shows a typical application of one of the amplifiers of a MAX457 being used to drive a doubly terminated 75 Ω cable. The closed loop gain of the amplifier is 2.00V/V. R_1 is 1.05k Ω instead of 1k Ω to make up for the low open loop gain of the MAX457. R_1 can be calculated from the following equation:

High-Precision, Low-Voltage, Micropower Operational Amplifier

General Description

Maxim's new MAX480 is a precision micropower operational amplifier with flexible power-supply capability and superior DC performance characteristics over the industry standard OP90. The MAX480's guaranteed $70\mu\text{V}$ maximum offset voltage ($25\mu\text{V}$ typ) is the lowest of any other micropower op amp. This represents a better than two times improvement over the highest grade OP90A. Similarly, input bias current, input offset current and drift specifications are improved over the OP90 Family.

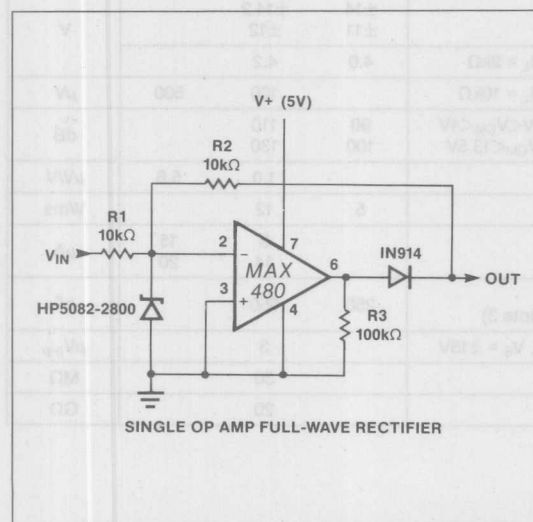
Both input and output voltage ranges include the negative supply rail, allowing maximum signal range capability in single-supply applications. The MAX480 operates with either single supplies ranging from $+1.6\text{V}$ to $+36\text{V}$ or dual supplies from $\pm 0.8\text{V}$ to $\pm 18\text{V}$. The MAX480 consumes less than $20\mu\text{A}$, allowing operation in excess of 10,000 hours from a 250mA-hr lithium coin cell. Even with a minimal quiescent current, the amplifier sinks or sources 5mA from its output.

The MAX480 is available in 8-pin DIP and Narrow Small Outline (SO) packages in commercial, extended and military temperature ranges.

Applications

Precision Micropower Amplifiers
Micropower Signal Processing
Battery-Powered Analog Circuits

Typical Operating Circuit



Features

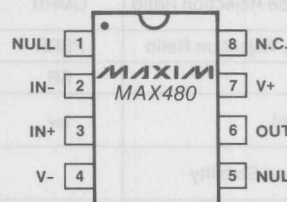
- ◆ Single- or Dual-Supply Operation: $+1.6\text{V}$ to $+36\text{V}$, $\pm 0.8\text{V}$ to $\pm 18\text{V}$
- ◆ True Single-Supply Operation: Input and Output Voltage Ranges Include Ground
- ◆ $1.5\mu\text{V}/^\circ\text{C}$ Max Offset Voltage Drift
- ◆ $20\mu\text{A}$ Max Supply Current
- ◆ 5mA Min Output Drive
- ◆ $70\mu\text{V}$ Max Input Offset Voltage
- ◆ 3nA Max Input Bias Current
- ◆ 700V/mV Min Open-Loop Gain
- ◆ Standard 741 Pin Out With Nulling to V-
- ◆ Improved OP90 Replacement

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX480CPA	0°C to $+70^\circ\text{C}$	8 Plastic DIP
MAX480CSA	0°C to $+70^\circ\text{C}$	8 Narrow SO
MAX480EPA	-40°C to $+85^\circ\text{C}$	8 Plastic DIP
MAX480ESA	-40°C to $+85^\circ\text{C}$	8 Narrow SO
MAX480MJA	-55°C to $+125^\circ\text{C}$	8 CERDIP

Pin Configuration

TOP VIEW



High-Precision, Low-Voltage, Micropower Operational Amplifier

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to V^-)	$\pm 18V$
Internal Power Dissipation	500mW
CERDIP (J) — derate at 8.0mW/°C above +70°C	
Plastic DIP (P) — derate at 6.9mW/°C above +70°C	
Small Outline (S) — derate at 5.88mW/°C above +70°C	
Differential Input Voltage	[(V^-)-20V] to [(V^+)+20V]
Common-Mode Input Voltage	[(V^-)-20V] to [(V^+)+20V]
Output Short-Circuit Duration	Indefinite

Operating Temperature Range	
MAX480 (CPA, CSA)	0°C to +70°C
MAX480 (EPA, ESA)	-40°C to +85°C
MAX480MJA	-55°C to +125°C
Junction Temperature (T_J)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Note 1: Absolute maximum ratings apply to packaged parts, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_S = \pm 1.5V$ to $\pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX480			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			25	70	μV
Input Offset Current	I_{OS}	$V_{CM} = 0V$		0.2	1	nA
Input Bias Current	I_B	$V_{CM} = 0V$		1	3	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$				V/mV
		$R_L = 100k\Omega$	700	1200		
		$R_L = 10k\Omega$	350	600		
		$R_L = 2k\Omega$	125	250		
		$V^+ = 5V$, $V^- = 0V$, $1V < V_O < 4V$				
		$R_L = 100k\Omega$	200	400		
		$R_L = 10k\Omega$	100	180		
Input Voltage Range	IVR	$V^+ = 5V$, $V^- = 0V$ $V_S = \pm 15V$ (Note 2)	0/4 -15/13.5			V
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 14 ± 11	± 14.2 ± 12		V
	V_{OH}	$V^+ = 5V$, $V^- = 0V$, $R_L = 2k\Omega$	4.0	4.2		
	V_{OL}	$V^+ = 5V$, $V^- = 0V$, $R_L = 10k\Omega$		100	500	μV
Common-Mode Rejection Ratio	CMRR	$V^+ = 5V$, $V^- = 0V$, $0V < V_{CM} < 4V$ $V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	90 100	110 130		dB
Power-Supply Rejection Ratio	PSRR			1.0	5.6	$\mu V/V$
Slew Rate	SR	$V_S = \pm 15V$	5	12		V/ms
Supply Current	I_{SY}	$V_S = \pm 1.5V$		9	15	μA
		$V_S = \pm 15V$		14	20	
Capacitive Load Stability		$A_V = +1$ No Oscillations (Note 3)	250	650		pF
Input Noise Voltage	e_{n-p-p}	$f_O = 0.1Hz$ to $10Hz$, $V_S = \pm 15V$		3		μV_{p-p}
Input Resistance Differential Mode	R_{IN}	$V_S = \pm 15V$		30		M Ω
Input Resistance Common Mode	R_{INCM}	$V_S = \pm 15V$		20		G Ω

High-Precision, Low-Voltage, Micropower Operational Amplifier

MAX480

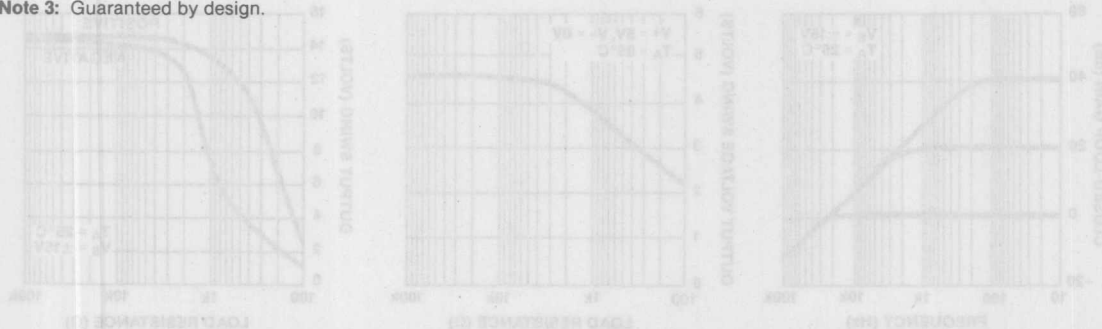
ELECTRICAL CHARACTERISTICS

($V_S = \pm 1.5V$ to $\pm 15V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX480C			MAX480E			MAX480M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			40	100		50	150		70	200	μV
Input Offset Voltage Drift	TCV_{OS}			0.3	1.5		0.3	1.5		0.3	1.5	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$		0.2	2.0		0.3	2.0		0.5	2.0	nA
Input Bias Current	I_B	$V_{CM} = 0V$		1	3		2	5		3	7	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V = \pm 10V$										V/mV
		$R_L = 100k\Omega$	500	950		500	800		225	400		
		$R_L = 10k\Omega$	250	400		250	400		125	240		
		$R_L = 2k\Omega$	75	125		75	150		50	110		
		$V_+ = 5V$, $V_- = 0V$, $1V < V_O < 4V$										
		$R_L = 100k\Omega$ $R_L = 10k\Omega$	150 75	360 150		150 75	280 140		100 50	200 110		
Input Voltage Range	IVR	$V_+ = 5V$, $V_- = 0V$ $V_S = \pm 15V$ (Note 2)	0/3.5 -15/13.5			0/3.5 -15/13.5			0/3.5 -15/13.5			V
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 13.5 ± 10.5	± 14 ± 11.8		± 13.5 ± 10.5	± 14 ± 11.8		± 13.5 ± 10.5	± 13.7 ± 11.5		V
	V_{OH}	$V_+ = 5V$, $V_- = 0V$ $R_L = 2k\Omega$	3.9	4.1		3.9	4.1		3.9	4.1		
	V_{OL}	$V_+ = 5V$, $V_- = 0V$ $R_L = 10k\Omega$		100	500		100	500		100	500	μV
Common-Mode Rejection Ratio	CMRR	$V_+ = 5V$, $V_- = 0V$, $0V < V_{CM} < 3.5V$	90	110		90	110		85	105		dB
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	100	120		100	120		95	115		
Power-Supply Rejection Ratio	PSRR			1.0	5.6		1.0	5.6		3.2	10	$\mu V/V$
Supply Current	I_{SY}	$V_S = \pm 1.5V$		12	25		13	25		15	25	μA
		$V_S = \pm 15V$		16	30		17	30		19	30	

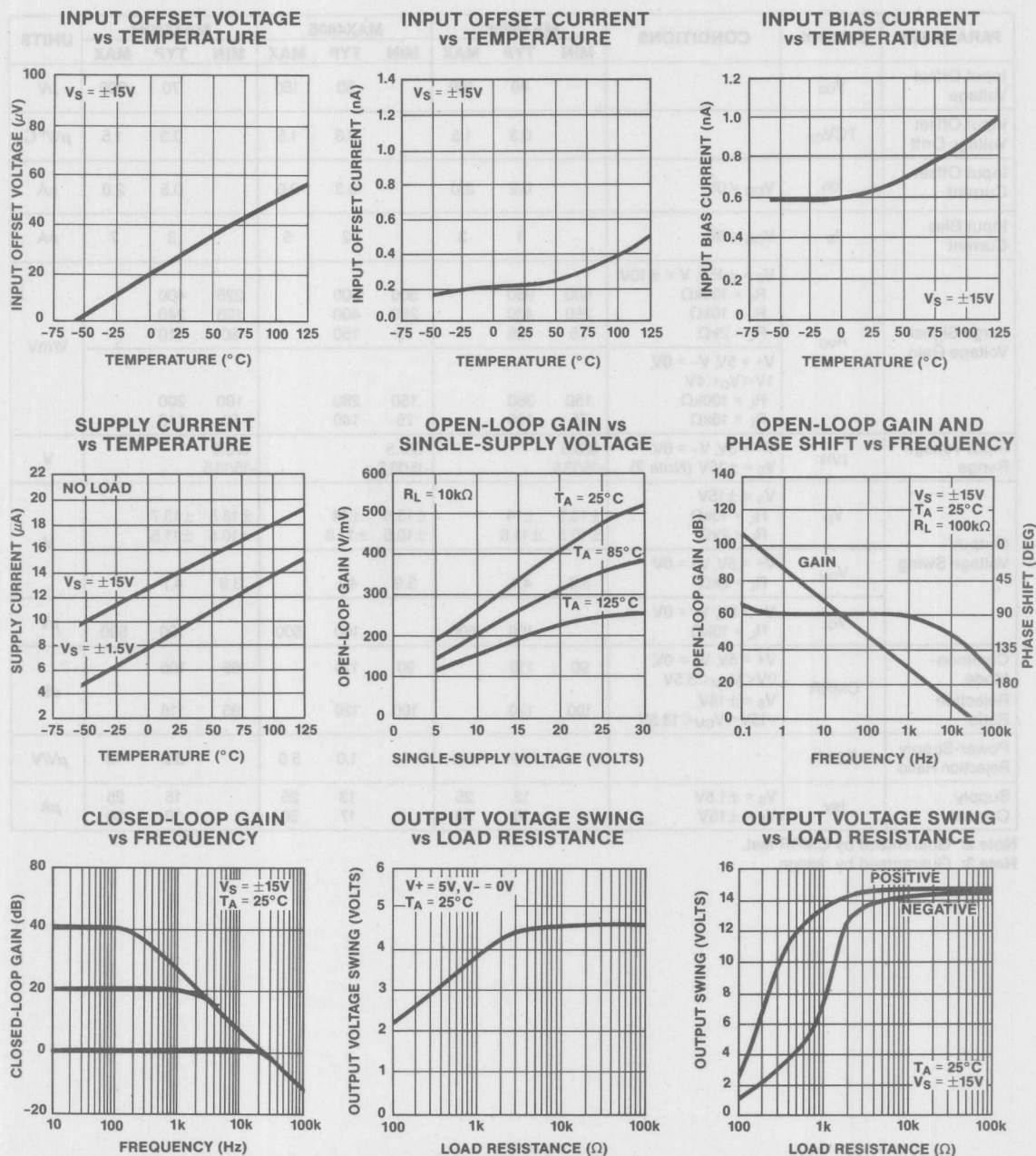
Note 2: Guaranteed by CMRR test.

Note 3: Guaranteed by design.



High-Precision, Low-Voltage, Micropower Operational Amplifier

Typical Operating Characteristics

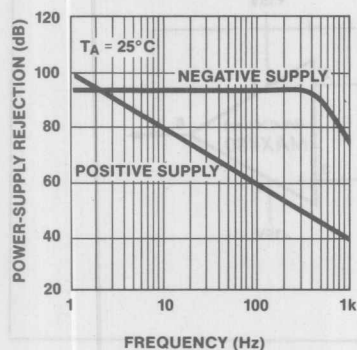


High-Precision, Low-Voltage, Micropower Operational Amplifier

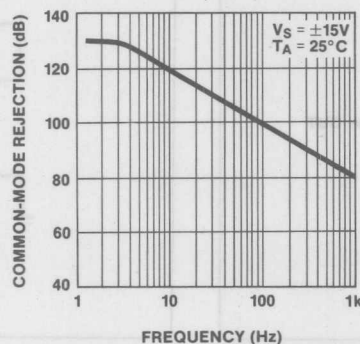
Typical Operating Characteristics (continued)

MAX480

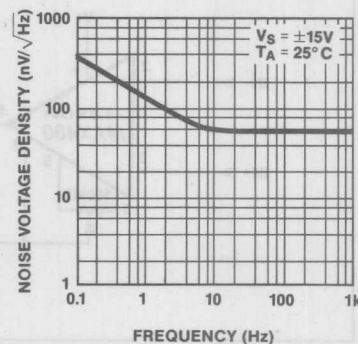
POWER-SUPPLY REJECTION
RATIO vs FREQUENCY



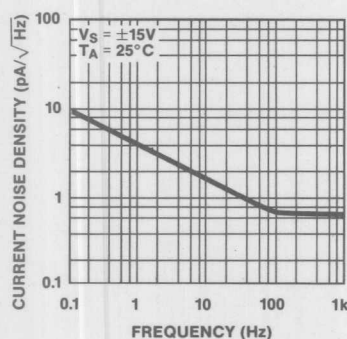
COMMON-MODE REJECTION
RATIO vs FREQUENCY



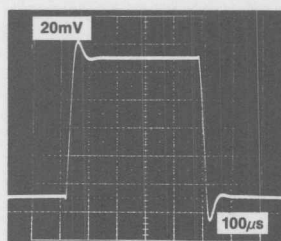
NOISE VOLTAGE DENSITY
vs FREQUENCY



CURRENT NOISE DENSITY
vs FREQUENCY

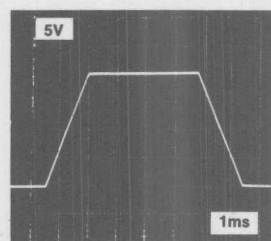


SMALL SIGNAL
TRANSIENT RESPONSE



TA = 25°C
VS = ±15V
AV = +1
RL = 10kΩ
CL = 500pF

LARGE SIGNAL
TRANSIENT RESPONSE



TA = 25°C
VS = ±15V
AV = +1
RL = 10kΩ
CL = 500pF

4

High-Precision, Low-Voltage, Micropower Operational Amplifier

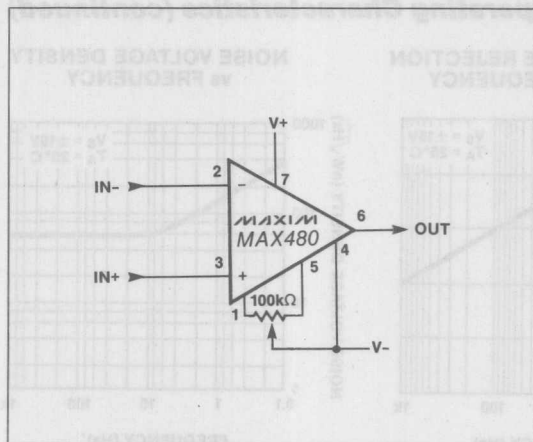


Figure 1. Offset Nulling Circuit

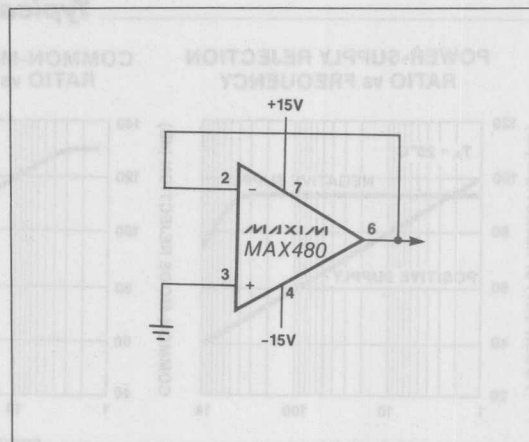


Figure 2. Burn-In Circuit

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

High-Speed, Low-Power Quad Voltage Comparators

General Description

The MAX900/MAX901 high-speed, low-power quad voltage comparators contain differential analog inputs and TTL logic outputs with active internal pullups. Propagation delay is 8ns with a 5mV input overdrive. By combining fast propagation delay with low power, the MAX900/MAX901 are ideal for a wide range of applications including fast A/D converters and sampling circuits, line receivers, V/F converters and many other general purpose data-discrimination applications.

Both comparators can be powered from separate analog and digital power supplies or from a single combined supply voltage. The analog input common-mode range includes the negative rail, allowing ground sensing when powered from a single supply. The MAX900/MAX901 power consumption is 70mW when powered from +5V.

The 4 comparators in the MAX900 are equipped with independent TTL compatible latch inputs. The comparator output states are held when the latch inputs are driven low. The MAX901 provides the same performance as the MAX900 with the exception of the latches. The MAX900/MAX901 are offered in 20- and 16-pin DIP and Wide SO packages, respectively.

Applications

High-Speed A/D Converters
High-Speed V/F Converters
Line Receivers
Threshold Detectors
Input Trigger Circuitry
High-Speed Data Sampling

Features

- ◆ 8ns Propagation Delay (Typ)
- ◆ 70mW Power Consumption (Typ at +5V)
- ◆ Separate Analog and Digital Supplies
- ◆ Flexible Analog Supply: +5V to +10V or ±5V
- ◆ Input Range Includes Negative Supply Rail
- ◆ TTL Compatible Outputs
- ◆ TTL Compatible Latch (MAX900 Only)

Ordering Information

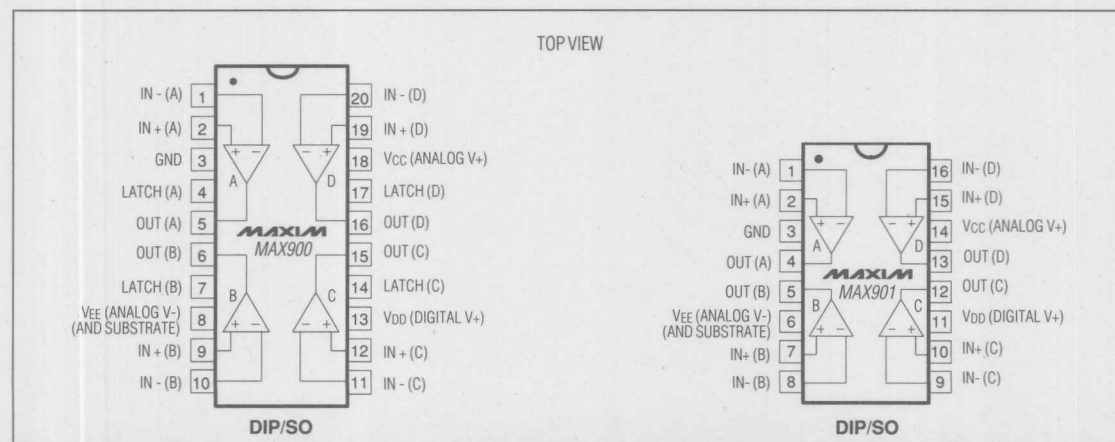
PART	TEMP. RANGE	PIN-PACKAGE
MAX900ACPP	0°C to +70°C	20 Plastic DIP
MAX900BCPP	0°C to +70°C	20 Plastic DIP
MAX900ACWP	0°C to +70°C	20 Wide SO
MAX900BCWP	0°C to +70°C	20 Wide SO
MAX900BC/D	0°C to +70°C	Dice*
MAX900AEPP	-40°C to +85°C	20 Plastic DIP
MAX900BEPP	-40°C to +85°C	20 Plastic DIP
MAX900AEWP	-40°C to +85°C	20 Wide SO
MAX900BEWP	-40°C to +85°C	20 Wide SO
MAX900AMJP	-55°C to +125°C	20 CERDIP
MAX900BMJP	-55°C to +125°C	20 CERDIP

* Consult factory for dice specifications.
Ordering information for MAX900 only.

MAX900/MAX901

4

Pin Configurations





Power-Supply Circuits

MAX631	CMOS Fixed/Adjustable Output Step-Up Switching Regulator	5-1
MAX632	CMOS Fixed/Adjustable Output Step-Up Switching Regulator	5-1
MAX633	CMOS Fixed/Adjustable Output Step-Up Switching Regulator	5-1
MAX635	Preset/Adjustable Output CMOS Inverting Switching Regulator	5-9
MAX636	Preset/Adjustable Output CMOS Inverting Switching Regulator	5-9
MAX637	Preset/Adjustable Output CMOS Inverting Switching Regulator	5-9
MAX638	+5V/Adjustable CMOS Step-Down Switching Regulator	5-17
MAX641	Fixed Output 10W CMOS Step-Up Switching Regulator	5-25
MAX642	Fixed Output 10W CMOS Step-Up Switching Regulator	5-25
MAX643	Fixed Output 10W CMOS Step-Up Switching Regulator	5-25
MAX650	-48V to +5V Output Switching DC-DC Converter	5-37
MAX654	Low Voltage Step-Up DC-DC Converter	5-47
MAX655	Low Voltage Step-Up DC-DC Converter	5-47
MAX656	Low Voltage Step-Up DC-DC Converter	5-47
MAX657	Low Voltage Step-Up DC-DC Converter	5-47
MAX658	Low Voltage Step-Up DC-DC Converter	5-47
MAX659	Low Voltage Step-Up DC-DC Converter	5-47
MAX663	CMOS +5V/Adjustable Micropower Positive Voltage Regulator	5-59
MAX664	CMOS +5V/Adjustable Micropower Negative Voltage Regulator	5-59
MAX666	CMOS +5V/Adjustable Voltage Regulator with Low Battery Detect	5-59
MAX667	+5V/Programmable Low-Dropout Voltage Regulator	5-67
MAX680	+5V to ± 10 V Voltage Converter	5-69
MAX681	+5V to ± 10 V Voltage Converter	5-69
MAX690	Microprocessor Watchdog/Battery Switchover/Reset Generator	5-75
MAX691	Microprocessor Watchdog/Battery Switchover/Reset Generator	5-75
MAX692	Microprocessor Watchdog/Battery Switchover/Reset Generator	5-75
MAX693	Microprocessor Watchdog/Battery Switchover/Reset Generator	5-75
MAX694	Microprocessor Supervisory Circuit/Battery Switchover/Reset Generator	5-75
MAX695	Microprocessor Watchdog/Battery Switchover/Reset Generator	5-75
MAX698	Low Cost Power-On Reset	5-89
MAX699	Low Cost Power-On Reset and Watchdog Controller	5-89
MAX700	Power-Supply Monitor with Reset	5-93
MAX701	Power-Supply Monitor with Reset	5-93
MAX702	Power-Supply Monitor with Reset	5-93
MAX742	Dual-Output, Switch-Mode Regulator (+5V to ± 15 V or ± 12 V)	5-97
MAX743	Dual-Output, Switch-Mode Regulator (+5V to ± 15 V or ± 12 V)	5-99
MAX790	High-Performance Supervisory Circuit	5-103
MAX791	High-Performance Supervisory Circuit	5-103

MAXIM

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

General Description

The MAX631, MAX632, and MAX633 are +5V, +12V, and +15V fixed output, step-up DC-DC converters for use in low-power, high-efficiency switching regulator applications. The only external components required are an output filter capacitor and a low-cost inductor. Included on-chip are low battery detection circuitry and a charge pump output for generating a negative voltage in dual-supply applications.

Though most simply used as fixed output regulators, the MAX631/632/633 can also be set for other output voltages by adding an external voltage divider.

Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters, with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive.

Applications

Minimum Component, High-Efficiency DC-DC Converters

Portable Instruments

Rechargeable and Primary Battery Power Conversion

Uninterruptable On-Board Power Supplies

Card Level Multiple Power Conversion

Features

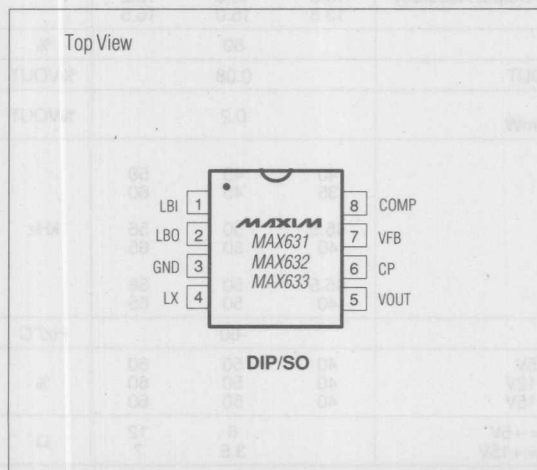
- ◆ Fixed +5V, +12V, +15V Output Voltages
- ◆ Adjustable Output with 2 Resistors
- ◆ 80% Typ Efficiency
- ◆ Only 2 External Components
- ◆ Charge Pump for Negative Output
- ◆ 135µA Typ Operating Current

Ordering Information

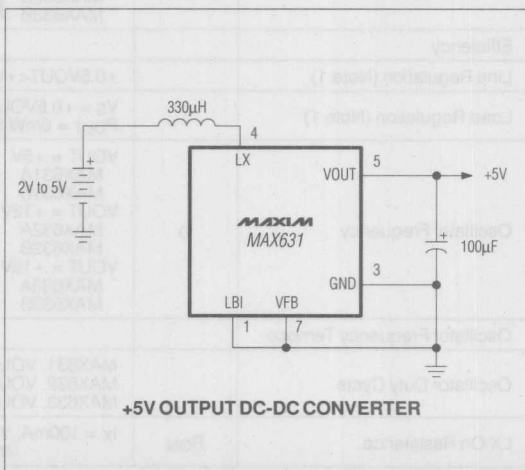
PART*	TEMP. RANGE	PIN-PACKAGE
MAX631XCPA	0°C to +70°C	8 Plastic DIP
MAX631XCSA	0°C to +70°C	8 Narrow SO
MAX631XC/D	0°C to +70°C	Dice
MAX631XEPA	-40°C to +85°C	8 Plastic DIP
MAX631XESA	-40°C to +85°C	8 Narrow SO
MAX631XEJA	-40°C to +85°C	8 CERDIP
MAX631XMJA	-55°C to +125°C	8 CERDIP
MAX632XCPA	0°C to +70°C	8 Plastic DIP
MAX632XCSA	0°C to +70°C	8 Narrow SO
MAX632XC/D	0°C to +70°C	Dice
MAX632XEPA	-40°C to +85°C	8 Plastic DIP
MAX632XESA	-40°C to +85°C	8 Narrow SO
MAX632XEJA	-40°C to +85°C	8 CERDIP
MAX632XMJA	-55°C to +125°C	8 CERDIP

* X = A for 5% Output Accuracy. X = B for 10% Accuracy.
Ordering Information continued on last page.

Pin Configuration



Typical Operating Circuit



MAX631/632/633

5

MAXIM

Maxim Integrated Products 5-1

MAXIM is a registered trademark of Maxim Integrated Products.
Dual Mode is a trademark of Maxim Integrated Products.

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VOUT	+18V
Output Voltage, LX and LBO	+18V
Input Voltage, LBI and VFB	-0.3V to (VOUT + 0.3V)
LX Output Current	450mA Peak
LBO Output Current	50mA
Power Dissipation	
Plastic DIP (derate 8.33mW/°C above +50°C)	625mW
SO (derate 6mW/°C above +50°C)	450mW
CERDIP (derate 8mW/°C above +50°C)	800mW

Operating Temperature Range

MAX63_XC	0°C to +70°C
MAX63_XE	-40°C to +85°C
MAX63_XM	-55°C to +125°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range		Voltage at VOUT Over Temperature (C, E) Over Temperature (M)	2.0 2.4		16.5 16.5	V
Start-up Voltage		Voltage at VOUT T _A = +25°C Over Temperature (C, E) Over Temperature (M)	1.5 1.8 2.0	1.3		V
Supply Current	I _S	LX off, Over Temperature VOUT = +5V, MAX631 VOUT = +12V, MAX632 VOUT = +15V, MAX633		0.135 0.5 0.75	0.4 2.0 2.5	mA
Reference Voltage (Internal)		T _A = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
VOUT Voltage		No Load, VFB = GND Over Temperature MAX631A MAX632A MAX633A MAX631B MAX632B MAX633B	4.75 11.4 14.25 4.5 10.8 13.5	5.0 12.0 15.0 5.0 12.0 15.0	5.25 12.6 15.75 5.5 13.2 16.5	V
Efficiency				80		%
Line Regulation (Note 1)		+0.5VOUT < +V _S < VOUT		0.08		%VOUT
Load Regulation (Note 1)		V _S = +0.5VOUT, P _{OUT} = 0mW to 150mW		0.2		%VOUT
Oscillator Frequency	f _o	VOUT = +5V MAX631A MAX631B VOUT = +12V MAX632A MAX632B VOUT = +15V MAX633A MAX633B	40 35 45.5 40 45.5 40	45 45 50 50 50 50	50 60 56 65 56 65	kHz
Oscillator Frequency Tempco				-60		Hz/°C
Oscillator Duty Cycle		MAX631, VOUT = +5V MAX632, VOUT = +12V MAX633, VOUT = +15V	40 40 40	50 50 50	60 60 60	%
LX On Resistance	R _{ON}	I _L = 100mA, VOUT = +5V VOUT = +15V		6 3.5	12 7	Ω

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

MAX631/632/633

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Leakage Current	I _{XL}	V ₄ = +16.5V T _A = +25°C Over Temperature (C, E) Over Temperature (M)		0.01	1.0 30 100	μA
Diode Forward Voltage	V _F	I _F = 100mA			1.0	V
CP On Resistance		V _{OUT} = +5V, I _{OUT} = ±10mA V _{OUT} = +15V, I _{OUT} = ±30mA		70 30	140	Ω
VFB Input Bias Current	I _{FB}			0.01	10	nA
Low Battery Input Threshold	V _{LBI}			1.31		V
Low Battery Input Bias Current	I _{LBI}			0.01	10	nA
Low Battery Output Current	I _{LBO}	V ₂ = +0.4V, V ₁ = +1.1V T _A = +25°C Over Temperature	0.5	1.0		mA
Low Battery Output Leakage Current	I _{LBOL}	V ₂ = +16.5V, V ₁ = +1.4V		0.01	3.0	μA

Note 1: Guaranteed by correlation with DC pulse measurements.

Pin Description

PIN	NAME	FUNCTION
1	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the Low Battery Detector threshold (1.31V), LBO sinks current.
2	LBO	The Low Battery Detector Output is an open drain N-channel MOSFET which sinks current when LBI is below 1.31V.
3	GND	Ground
4	LX	This pin drives the external inductor with an internal N-channel power MOSFET. LX has an output resistance of typically 6Ω and a peak current rating of 425mA.
5	VOUT	The regulated DC-DC converter output.
6	CP	The Charge Pump output is a low impedance buffer which swings from GND to VOUT at the oscillator frequency. 2 external capacitors and diodes can be connected to generate a negative output voltage (Figure 3).
7	VFB	When VFB is grounded, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected from VOUT to VFB and GND, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between VOUT and COMP reduces low-frequency ripple and improves transient response.

Typical Applications

Basic Step-Up Circuits

Figure 1 shows the basic boost or step-up circuit for the MAX631/632/633. The circuit corresponds to Table 1 which shows values for typical input voltages and output currents.

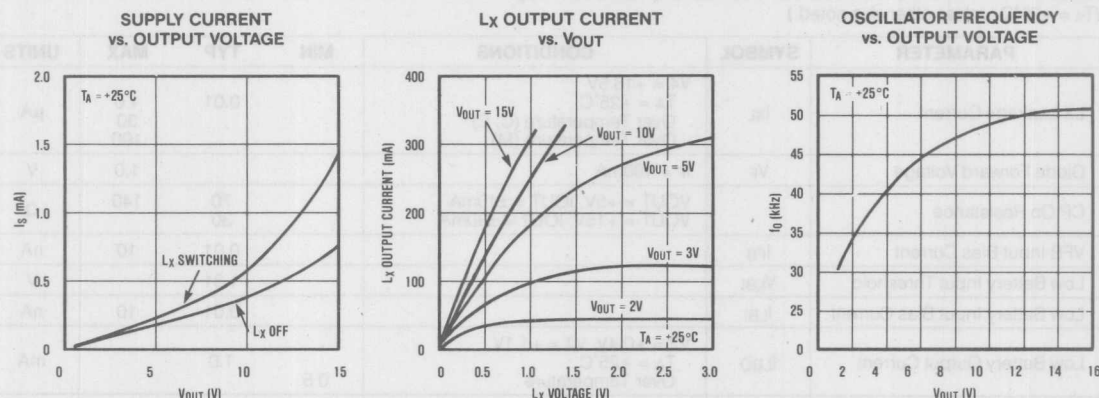
Table 1. Inductor Selection for Common Designs

V _{IN} (V)	V _{OUT} (V)	I _{OUT} (mA)	EFF. (%)	INDUCTOR		
				P.N. (Note 2)	μH	Ω
2	5	5	78	CB 6860-21	470	0.4
2	5	10	74	G 1B253	250	0.44
2	5	15	61	G 1B103	100	0.25
3	5	25	82	CB 6860-21	470	0.4
3	5	40	75	CB 7070-29	220	0.55
3	12	5	79	CB 6860-19	330	0.35
3	12	10	79	CB 7070-28	180	0.48
5	12	12	88	CB 6860-21	470	0.4
5	12	25	87	CB 6860-19	330	0.35
3	15	5	73	CB 7070-29	220	0.55
3	15	8	71	CB 7070-27	150	0.43
5	15	10	85	CB 6860-21	470	0.4
5	15	15	85	CB 6860-19	330	0.35
8	15	35	90	G 1B503	500	0.56

Note 2: CB = Cadell-Burns, NY, (516) 746-2310
G = Gowanda Electronics Corp., NY, (716) 532-2234
Other Manufacturers listed in Table 2.

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

Typical Operating Characteristics



Detailed Description

The operation of the MAX631/632/633 can best be understood by examining the regulating loop of Figure 1. When the output voltage drops below the preset (or externally set) value, the Error Comparator switches high and connects the internal 45kHz Oscillator to the gate of the LX output driver, N1. N1 is an N-channel MOSFET with a typical on resistance of 6Ω and a current rating of 150mA. The following equation provides a good rule of thumb to see if the MAX631/632/633 can provide the desired output current without exceeding the current rating of N1:

$$\frac{8(V_{OUT} - V_{IN}) I_{OUT}}{V_{IN}} \leq 450\text{mA}$$

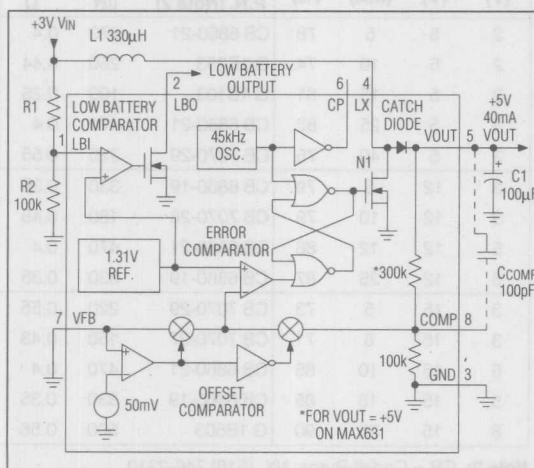


Figure 1. +3V to +5V Converter and Block Diagram

A low output voltage turns N1 on and off at the internal clock frequency. During each on half-cycle, the current through the inductor rises linearly, storing energy in the coil. During each off half-cycle, the coil's magnetic field collapses and voltage across the inductor reverses sign. The voltage at LX then rises until the internal diode is forward biased, delivering power to the output. When the output voltage reaches the desired level, the Error Comparator inhibits N1 until the load discharges the output filter capacitor (C1) to less than the desired output level.

VIN, Bootstrapped Operation

The MAX631/632/633 does not have a VIN pin. Input power to start the DC-DC converter is supplied via the external inductor to the VOUT pin. Once the converter has started, it is then powered from its own output. This "bootstrap" design ensures that the output MOSFET, N1, will have maximum gate drive and, hence, a minimum RON. It also allows the converter to start at lower input voltages.

VIN, Greater Than VOUT

If the regulator's input voltage is more than one forward diode drop greater than the desired output voltage, N1 will not turn on. Current will still be supplied to the load directly through the inductor and the internal diode, but without regulation. As long as the input is more than 0.6V above the desired output, the actual output voltage will be equal to the input voltage minus 0.6V.

Fixed or Adjustable Output

For operation at one of the preset output voltages (+5V for the MAX631, +12V for the MAX632, and +15V for the MAX633), VFB is connected to GND, and no external resistors are required. For an output voltage other than the preset value, an external voltage divider (R3 and R4, Figure 2) is required. VOUT is set as follows:

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R3 = R4 \left(\frac{V_{OUT}}{1.31V} - 1 \right)$$

Table 1 shows nominal inductor parameters for a variety of input and output voltages. Values are given for both maximum output and maximum efficiency designs. When noise is not critical, a low-cost bobbin inductor will suffice. For higher power circuits or when low EMI and noise are required, pot cores and toroids should be used. (See Tables 1 and 2 for typical part numbers and manufacturers.)

Table 2. Coil and Core Manufacturers (Note 3)

MANUFACTURER	TYPICAL PART #	DESCRIPTION
BOBBIN INDUCTORS		
Dale	IHA-104	500μH, 0.5Ω
Caddell-Burns	7070-29	220μH, 0.55Ω
Gowanda	1B253	250μH, 0.44Ω
TRW	LL-500	500μH, 0.75Ω
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82Ω
TRW	MH-1	600μH, 1.9Ω
Gowanda	050AT1003	100μH, 0.05Ω
FERRITE CORES AND TOROIDS (Note 4)		
Siemens	B64290-K38-X38	Tor. Core, 4μH/T ²
Magnetics	555.130	Tor. Core, 53nH/T ²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T ²

Note 3: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Note 4: Permag Corp. is a distributor for many of the listed core and toroid manufacturers. (516) 822-3311.

Output Filter Capacitor

The MAX631/632/633's output ripple has 2 components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often

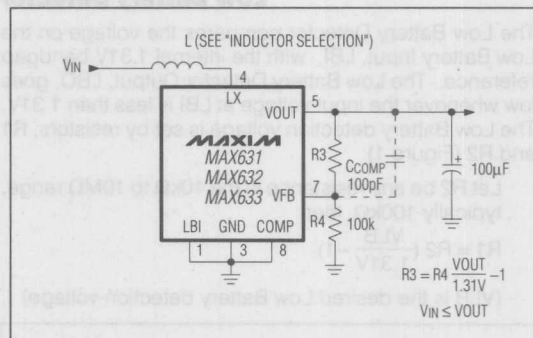


Figure 2. Connections for Adjustable Output

larger than that caused by the change in charge. Consequently, high-quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at a reasonable cost are typically achieved with a high-quality aluminum electrolytic, in the 100μF to 500μF range, in parallel with a 0.1μF ceramic capacitor.

Catch Diode

The MAX631 series regulators contain an internal "catch" diode and, therefore, require no external diode for most applications. However, an external diode can be connected in parallel with the internal diode at the LX and VOUT pins. For example, a Schottky diode with a low forward voltage drop will provide some improvement in efficiency.

Bypassing and Compensation

Since the inductor charging current can be relatively large, high currents flow through the ground connection to the MAX631/632/633. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and power-supply bypassing should be used.

When the value of the voltage setting resistors (R3 and R4, Figure 2) exceed 50kΩ, stray capacitance at the VFB input can add a "lag" to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the VFB node. It can also be remedied by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

The COMP input allows access to the internal voltage divider so that compensation can also be added when fixed output operation is used. A capacitor connected between VOUT and COMP again adds a "lead" to the regulator's response.

MAX631/632/633

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CMOS Fixed/Adjustable Output Step-Up Switching Regulators

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input, LBI, with the internal 1.31V bandgap reference. The Low Battery Detector Output, LBO, goes low whenever the input voltage at LBI is less than 1.31V. The Low Battery detection voltage is set by resistors, R1 and R2 (Figure 1).

Let R2 be any resistance in the 10k Ω to 10M Ω range, typically 100k Ω , then:

$$R1 = R2 \left(\frac{V_{LB}}{1.31V} - 1 \right)$$

(VLB is the desired Low Battery detection voltage)

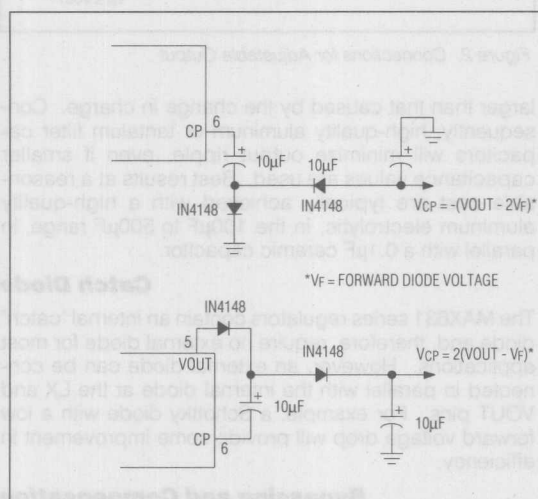


Figure 3. Using the Charge Pump (CP) output as a voltage inverter and/or doubler. Both circuits can be used together.

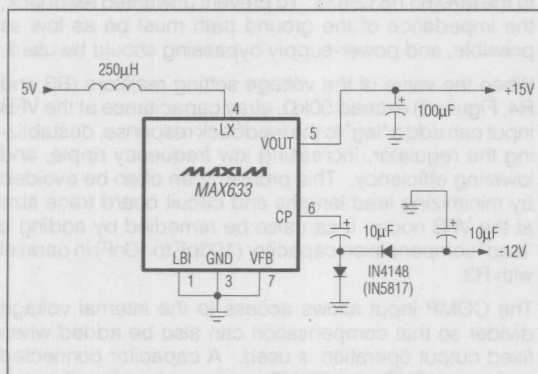


Figure 4. +5V to +15V/-12V Converter

Negative Output Voltage

The Charge Pump (CP) output is a low impedance buffer which swings from ground to VOUT at the oscillator frequency. Two external capacitors and diodes can be connected, as shown in Figure 3, to generate a negative output voltage of $-(VOUT - 1.2V)$ or a positive output of $2(VOUT - 1.2V)$. 1.2V is the forward drop of 2 silicon diodes. Both circuits can be used at once if desired. With 10 μ F capacitors, the output impedance of VCP is about 30 Ω . If space is critical, the capacitors can be reduced, but with a slight increase in output impedance and VCP output ripple.

The circuit shown in Figure 4 provides approximately $\pm 10mA$ with VOUT = +15V, and $\pm 15mA$ if VOUT = +12V. The magnitude of the negative output is about 3V less than VOUT due to the forward voltage drop of the 1N4148 diodes and the output impedance of CP. Using Schottky diodes (IN5817) will increase the absolute value of the negative output by about 1V. The performance of the CP output is shown in Figure 5.

What Value of Inductor?

A General Discussion

The converters in this data sheet operate by charging an inductor from a DC input and then discharging the inductor to generate a DC output that is greater than the input.

The proper inductor for any DC-DC converter depends on three things: the desired output power, the input voltage (or range of input voltage), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This, along with the input

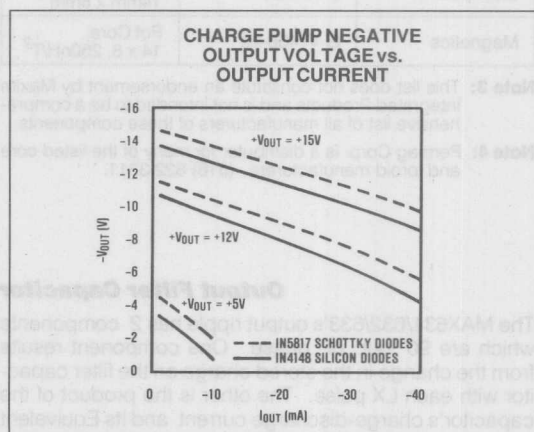


Figure 5. Charge Pump Negative Output Voltage vs. Current

CMOS Fixed/Adjustable Output Step-Up Switching Regulators

MAX631/632/633

voltage, determines how much energy will be stored in the coil.

The inductor must meet four electrical criteria:

[] **Value-** Low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case conditions for high power-switch transistor on time and high input voltage.

[] **Saturation-** The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[] **EMI-** Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for digital circuits; toroid or pot core types work well for EMI-sensitive analog circuits.

[] **DC resistance-** Winding resistance must be adequately low so efficiency is not affected and self-heating does not occur. Values less than 0.5Ω are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX631/632/633 operating frequency.

Inductor Value- Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst-case is:

- [] Maximum load current
- [] Minimum supply voltage
- [] Maximum inductor value, including tolerance
- [] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
- [] Worst-case low on time

Inductor Value- High Enough?

The inductor value must also be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. All kinds of odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values may result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

- [] Maximum supply voltage
- [] Minimum inductor value, including tolerance

- [] Minimum on resistance of the switch
- [] Low switching frequency (or maximum switch on-time)

Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for lowest ripple.

$$[1] I_{pk} = \frac{V_{OUT} + V_{DIODE} - V_{IN}}{(0.25)(V_{IN} - V_{SW})} (I_{OUT})$$

$$[2] L = \frac{V_{IN} - V_{SW}}{I_{pk}} (t_{ON})$$

Where V_{SW} is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V max, 0.25V min with $V_{IN} = +15V$ and 1.5V max, 0.5V min with $V_{IN} = +5V$.

Example: A +5V 10% input must be converted to +15V at 15mA. A Schottky diode (1N5817) and a MAX633B are used.

Calculate maximum inductor value allowed:

$$I_{pk} = \frac{15V + 0.4V - 4.5V}{(0.25)(4.5V - 0.75V)} (15mA) = 174mA$$

$$L = \frac{4.5 - 0.75}{174mA} (8\mu s) = 172\mu H$$

Calculate the minimum inductor value allowed:

$$I_{pk} = 450mA \text{ (from table of max ratings)}$$

$$L = \frac{5.5V - 0.25V}{450mA} (12\mu s) = 140\mu H$$

If this minimum value is greater than the maximum value calculated above, an external power MOSFET must be used. See the MAX641/642/643 data sheet.

A value of 160 μH would be a good choice for this application. The "A" grade devices, with tighter oscillator tolerance, allow more output current in a given application.

Inductor Saturation

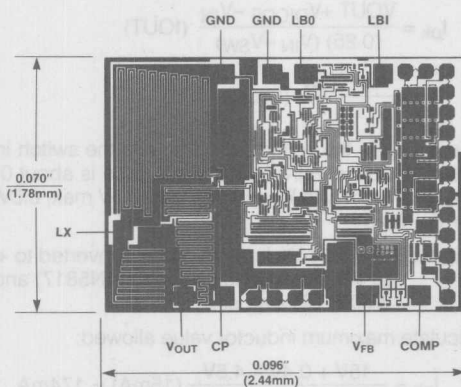
When using off-the-shelf inductors, make sure the peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns or NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor. Inductor saturation leads to very high current levels causing excessive power dissipation, poor efficiency, and possible damage to the chip and the catch diode.

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CMOS Fixed/Adjustable Output Step-Up Switching Regulators

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates. It is this rapid current increase and the resultant high peak currents that can damage the inductor and the catch diode.

Chip Topography



Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE
MAX633XCPA	0°C to +70°C	8 Plastic DIP
MAX633XCSA	0°C to +70°C	8 Narrow SO
MAX633XC/D	0°C to +70°C	Dice
MAX633XEPA	-40°C to +85°C	8 Plastic DIP
MAX633XESA	-40°C to +85°C	8 Narrow SO
MAX633XEJA	-40°C to +85°C	8 CERDIP
MAX633XMJA	-55°C to +125°C	8 CERDIP

* X = A for 5% Output Accuracy. X = B for 10% Accuracy.

Calculate the minimum inductor value allowed:

$$L = \frac{V_{OUT} - V_{IN}}{\Delta I} \times \frac{1}{f_{SW}}$$

where:

- V_{OUT} = 4.5V (from table of max ratings)
- V_{IN} = 2.5V - 0.2V = 2.3V
- ΔI = 450mA (132% = 140% of 450mA)
- f_{SW} = 100kHz

If the minimum value is greater than the maximum value calculated above, an external power MOSFET must be used. See the MAX631/632/633 data sheet.

A value of 100µH would be a good choice for this application. The 'A' grade device, with tighter capacitor tolerance, allow more output current in a given application.

Inductor Saturation

When using off-the-shelf inductors, make sure the peak current rating is observed. When designing your own inductor, observe the core manufacturer's Ampere-turns or Ht ratings. Failure to observe the peak current or Ht ratings may lead to saturation of the inductor. Inductor saturation leads to very high current levels causing excessive power dissipation, poor efficiency, and

Inductor Value—Low Enough?

The problem that plagues designers most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst case is:

- Maximum load current
- Minimum supply voltage
- Maximum inductor value, including tolerance
- Maximum on resistance of the switch, because it reduces the excitation voltage across the inductor
- Worst-case low on time

Inductor Value—High Enough?

The inductor value must also be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. All kinds of odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sink, winding coils, and increased output ripple. Very low inductor values may result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches is a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

- Maximum supply voltage

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

Preset/Adjustable Output CMOS Inverting Switching Regulators

General Description

The MAX635/MAX636/MAX637 inverting switching regulators are designed for minimum component DC-DC conversion in the 5mW to 500mW range.

Low power applications require only a diode, output filter capacitor, and a low-cost inductor. An additional MOSFET and driver are needed for higher power applications. Low battery detection circuitry is included on chip.

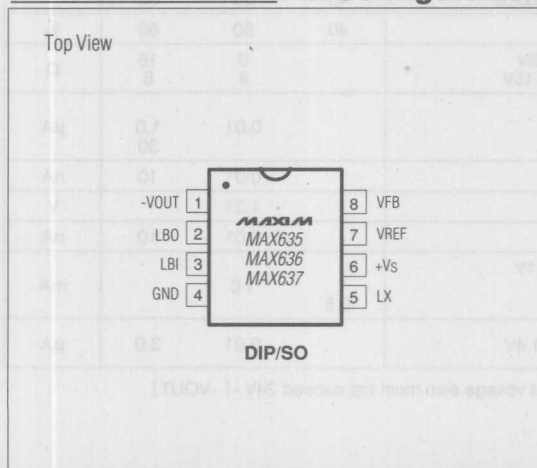
The MAX635/636/637 are preset for -5V, -12V, and -15V outputs, respectively. However, the regulators can be set to other levels by adding 2 resistors.

Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters, with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive.

Applications

Minimum Component, High-Efficiency
DC-DC Converters
Portable Instruments
Battery Power Conversion
Board Level DC-DC Conversion

Pin Configuration



Features

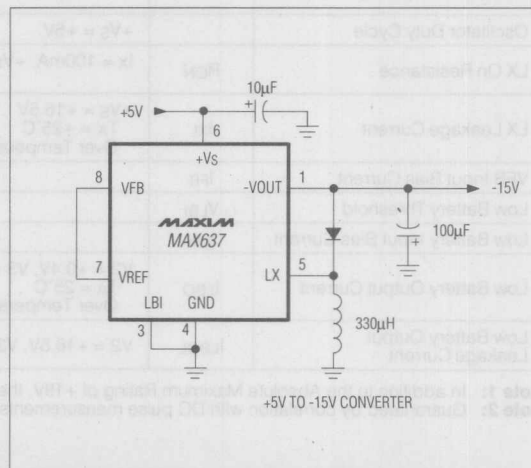
- ◆ Preset -5V, -12V, -15V Output Voltages
- ◆ Adjustable Output with 2 Resistors
- ◆ 85% Typ Efficiency
- ◆ Only 3 External Components
- ◆ 80 μ A Typ Operating Current
- ◆ Low Battery Detector

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX635XCPA	0°C to +70°C	8 Plastic DIP
MAX635XCSA	0°C to +70°C	8 Narrow SO
MAX635XC/D	0°C to +70°C	Dice
MAX635XEPA	-40°C to +85°C	8 Plastic DIP
MAX635XESA	-40°C to +85°C	8 Narrow SO
MAX635XEJA	-40°C to +85°C	8 CERDIP
MAX635XMJA	-55°C to +125°C	8 CERDIP
MAX636XCPA	0°C to +70°C	8 Plastic DIP
MAX636XCSA	0°C to +70°C	8 Narrow SO
MAX636XC/D	0°C to +70°C	Dice
MAX636XEPA	-40°C to +85°C	8 Plastic DIP
MAX636XESA	-40°C to +85°C	8 Narrow SO
MAX636XEJA	-40°C to +85°C	8 CERDIP
MAX636XMJA	-55°C to +125°C	8 CERDIP

*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.
Ordering Information continued on last page.

Typical Operating Circuit



Preset/Adjustable Output CMOS Inverting Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +Vs (Note 1)	+18V
Input Voltage, LBO, LBI, VFB	-0.3V to (+Vs + 0.3V)
LX Output Current	525mA Peak
LBO Output Current	50mA
Power Dissipation	
Plastic DIP (derate 8.33mW/°C above +50°C)	625mW
Small Outline (derate 6mW/°C above +50°C)	450mW
CERDIP (derate 8mW/°C above +50°C)	800mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Temperature Range	
MAX63_C	0°C to +70°C
MAX63_E	-40°C to +85°C
MAX63_M	-55°C to +125°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

ELECTRICAL CHARACTERISTICS

(TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	+Vs	TA = +25°C Over Temperature	2.3 2.6		16.5 16.5	V
Supply Current	Is	No Load, LX Off, Over Temperature +Vs = +5V +Vs = +15V		80 260	150 500	μA
Reference Voltage	VREF	TA = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
VOUT Voltage (Note 2)		No Load, VFB = VREF Over Temperature				V
		MAX635A } 5% Output Accuracy MAX636A } MAX637A }	-4.75 -11.4 -14.25	-5.0 -12.0 -15.0	-5.25 -12.6 -15.75	
		MAX635B } 10% Output Accuracy MAX636B } MAX637B }	-4.5 -10.8 -13.5	-5.0 -12.0 -15.0	-5.5 -13.2 -16.5	
Efficiency				85		%
Line Regulation (Note 2)		+5V < +Vs < +15V		0.5		%VOUT
Load Regulation (Note 2)		POUT = 0mW to 150mW		0.2		%VOUT
Oscillator Frequency	f0	+Vs = +5V MAX63_A MAX63_B	45 40	50 50	56 65	kHz
Oscillator Duty Cycle		+Vs = +5V	40	50	60	%
LX On Resistance	RON	Ix = 100mA, +Vs = +5V = +15V		9 4	16 8	Ω
LX Leakage Current	IXL	+Vs = +16.5V TA = +25°C Over Temperature		0.01	1.0 30	μA
VFB Input Bias Current	IFB			0.01	10	nA
Low Battery Threshold	VLBI			1.31		V
Low Battery Input Bias Current	ILBI			0.01	10	nA
Low Battery Output Current	ILBO	V2 = +0.4V, V3 = +1.1V TA = 25°C Over Temperature	0.5	1.0		mA
Low Battery Output Leakage Current	ILBOL	V2 = +16.5V, V3 = +1.4V		0.01	3.0	μA

Note 1: In addition to the Absolute Maximum Rating of +18V, the input voltage also must not exceed 24V - | -VOUT |.

Note 2: Guaranteed by correlation with DC pulse measurements.

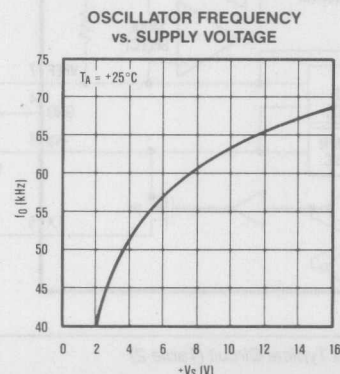
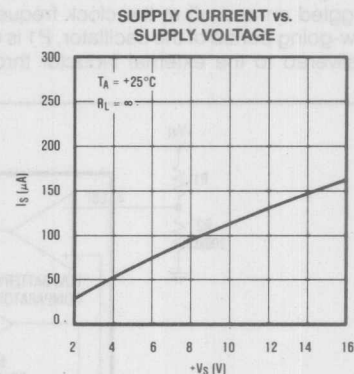
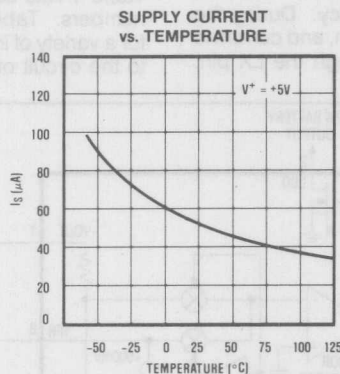
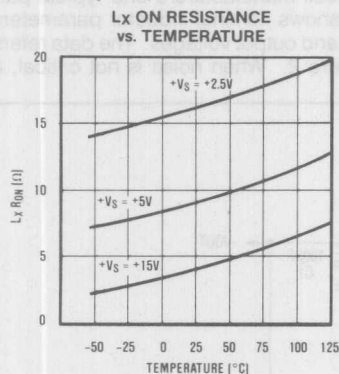
Preset/Adjustable Output CMOS Inverting Switching Regulators

Pin Description

PIN	NAME	FUNCTION
1	-VOUT	The sense INPUT for fixed output operation, -VOUT, is internally connected to the on-chip voltage divider. Although it is connected to the output of the DC-DC converter (Figure 2), VOUT does not supply current, LX does.
2	LBO	Low Battery Detector Output. An open drain N-channel MOSFET which sinks current when the voltage at LBI is below 1.31V.
3	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the low Battery Detector threshold (+1.31V), LBO sinks current.
4	GND	Ground

PIN	NAME	FUNCTION
5	LX	This pin drives the external inductor with an internal P-channel power MOSFET. LX has an output resistance of typically 6Ω and a peak current rating of 525mA.
6	+VS	The positive Supply Voltage, from +2V to +16.5V. The total difference between the negative output voltage and the positive input must be less than 24V.
7	VREF	The Voltage Reference output is +1.31V, generated by an on-chip bandgap reference.
8	VFB	When VFB is tied to VREF, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected to VFB and VREF, this pin becomes the feedback input for adjustable output operation.

Typical Operating Characteristics



Preset/Adjustable Output CMOS Inverting Switching Regulators

Detailed Description

Principle of Operation

Figure 1 shows a simplified inverting converter. When the switch is closed, a charging current flows through the inductor, creating a magnetic field. When the switch opens, the current continues to flow through the inductor in the same direction as the charging current. Since the switch is now open, the current must flow through the diode, thereby charging the capacitor with a negative voltage. As the energy stored in the inductor is transferred to the output filter capacitor, the current linearly decays to zero, and the magnetic field collapses.

The MAX635/636/637 controls the magnitude of the negative output voltage by turning the switch on and off only when the output voltage has become more positive than the desired value.

Basic Circuit Operation

Figure 2 shows the standard circuit for converting a positive voltage into a negative one. When the output becomes more positive than the preset level, the Error Comparator switches low, and the MOSFET at LX is toggled on and off at the clock frequency. During the low-going period of the oscillator, P1 is on, and current is delivered to the external inductor through the LX pin.

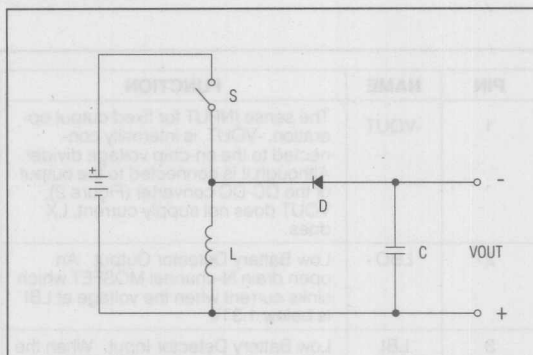


Figure 1. Simplified Inverting Converter

When the oscillator output goes high, the MOSFET turns off, but current continues to flow through the inductor. Diode D1 thus conducts, and the output filter capacitor, C1, is charged negatively.

Basic Step-Down Circuit

Table 1 lists some coil manufacturers and typical part numbers. Table 2 shows nominal inductor parameters for a variety of input and output voltages. The data refers to the circuit of Figure 2. When noise is not critical, a

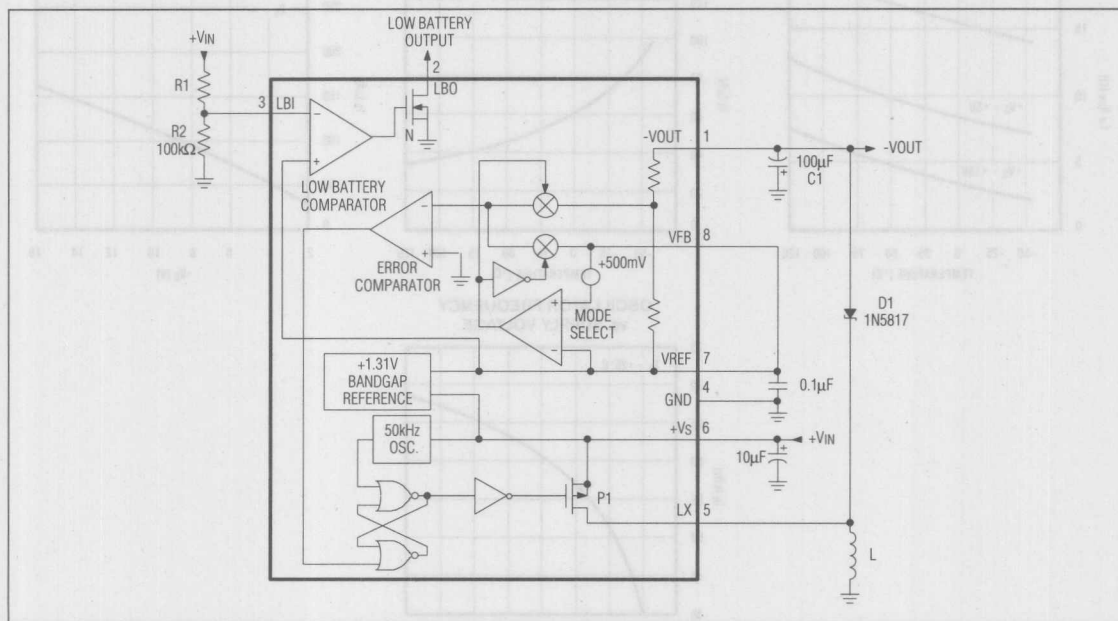


Figure 2. MAX635/636/637 Block Diagram and Typical Circuit (Table 2)

Preset/Adjustable Output CMOS Inverting Switching Regulators

low-cost bobbin inductor will suffice. For higher power circuits, or when low noise and EMI are required, pot cores or toroids should be used. If more output power is desired, see the Medium Power Inverters section.

Table 1. Coil and Core Manufacturers (Note 3)

MANUFACTURER	TYPICAL PART #	DESCRIPTION
ASIA		
TDK Corporation 13-1, Nihonbashi 1-chome Chuo-ku Tokyo 103 Japan		
EUROPE		
Richard Jahre GmbH Luetzowstrasse 90 1000 Berlin 30 Germany		
BOBBIN INDUCTORS		
Dale	IHA-104	500μH, 0.5Ω
Caddell-Burns	7070-29	220μH, 0.55Ω
Gowanda	1B253	250μH, 0.44Ω
TRW	LL-500	500μH, 0.75Ω
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82Ω
TRW	MH-1	600μH, 1.9Ω
Gowanda	050AT1003	100μH, 0.05Ω
FERRITE CORES AND TOROIDS (Note 4)		
Allen Bradley	T0451S100A	Tor. Core, 500nH/T ²
Siemens	B64290-K38-X38	Tor. Core, 4μH/T ²
Magnetics	555.130	Tor. Core, 53nH/T ²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T ²

Note 3: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Note 4: Permag Corp. is a distributor for many of the listed core and toroid manufacturers (516) 822-3311.

Table 2. Inductor Selection for Common Designs (Figure 2)

V _{IN} (V)	V _{OUT} (V)	I _{OUT} (mA)	Part No.	INDUCTOR	
				μH	Ω
+3	-5	5	7070-27	150μH	0.43
+5	-5	25	7070-27	150μH	0.43
+9	-5	40	7070-31	330μH	0.72
+12	-5	45	7070-33	470μH	0.88
+15	-5	50	7070-35	680μH	1.5
+5	-12	12	7070-26	120μH	0.32
+9	-12	30	7070-31	330μH	0.72
+12	-12	40	7070-33	470μH	0.88
+3	-15	2	7070-27	150μH	0.43
+5	-15	8	7070-27	150μH	0.43
+9	-15	25	7070-31	330μH	0.72

Note 5: Caddell-Burns N.Y. (516) 746-2310.

Low Battery Detector

The Low Battery Output, LBO, sinks current whenever the input voltage at Low Battery Input, LBI, is less than +1.31V. LBI is a high impedance CMOS input, with less than 10nA leakage current. LBO is an open drain N-channel MOSFET with about 500Ω of output resistance. The trip voltage of the Low Battery Detector can be adjusted using an external voltage divider as shown in Figure 2. If hysteresis is desired, add a resistor between LBO and LBI.

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R1 = R2 \left(\frac{V_{LB}}{1.31V} - 1 \right)$$

(V_{LB} is the desired Low Battery detection voltage.)

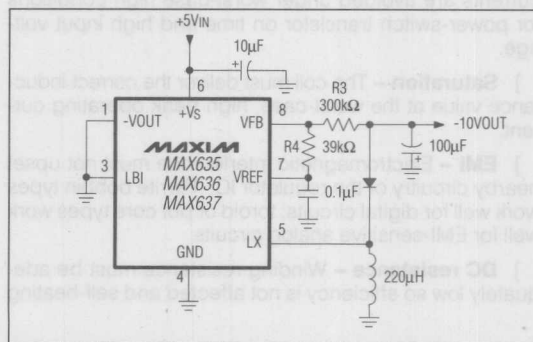


Figure 3. Adjustable Output Operation

Preset/Adjustable Output CMOS Inverting Switching Regulators

Fixed or Adjustable Output

For operation at one of the preset output voltages (-5V for the MAX635, -12V for the MAX636, and -15V for the MAX637), VFB is connected to VREF, and no external resistors are required.

Other output voltages are selected by connecting an external voltage divider to VFB as shown in Figure 3. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$V_{OUT} = -1.31V \times \frac{R3}{R4}$$

External Components

What Value of Inductor?

A General Discussion

The converters in this data sheet operate by charging an inductor from a DC input and then discharging the inductor to generate a DC output that is opposite in polarity to the input.

Inductor selection for any DC-DC converter depends on three things: the desired output power, the input voltage (or input voltage range), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This, along with the input voltage, determines how much energy will be stored in the coil.

The maximum amount of energy (EL) in the coil each cycle is a function of the peak current (Ipk) and the inductance of the coil (L):

The inductor must meet four electrical criteria:

[] **Value** – low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case high conditions for power-switch transistor on time and high input voltage.

[] **Saturation** – The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[] **EMI** – Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for digital circuits; toroid or pot core types work well for EMI-sensitive analog circuits.

[] **DC resistance** – Winding resistance must be adequately low so efficiency is not affected and self-heating

does not occur. Values less than 0.5Ω are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX635/636/637 operating frequency.

Inductor Value – Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst case is:

- [] Maximum load current
- [] Minimum supply voltage
- [] Maximum inductor value, including tolerance
- [] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
- [] Worst-case low on time

Inductor Value – High Enough?

The inductor value must also be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. Odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values can result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

- [] Maximum supply voltage
- [] Minimum inductor value, including tolerance
- [] Minimum on resistance of the switch
- [] Low switching frequency (or maximum switch on time)

Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for lowest ripple.

$$[1] \quad I_{pk} = \frac{V_{OUT} + V_{DIODE}}{(0.25)(V_{IN} - V_{SW})} (I_{OUT})$$

$$[2] \quad L = \frac{V_{IN} - V_{SW}}{I_{pk}} (t_{ON})$$

where VSW is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V

Preset/Adjustable Output CMOS Inverting Switching Regulators

MAX635/636/637

max, 0.25V min with $V_{IN} = +15V$ and 1.5V max, 0.5V min with $V_{IN} = +5V$.

Example: A +5V 10% input must be converted to -12V at 12mA.
A Schottky diode (1N5817) and a MAX636A are used.

Calculate the maximum inductor value allowed:

$$I_{pk} = \frac{12V - 0.4V}{(0.25)(4.5V - 1.5V)} (12mA) = 198mA$$

$$L = \frac{4.5V - 1.5V}{198mA} (9\mu s) = 136\mu H$$

Calculate the minimum inductor value allowed:

$I_{pk} = 525mA$ (from table of max ratings; use the power MOSFET max ratings for external transistor circuits.)

$$L = \frac{5.5V - 0.5V}{525mA} (11\mu s) = 105\mu H$$

A value of 120 μH would be a good choice for this application.

I_{pk} must also be compared to the current rating of the LX switch. If I_{pk} exceeds the peak current rating of the switch (525mA), an external MOSFET or transistor with an adequate current rating must be used (see Medium Power Inverters).

The coil resistance has a significant effect on the output current; a coil with a low resistance will increase the output current and overall efficiency. The inductor

should have a powdered iron or ferrite core and should have a resistance less than 0.5 Ω .

Medium Power Inverters

In the circuit of Figure 4, the MAX626 MOSFET driver is used to convert the open drain LX output to a signal suitable for driving the gate of an external P-Channel MOSFET. The IRF9541 has a gate threshold voltage of 2V to 4V so it will have a relatively high resistance if driven with only 5V of gate drive. To increase the gate drive voltage, and thereby increase efficiency, the negative supply pin of the CMOS inverter is connected to the negative output rather than to the ground. Once the circuit is started, the gate drive swings from +5V to -VOUT.

At start-up, the voltage at -VOUT is one Schottky diode drop above ground, and the gate drive to the power MOSFET is slightly less than 5V. The output should be only lightly loaded to ensure start-up, since the output power capability of the circuit is very low until -VOUT is a couple of volts negative. (See Table 3 for component values for L2 and IC1.)

Table 3. Component Selector for Medium Power Inverters (Figure 4)

V_{IN}	-VOUT	IOUT	EFFICIENCY	IC1	L1
5V	-5V	400mA	70%	MAX635	27 μH
5V	-5V	500mA	64%	MAX635	18 μH
5V	-12V	150mA	75%	MAX636	27 μH
5V	-12V	200mA	70%	MAX636	18 μH

Notes: 18 μH Coil = Caddell-Burn's (Mineola, NY) Model 6860-04.
27 μH Coil = Caddell-Burn's Model 6860-06.

External Diode

In most DC-DC converter circuits, the current in the "catch" diode (Figure 2, D1) abruptly goes from zero to its peak value each time the MOSFET at LX switches off. To avoid excessive losses, the diode must have a fast turn-on time. For low power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well. For higher current circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Output Filter Capacitor

The MAX635/636/637's output ripple has 2 components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent

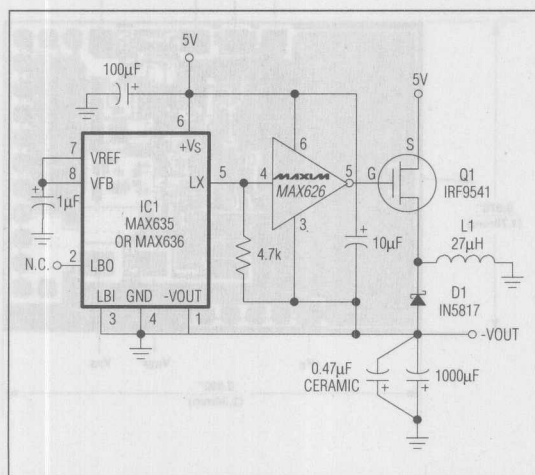


Figure 4. Medium Power Inverter

Preset/Adjustable Output CMOS Inverting Switching Regulators

Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved with a high quality aluminum electrolytic, in the 100 μ F to 500 μ F range, in parallel with a 0.1 μ F ceramic capacitor.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that their peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns on NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external boosting transistors. Inductor saturation leads to very high current levels through the power switching device causing excessive power dissipation, poor efficiency, and possible damage.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

Ordering Information (continued)

PART*	TEMP. RANGE	PIN - PACKAGE
MAX637XCPA	0°C to +70°C	8 Plastic DIP
MAX637XCSA	0°C to +70°C	8 Narrow SO
MAX637XCJA	0°C to +70°C	8 CERDIP
MAX637XC/D	0°C to +70°C	Dice
MAX637XEPA	-40°C to +85°C	8 Plastic DIP
MAX637XESA	-40°C to +85°C	8 Narrow SO
MAX637XEJA	-40°C to +85°C	8 CERDIP
MAX637XMJA	-55°C to +125°C	8 CERDIP

*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.

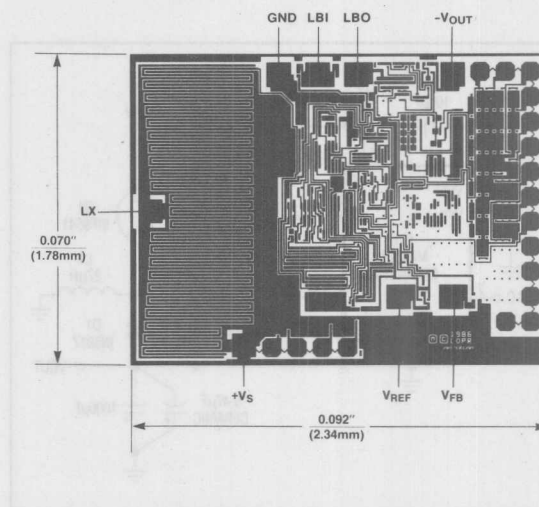
Bypassing and Compensation

The high current pulses in the LX output and the external inductor can cause erratic operation unless the MAX635/636/637 is properly bypassed. Connect a 10mF bypass capacitor directly across the device between +VS and GND to minimize the inductance and high frequency impedance of the power source. Also make sure that the high current ground return path of the inductor does not cause a voltage drop in the regulator's ground line.

The reference voltage output, VREF, should be bypassed to ground with a 0.1 μ F capacitor. Avoid coupling to the high current path that includes the LX output and the inductor ground return.

When the value of the voltage setting resistors (R3 and R4, Figure 3) exceed 50k Ω , stray capacitance at the VFB input can add a "lag" to the feedback response causing output pulses to occur in bursts. This increases low-frequency ripple and lowers efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the VFB node. Normal operation with evenly distributed output pulses can be restored by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

+5V/Adjustable CMOS Step-Down Switching Regulator

MAX638

General Description

The MAX638 step-down switching regulator is designed for minimum component, low power, DC-DC conversion.

Typical applications require only a small, low-cost inductor, an output filter capacitor, and a catch diode. Low battery detection circuitry is included on chip.

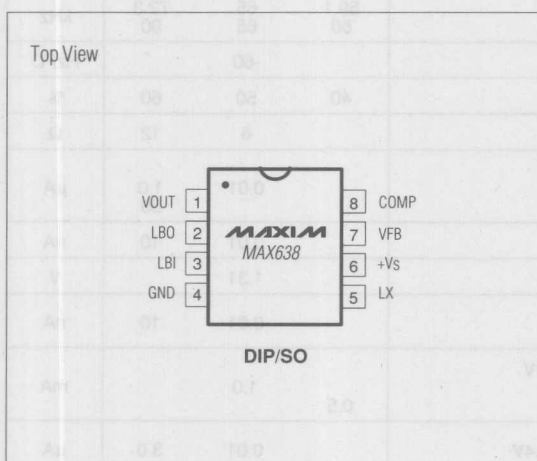
Though most simply used as a fixed +5V output regulator, the MAX638 can be set for other voltages by adding 2 resistors.

Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters, with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive.

Applications

Efficient DC-DC Step-Down Regulation
Linear Voltage Regulator Replacement
+12V to +5V Conversion
Battery Life Extension
Portable Instruments

Pin Configuration



Features

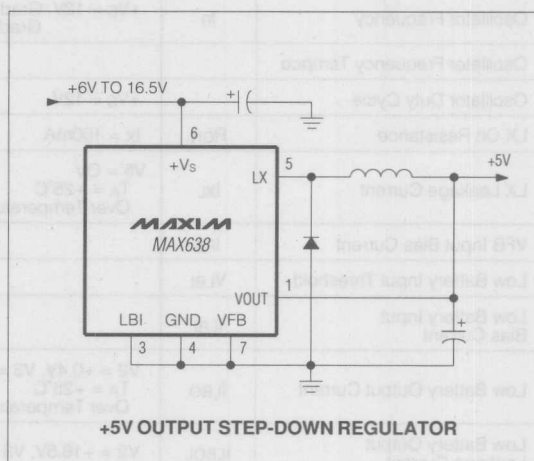
- ◆ Fixed +5V Output
- ◆ Adjustable Output with 2 Resistors
- ◆ Low Operating Current
- ◆ 85% Typ Efficiency
- ◆ 8-Pin Plastic DIP and Narrow SO Packages
- ◆ 3 External Components
- ◆ Low Battery Detector

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX638XCPA	0°C to +70°C	8 Plastic DIP
MAX638XCSA	0°C to +70°C	8 Narrow SO
MAX638XC/D	0°C to +70°C	Dice
MAX638XEPA	-40°C to +85°C	8 Plastic DIP
MAX638XESA	-40°C to +85°C	8 Narrow SO
MAX638XEJA	-40°C to +85°C	8 Cerdip
MAX638XMJA	-55°C to +125°C	8 Cerdip

*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.

Typical Operating Circuit



5

MAXIM

Maxim Integrated Products 5-17

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Dual Mode is a trademark of Maxim Integrated Products.

+5V/Adjustable CMOS Step-Down Switching Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +Vs	+18V
Output Voltage, LX and LBO	+18V
Input Voltage, LBO, LBI, VFB, COMP	-0.3V to (+Vs + 0.3V)
LX Output Current	525mA Peak
LBO Output Current	50mA
Power Dissipation	
Plastic DIP (derate 8.33mW/°C above +50°C)	625mW
Small Outline (derate 6mW/°C above +50°C)	450mW
CERDIP (derate 8mW/°C above +50°C)	800mW

Operating Temperature

MAX638C	-0°C to +70°C
MAX638E	-40°C to +85°C
MAX638M	-55°C to +125°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(+Vs = +12V, TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	+Vs	Over Temperature VOUT = +5V Adjustable mode	5 2.6		16.5 16.5	V
Supply Current	IS	TA = +25°C Over Temperature		135 180	600	μA
Reference Voltage (Internal)		TA = +25°C Over Temperature	1.28 1.24	1.31	1.34 1.38	V
VOUT Voltage (Note 1)		No Load, VFB = GND, Over Temperature	4.75 4.5	5.0 5.0	5.25 5.5	V
Efficiency				85		%
Line Regulation (Note 1)		+10V < +Vs < +15V		0.2		% VOUT
Load Regulation (Note 1)		POUT = 0mW to 150mW		0.2		% VOUT
Oscillator Frequency	f0	+Vs = 12V, Grade A Grade B	59.1 50	65 65	72.3 90	kHz
Oscillator Frequency Tempco				-60		Hz/°C
Oscillator Duty Cycle		+Vs = 12V	40	50	60	%
LX On Resistance	RON	IX = 100mA		6	12	Ω
LX Leakage Current	IXL	V5 = OV TA = +25°C Over Temperature		0.01	1.0 30	μA
VFB Input Bias Current	IFB			0.01	10	nA
Low Battery Input Threshold	VLBI			1.31		V
Low Battery Input Bias Current	ILBI			0.01	10	nA
Low Battery Output Current	ILBO	V2 = +0.4V, V3 = +1.1V TA = +25°C Over Temperature	0.5	1.0		mA
Low Battery Output Leakage Current	ILBOL	V2 = +16.5V, V3 = +1.4V		0.01	3.0	μA

Note 1: Guaranteed by correlation with DC pulse measurements.

+5V/Adjustable CMOS Step-Down Switching Regulator

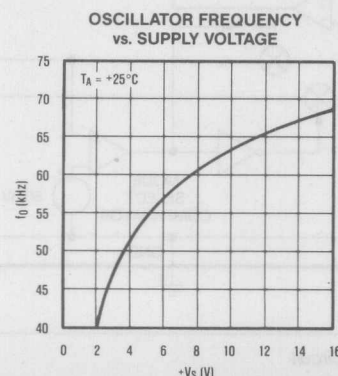
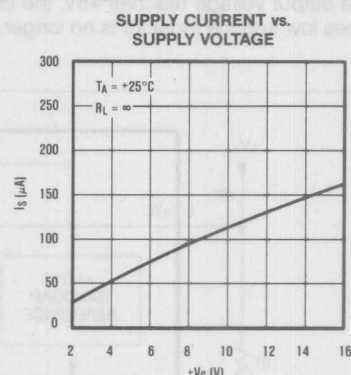
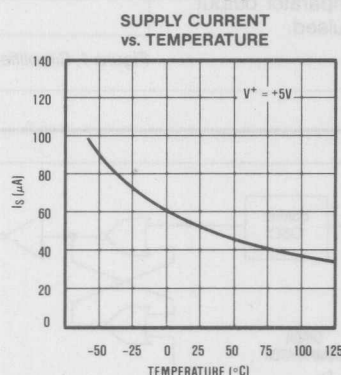
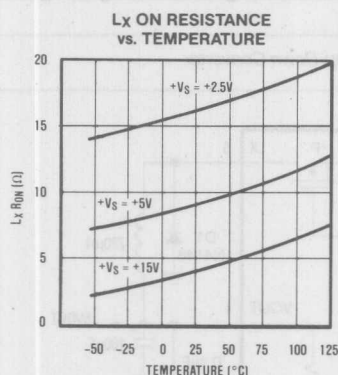
MAX638

Pin Description

PIN	NAME	FUNCTION
1	VOUT	The sense INPUT for fixed +5V output operation, VOUT, is internally connected to the on-chip voltage divider. Although it is connected to the output of the DC-DC converter (Figure 2), the VOUT pin does not supply current, LX does.
2	LBO	Low Battery Detector Output. An open drain N-channel MOSFET which sinks current when the voltage at LBI is below +1.31V.
3	LBI	Low Battery Detector Input. When the voltage at LBI is lower than the Low Battery Detector threshold (+1.31V), LBO sinks current.
4	GND	Ground

PIN	NAME	FUNCTION
5	LX	This pin drives the external inductor with an internal P-channel power MOSFET. LX has an output resistance of typically 6Ω and a peak current rating of 525mA.
6	+Vs	The input voltage, from VOUT to +16.5V.
7	VFB	When VFB is grounded, the DC-DC converter output will be +5V. When an external voltage divider is connected from VOUT to VFB, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. It is normally left unconnected. In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between VOUT and COMP reduces low-frequency ripple and improves transient response.

Typical Operating Characteristics



+5V/Adjustable CMOS Step-Down Switching Regulator

Detailed Description

Basic Operation

Figure 1 shows a simplified step-down DC-DC converter. When the switch closes, a charging current flows through the inductor creating a magnetic field. (This current flows into the filter capacitor and load as well.) When the switch opens, the current continues to flow through the inductor in the same direction as the charging current. But since the switch is now open, the current must flow through the diode. With the switch open, the inductor alone supplies current to the load. This current linearly decays to zero as the magnetic field collapses and the energy in the core of the inductor is transferred to the filter capacitor and load.

Figure 2 shows a block diagram of the MAX638 and a typical connection in which a +9V input is converted to a +5V output with 85% efficiency. When the output drops below +5V, the Error Comparator switches high and connects the internal 65kHz oscillator to the gate of the LX output driver. LX turns on and off at the clock frequency, charging and discharging the inductor and supplying current to the output as described above. When the output voltage reaches +5V, the comparator output goes low and the inductor is no longer pulsed.

Basic Step-Down Circuits

Table 1 shows nominal inductor parameters for a variety of input voltages. The data refers to the circuit of Figure 3.

Output Driver (LX Pin)

A large P-channel MOSFET with an on resistance of approximately 6Ω is used to charge the inductor. It is internally connected between $+V_S$ and LX and has a peak current rating of 525mA. The available output current for most applications will be less than the peak current rating. A good rule of thumb for MAX638 maximum output current is:

$$4 I_{OUT} < 525\text{mA}, \text{ assuming } V_{IN} \approx 2\text{VOUT}$$

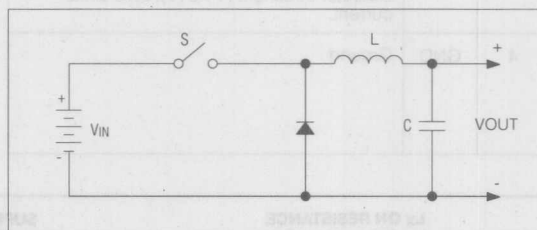


Figure 1. Simplified Step-Down Converter

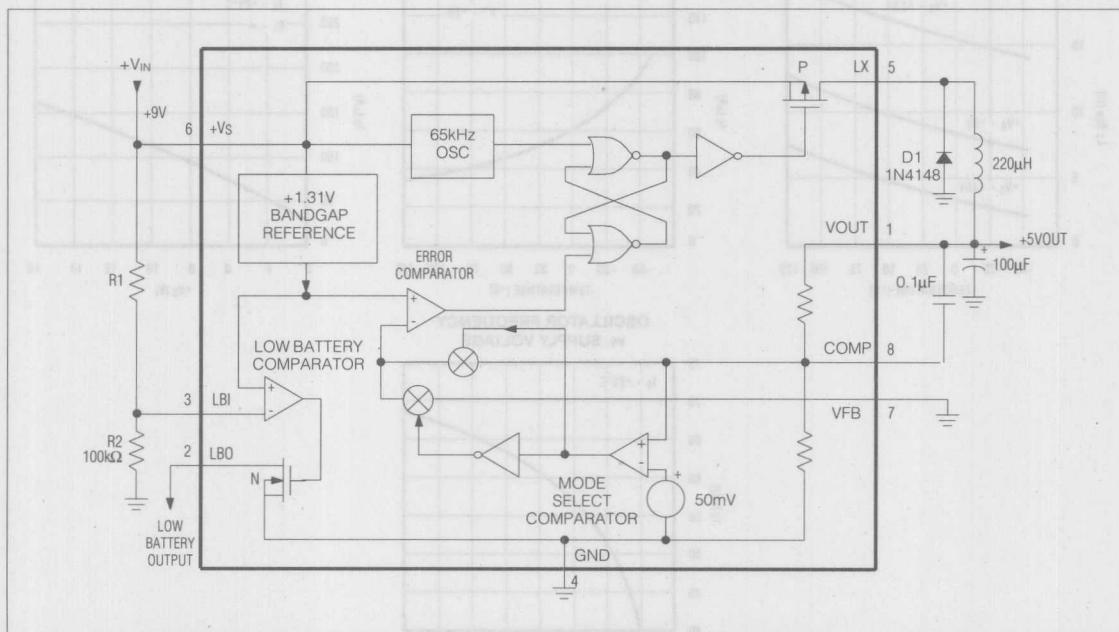


Figure 2. MAX638 Block Diagram and Typical Circuit

+5V/Adjustable CMOS Step-Down Switching Regulator

MAX638

Table 1. Inductor Selection For Common Designs (See Figure 3)

MAXIM PART NO.	V _{IN} (V)	V _{OUT} (V)	I _{OUT} (mA)	TYP EFF (%)	I _{pk} (mA)	PART NO.*	INDUCTOR (L) μH	Ω
MAX638	7-9.5	5	35	92	200	7070-27	150	0.4
	8-9.5	5	55	89	200	7070-27	150	0.4
	10-14	5	50	92	300	7070-30	270	0.6
	12	5	60	92	250	7070-30	270	0.6
	12	5	75	89	300	7070-28	180	0.5

* Caddell-Burns, NY, (516) 746-2310

Fixed or Adjustable Output

For operation at the preset +5V output voltage, VFB is connected to GND, and no external resistors are required. For other output voltages, an external voltage divider is connected to VFB as shown in Figure 4. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R3 = R4 \left(\frac{V_{OUT}}{1.31V} - 1 \right)$$

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input (LBI) with the internal +1.31V bandgap reference. The Low Battery Detector Output (LBO) goes low whenever the input voltage at LBI is less than +1.31V. The Low Battery detection voltage is set by resistors, R1 and R2 (Figure 2).

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R1 = R2 \left(\frac{V_{LB}}{1.31V} - 1 \right) \quad (V_{LB} \text{ is the desired Low Battery detection voltage})$$

What Value of Inductor?

A General Discussion

The converter in this data sheet operates by charging an inductor from a DC input, and then discharging the inductor to generate a DC output less than the input.

The proper inductor for any DC-DC converter depends on three things: the desired output power, the input voltage (or input voltage range), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This and the input voltage determines how much energy will be stored in the coil.

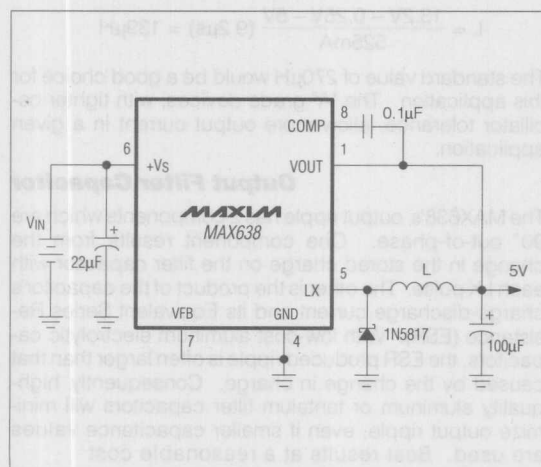


Figure 3. Typical Operating Circuit (Table 1)

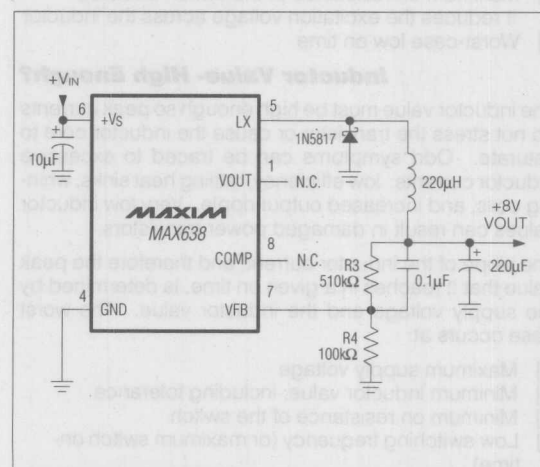


Figure 4. Adjustable Output Operation

+5V/Adjustable CMOS Step-Down Switching Regulator

The inductor must meet four electrical criteria:

[] **Value-** Low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case high conditions for power-switch transistor on time and high input voltage.

[] **Saturation-** The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[] **EMI-** Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for most digital circuits; toroids or pot cores work well for EMI-sensitive analog circuits.

[] **DC resistance-** Winding resistance must be adequately low so efficiency is not affected and self-heating does not occur. Values less than 2Ω are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX638 operating frequency.

Inductor Value- Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst case is:

- [] Maximum load current
- [] Minimum supply voltage
- [] Maximum inductor value, including tolerance
- [] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
- [] Worst-case low on time

Inductor Value- High Enough?

The inductor value must be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. Odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values can result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

- [] Maximum supply voltage
- [] Minimum inductor value, including tolerance
- [] Minimum on resistance of the switch
- [] Low switching frequency (or maximum switch on-time)

Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for low ripple.

$$[1] \quad I_{pk} = \frac{4 I_{OUT}}{\frac{V_{IN} - V_{SW} - V_{OUT}}{V_{OUT} - V_{DIODE}} + 1}$$

$$[2] \quad L = \frac{V_{IN} - V_{SW} - V_{OUT}}{I_{pk}} (t_{ON})$$

where V_{SW} is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V max, 0.25V min with $V_{IN} = +15V$ and 1.5V max, 0.5V min with $V_{IN} = +5V$.

Example: A +12V 10% input must be converted to +5V at 50mA. A Schottky diode (1N5817) and a MAX638B are used.

Calculate the maximum inductor value allowed:

$$I_{pk} = \frac{(4) (50mA)}{\frac{10.8V - 0.75V - 5V}{5V - 0.4V} + 1} = 95mA$$

$$L = \frac{10.8V - 0.75V - 5V}{95mA} (6\mu s) = 319\mu H$$

Calculate the minimum inductor value allowed:

$$I_{pk} = 525mA \text{ (from table of max ratings)}$$

$$L = \frac{13.2V - 0.25V - 5V}{525mA} (9.2\mu s) = 139\mu H$$

The standard value of 270 μ H would be a good choice for this application. The "A" grade devices, with tighter oscillator tolerance, allow more output current in a given application.

Output Filter Capacitor

The MAX638's output ripple has 2 components which are 90° out-of-phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high-quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at a reasonable cost

+5V/Adjustable CMOS Step-Down Switching Regulator

are typically achieved with a high-quality aluminum electrolytic, in the 100 μ F to 500 μ F range, in parallel with a 0.1 μ F ceramic capacitor.

**Table 2. Coil and Core Manufacturers
(Note 2)**

MANUFACTURER	TYPICAL PART #	DESCRIPTION
ASIA		
TDK Corporation 13-1, Nihonbashi 1-chome Chuo-ku Tokyo 103 Japan		
EUROPE		
Richard Jahre GmbH Luetzowstrasse 90 1000 Berlin 30 Germany		
BOBBIN INDUCTORS		
Dale	IHA-104	500 μ H, 0.5 Ω
Caddell-Burns	7070-29	220 μ H, 0.55 Ω
Gowanda	1B253	250 μ H, 0.44 Ω
UTC	LL-500	500 μ H, 0.75 Ω
POTTED TOROIDAL INDUCTORS		
Dale	TE-3Q4TA	1mH, 0.82 Ω
UTC	MH-1	600 μ H, 1.9 Ω
Gowanda	050AT1003	100 μ H, 0.05 Ω
FERRITE CORES AND TOROIDS (Note 3)		
Siemens	B64290-K38-X38	Tor. Core, 4 μ H/T ²
Magnetics	555.130	Tor. Core, 53nH/T ²
Stackpole	57-3215	Pot Core, 14mm x 8mm
Magnetics	G-41408-25	Pot Core, 14 x 8, 250nH/T ²

Note 2: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufactures of these components.

Note 3: Permag Corp. is a distributor for many of the listed core and toroid manufacturers (516) 822-3311.

External Diode

In most MAX638 circuits, the current in the external diode (D1, Figure 2) abruptly goes from zero to its peak value each time LX switches off. To avoid excessive losses, the diode must have a fast turn-on time. For low-power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well. For higher power circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended.

Although 1N4001s and other general purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that their peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns or NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external boost transistors. Inductor saturation leads to very high current levels through the power switching device causing excessive power dissipation, poor efficiency, and possible damage.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

Bypassing and Compensation

Since the inductor charge and discharge currents can be relatively large, high currents may flow in ground connections near the MAX638. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and power-supply bypassing should be used. A 10 μ F aluminum electrolytic placed at the device pins is recommended.

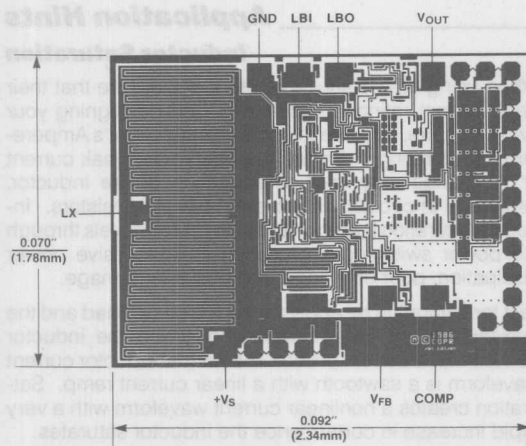
When the value of the voltage setting resistors (R3 and R4, Figure 4) exceed 50k Ω , stray capacitance at the VFB input can add a "lag" to the feedback response, increasing low-frequency ripple and lowering efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the VFB node. It can also be remedied by adding a "lead" compensation capacitor (100pF to 0.1 μ F) in parallel with R3.

MAX638

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+5V/Adjustable CMOS Step-Down Switching Regulator

Chip Topography



Since the inductor charge and discharge currents can be relatively large, high currents may flow in ground connections near the MAX638. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and power-supply bypassing should be used. A 10 μ F aluminum electrolytic placed at the device pins is recommended.

When the value of the voltage setting resistor (R_3) and R_4 (Figure 4) exceed 50k Ω , stray capacitance at the VFB input can add a lag to the feedback response, increasing low-frequency ripple and lowering efficiency. This problem can often be avoided by minimizing lead lengths and output board trace size at the VFB node. It can also be remedied by adding a lead compensation capacitor (100pF to 0.1 μ F) in parallel with R_3 .

are typically achieved with a high-quality aluminum electrolytic capacitor in the 100 μ F to 500 μ F range. In parallel with a 0.1 μ F ceramic capacitor.

Table 2. Coil and Core Manufacturers (Note 3)

MANUFACTURER	TYPICAL PART #	DESCRIPTION
ASIA		
TOK Corporation		12-1, 1000000-1, 1000000-2
Chuoichi		1000000-1, 1000000-2
Europe		
Robert Schenck		1000000-1, 1000000-2
1000000-1, 1000000-2		
ROBIN INDUSTRIES		
DAI	HA-101	5000H, 0.500
Coastal Group	1000-25	5000H, 0.500
Gowanda	1000-25	5000H, 0.500
UTC	LI-100	5000H, 0.500
POTTED TOROIDAL INDUCTORS		
DAI	TS-3001A	1000H, 0.500
UTC	MH-1	1000H, 0.500
Gowanda	5000H-100	1000H, 0.500
PERMITE CORES AND TOROIDS (Note 3)		
Shimada	BR-200-K-100	1000H, 0.500
Magnetics	400-100	1000H, 0.500
Shimada	BR-200-K-100	1000H, 0.500
Magnetics	400-100	1000H, 0.500

Note 3: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of manufacturers or device components.

Note 3: Maxim Corp. is a distributor for many of the listed coil and toroid manufacturers (800-552-2211).

External Diode

In most MAX638 circuits, the diode in the external diode (Figure 5) should drop from zero to its peak value each time the switcher off. To avoid excessive power, the diode must have a fast turn-on time. For low-power circuits with peak currents less than 100mA, signal diodes such as 1N4148s perform well. For higher power circuits, the minimum efficiency at low power, the

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MAXIM

Fixed Output 10W CMOS Step-Up Switching Regulators

MAX641/642/643

General Description

The MAX641/MAX642/MAX643 step-up switching regulators are designed for minimum component DC-DC converter circuits in the 5mW to 10W range.

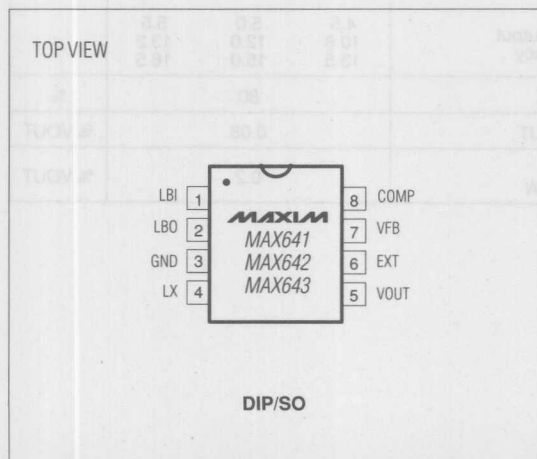
Low-power applications require only an output filter capacitor and a small, low-cost inductor. An additional MOSFET or bipolar transistor is needed for high-power applications. Low battery detection circuitry is included on chip.

The MAX641/642/643 are preset for +5V, +12V, and +15V outputs, respectively. However, the regulators can be set to other levels by adding 2 resistors. Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive. See Table 3 for a summary of other DC-DC converter products.

Applications

Simple, High-Efficiency DC-DC Converters
Uninterruptible Board-Level Power Supplies
Power Conditioning for Battery Systems
Portable Instruments and Communications

Pin Configuration



Features

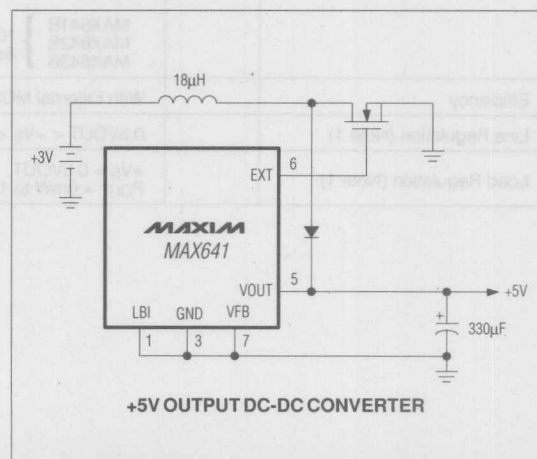
- ◆ Fixed +5V, +12V, +15V Output Voltages
- ◆ Adjustable Output with 2 Resistors
- ◆ On-Chip Driver for High-Power External MOSFET
- ◆ 135 μ A Typ Operating Current
- ◆ 80% Typ Efficiency
- ◆ 8-Pin Narrow DIP and Narrow SO Packages

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX641XCPA	0°C to +70°C	8 Plastic DIP
MAX641XCSA	0°C to +70°C	8 Narrow SO
MAX641XC/D	0°C to +70°C	Dice
MAX641XEPA	-40°C to +85°C	8 Plastic DIP
MAX641XESA	-40°C to +85°C	8 Narrow SO
MAX641XEJA	-40°C to +85°C	8 CERDIP
MAX641XMJA	-55°C to +125°C	8 CERDIP
MAX642XCPA	0° to +70°C	8 Plastic DIP
MAX642XCSA	0° to +70°C	8 Narrow SO
MAX642XC/D	0° to +70°C	Dice
MAX642XEPA	-40°C to +85°C	8 Plastic DIP
MAX642XESA	-40°C to +85°C	8 Narrow SO
MAX642XEJA	-40°C to +85°C	8 CERDIP
MAX642XMJA	-55°C to +125°C	8 CERDIP

*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.
Ordering information continued on last page.

Typical Operating Circuit



MAXIM

Maxim Integrated Products 5-25

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Dual Mode is a trademark of Maxim Integrated Products

Fixed Output 10W CMOS Step-up Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VOUT	+18V
Output Voltage, LX and LBO	+18V
Input Voltage, LBI, LBO, VFB, COMP. . . -0.3V to (+VOUT + 0.3V)	
LX Output Current	450mA Peak
LBO Output Current	50mA
Power Dissipation	
Plastic DIP (derate 8.33mW/°C above +50°C)	625mW
Small Outline (derate 6mW/°C above +50°C)	450mW
CERDIP (derate 8mW/°C above +50°C)	800mW

Operating Temperature

MAX64__C	0°C to +70°C
MAX64__E	-40°C to 85°C
MAX64__M	-55°C to 125°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	+Vs	Voltage at VOUT Over Temperature	2.0		16.5	V
Start-up Voltage	+Vs	Voltage at VOUT TA = +25°C Over Temperature	1.5 1.8	1.3		V
Supply Current	IS	LX Off, Over Temperature VOUT = +5V VOUT = +12V VOUT = +15V		0.135 0.5 0.75	0.4 2.0 2.5	mA
Reference Voltage (Internal)	VREF	TA = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
VOUT Voltage (Note 1)		No Load, VFB = GND, Over Temperature				
		MAX641A } 5% Output MAX642A } Accuracy MAX643A }	4.75 11.4 14.25	5.0 12.0 15.0	5.25 12.6 15.75	V
		MAX641B } 10% Output MAX642B } Accuracy MAX643B }	4.5 10.8 13.5	5.0 12.0 15.0	5.5 13.2 16.5	
Efficiency		With External MOSFET		80		%
Line Regulation (Note 1)		0.5VOUT < +Vs < VOUT		0.08		% VOUT
Load Regulation (Note 1)		+Vs = 0.5VOUT, POUT = 0mW to 150mW		0.2		% VOUT

Fixed Output 10W CMOS Step-Up Switching Regulators

MAX641/642/643

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Frequency	f _o	VOUT = +5V MAX641A MAX641B	40 37.5	45 45	50 56.5	kHz
		VOUT = +12V MAX642A MAX642B	45.5 42	50 50	56 62.5	
		VOUT = +15V MAX643A MAX643B	45.5 42	50 50	56 62.5	
Oscillator Frequency Tempco				-60		Hz/°C
Oscillator Duty Cycle		MAX641, VOUT = +5V MAX642, VOUT = +12V MAX643, VOUT = +15V	40 40 40	50 50 50	60 60 60	%
EXT Output Resistance		VOUT = +5V, IOUT = ±10mA VOUT = +15V, IOUT = ±30mA		140 90		Ω
EXT Switching Time	t _{ON} , t _{OFF}	C _L = 330pF VOUT = +5V VOUT = +15V		160 125		ns
LX On Resistance	R _{ON}	I _X = 100mA, VOUT = +5V VOUT = +15V		6 3.5	12 7	Ω
LX Leakage Current	I _{XL}	V4 = +16.5V T _A = +25°C Over Temperature (C,E) Over Temperature (M)		0.01	1.0 30 100	μA
Diode Forward Voltage	V _F	I _F = 100mA			1.0	V
VFB Input Bias Current	I _{FB}			0.01	10	nA
Low Battery Threshold	V _{LBI}			1.31		V
Low Battery Input Bias Current	I _{LBI}			0.01	10	nA
Low Battery Output Current	I _{LBO}	V2 = +0.4V, V1 = +1.1V T _A = +25°C Over Temperature	0.5	1.0		mA
Low Battery Output Leakage Current	I _{LBOL}	V2 = +16.5V, V1 = +1.4V		0.01	3.0	μA

Note 1: Guaranteed by correlation with DC pulse measurements.

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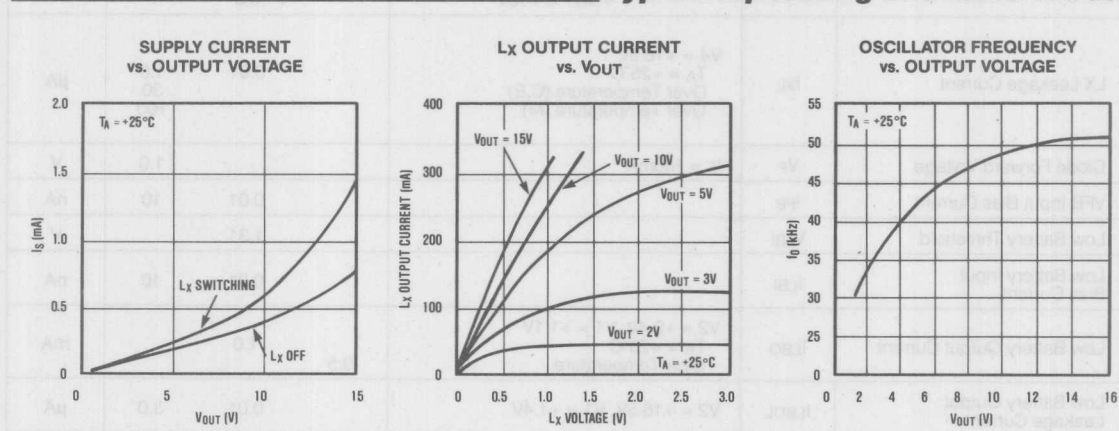
Fixed Output 10W CMOS Step-up Switching Regulators

Pin Description

PIN	NAME	FUNCTION
1	LBI	Low Battery Input. When the voltage at LBI is lower than the Low Battery Detector threshold (+1.31V), LBO sinks current.
2	LBO	The Low Battery Detector Output is an open drain N-channel MOSFET which sinks current when the LBI is below +1.31V.
3	GND	Ground
4	LX	In low-power applications, LX drives the external inductor with an internal N-channel power MOSFET. LX has a typical output resistance of 6Ω and a peak current rating of 450mA.
5	VOUT	The regulated DC-DC converter output when the internal MOSFET and catch diode are used. When an external diode is used, this pin becomes the supply voltage input pin and is usually connected to the cathode of the external diode.

PIN	NAME	FUNCTION
6	EXT	The drive output for an external power MOSFET or bipolar transistor. EXT swings from GND to VOUT and has approximately 100Ω sink/source impedance. EXT is low when LX is open circuit and high when LX is on.
7	VFB	When VFB is grounded, the DC-DC converter output will be the factory preset value. When an external voltage divider is connected to VFB, this pin becomes the feedback input for adjustable output operation.
8	COMP	The Compensation input is connected to the internal voltage divider which sets the fixed voltage output. In some circuit board layouts, a lead compensation capacitor (100pF to 10nF) connected between VOUT and COMP reduces low-frequency ripple and improves transient response. Ground comp when using an External Voltage divider on VFB.

Typical Operating Characteristics



MAX641/642/643

Basic Operation

When EXT is high, the MOSFET switches on, and the inductor current increases linearly storing energy in the coil. When EXT switches the MOSFET off, the coil's magnetic field collapses, and the voltage across the inductor reverses sign. The voltage at the anode of the catch diode then rises until the diode is forward biased, delivering power to the output. As the output voltage reaches the desired level, the Error Comparator inhibits EXT until the load discharges the output filter capacitor to less than the desired output level.

V_{IN} , Bootstrapped Operation

V_{IN} Greater Than V_{OUT}

If the regulator's input voltage is more than 1 forward diode drop greater than the desired output voltage, the EXT and LX outputs will not turn on, and the output will no longer be regulated. However, current will be supplied to the load directly through the catch diode. As long as the input is more than 0.6V above the desired output,



Figure 1. +3V to +5V Converter and Block Diagram for MAX641/642/643

Fixed Output 10W CMOS Step-up Switching Regulators

the output will equal the input voltage, less the forward drop of the catch diode.

Fixed or Adjustable Output

For operation at one of the preset output voltages (+5V for the MAX641, +12V for MAX642, and +15V for MAX643), VFB is connected to GND, and no external resistors are required.

For other output voltages, a voltage divider is connected to VFB as shown in Figure 2. The output is set by R3 and R4 as follows:

Let R4 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ, then:

$$R3 = R4 \left(\frac{V_{OUT}}{1.31} - 1 \right)$$

Low Battery Detector

The Low Battery Detector compares the voltage on the Low Battery Input (LBI), with the internal +1.31V bandgap reference. The Low Battery Detector Output (LBO) goes low whenever the input voltage at LBI is less than +1.31V. The Low Battery threshold is set by resistors R1 and R2 (Figure 1).

Let R2 be any resistance in the 10kΩ to 10MΩ range, typically 100kΩ.

$$R1 = R2 \left(\frac{V_{LB}}{1.31V} - 1 \right) \quad (V_{LB} \text{ is the desired Low Battery detection voltage})$$

What Value Of Inductor?

A General Discussion

The converters in this data sheet operate by charging an inductor from a DC input, then discharging the inductor to generate a DC output greater than the input.

The proper inductor for any DC-DC converter depends on three things: the desired output power, the input voltage (or range of input voltage), and the converter's oscillator frequency and duty cycle. The oscillator timing is important because it determines how long the coil will be charged during each cycle. This, along with the input voltage, determines how much energy will be stored in the coil.

The inductor must meet four electrical criteria:

[] **Value-** Low enough inductance so it stores adequate energy at the worst-case, low input voltage.

High enough so excessive and potentially destructive currents are avoided under worst-case high conditions for power-switch transistor on time and high input voltage.

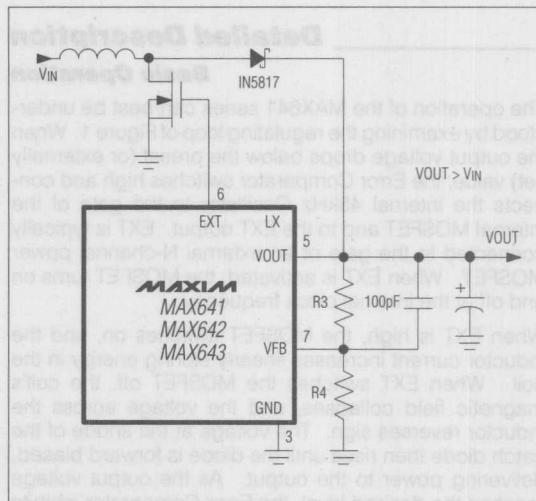


Figure 2. Connections for Adjustable Output Operation

[] **Saturation-** The coil must deliver the correct inductance value at the worst-case, high peak operating current.

[] **EMI-** Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite bobbin types work well for most digital circuits; toroids or pot cores work well for EMI-sensitive analog circuits.

[] **DC resistance-** Winding resistance must be adequately low so efficiency is not affected and self-heating does not occur. Values less than 0.5Ω are usually more than adequate.

Other inductor parameters, such as core loss or self-resonant frequency, are not a factor at the relatively low MAX641/642/643 operating frequency.

Inductor Value- Low Enough?

The problem that bites designs most often, especially in the production or pre-production phase, happens when the inductor value is too high. These units fail to deliver enough load current and exhibit poor load regulation. The worst case is:

- [] Maximum load current
- [] Minimum supply voltage
- [] Maximum inductor value, including tolerance
- [] Maximum on resistance of the switch because it reduces the excitation voltage across the inductor
- [] Worst-case low on time

Fixed Output 10W CMOS Step-Up Switching Regulators

MAX641/642/643

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Inductor Value- High Enough?

The inductor value must be high enough so peak currents do not stress the transistor or cause the inductor core to saturate. Odd symptoms can be traced to excessive inductor currents: low efficiency, rattling heat sinks, whining coils, and increased output ripple. Very low inductor values may result in damaged power transistors.

The slope of the inductor current, and therefore the peak value that it reaches in a given on time, is determined by the supply voltage and the inductor value. The worst case occurs at:

- [] Maximum supply voltage
- [] Minimum inductor value, including tolerance
- [] Minimum on resistance of the switch
- [] Low switching frequency (or maximum switch on time)

Inductor Selection

The inductor equations below must be calculated for both worst-case sets of conditions. The final value chosen should be between the minimum value and maximum value calculated. Within these bounds, the value can be adjusted slightly lower for extra load capability or higher for lowest ripple.

$$[1] \quad I_{pk} = \frac{V_{OUT} + V_{DIODE} - V_{IN}}{(0.25)(V_{IN} - V_{SW})} (I_{OUT})$$

$$[2] \quad L = \frac{V_{IN} - V_{SW}}{I_{pk}} (t_{ON})$$

Where V_{SW} is the voltage drop across the switch in the on state. Conservatively, the worst case is about 0.75V max, 0.25V min with $V_{IN} = +15V$ and 1.5V max, 0.5V min with $V_{IN} = +5V$.

Example: A +5V 10% input must be converted to +15V at 15mA. A Schottky diode (1N5817) and a MAX643B are used.

Calculate maximum inductor value allowed:

$$I_{pk} = \frac{15V + 0.4V - 4.5V}{(0.25)(4.5V - 0.75V)} (15mA) = 174mA$$

$$L = \frac{4.5 - 0.75}{174mA} (8\mu s) = 172\mu H$$

Calculate the minimum inductor value allowed:

$I_{pk} = 450mA$ (from table of max ratings; use the power MOSFET max ratings for external transistor circuits)

$$L = \frac{5.5V - 0.25V}{450mA} (12\mu s) = 140\mu H$$

A value of 160 μH would be a good choice for this application. The "A" grade devices, with tighter oscillator tolerance, allow more output current in a given application.

Application Hints

External MOSFET

An external MOSFET or transistor can be used to drive the inductor in high-power applications. The current handling specifications of the device must match the peak current which flows in the inductor (see Inductor Selection). The only restriction on the size of the external driver is that the EXT output must be able to drive the external device's gate (or base) capacitance at the internal clock rate (45kHz). An external driver may be used to increase operating voltage range of the MAX641/642/643.

Table 2 contains a list of MOSFETs and their manufacturers. Logic level MOSFETs should be used when the supply voltage is less than +5V. Refer to Figures 4 and 5 for circuits requiring external MOSFETs.

Output Filter Capacitor

The MAX641/642/643 output ripple has 2 components which are 90° out of phase. One component results from the change in the stored charge on the filter capacitor with each LX pulse. The other is the product of the capacitor's charge-discharge current and its Equivalent Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high-quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at a reasonable cost are typically achieved with a high-quality aluminum electrolytic, in the 100 μF to 500 μF range, in parallel with a 0.1 μF ceramic capacitor.

Diodes

When the MAX641/642/643 are used with an external power MOSFET, the internal diode can be used if the peak diode current rating (450mA) and maximum package power dissipation ratings are observed. For higher power circuits, an external Schottky diode such as the 1N5817 (1 Amp) or 1N5821 (3 Amp) should be connected between LX and VOUT in parallel with the internal diode. Although 1N4001s and other general purpose rectifiers are rated for high currents, they are not recommended because their slow turn-on time results in excessive losses and poor efficiency.

Fixed Output 10W CMOS Step-up Switching Regulators

Bypassing and Compensation

Since the inductor charging current can be relatively large, high currents flow through the ground connection near the MAX641/642/643. To prevent unwanted feedback, the impedance of the ground path must be as low as possible, and a bypass capacitor (10 μ F) should be at the VOUT pin, even if large filter capacitor are used elsewhere in the circuit.

When large values (>50k Ω) are used for the voltage setting resistors (R3 and R4 of Figure 2), stray capacitance at the VFB input can add a "lag" to the feedback response, destabilizing the regulator and causing output

pulses to occur in bursts. This problem can often be avoided by minimizing pin lengths and circuit board trace size at the VFB node. Normal operation with evenly distributed pulses can also be restored by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

The COMP input allows access to the internal voltage divider so that compensation can also be added when fixed output operation is used. A capacitor connected between VOUT and COMP adds a "lead" to the regulator's response.

Table 1. Representative N-Channel Power MOSFETs

PART NUMBER	PKG.	R _{on} AT (I _{DS} , V _{GS} = X)	V(MAX)	MFG.
IRFD121	4p DIP	0.3 Ω (1.3A, 10V)	60	H/IR
BUZ71A	TO-220	0.12 Ω (6A, 10V)	50	MOT/SI/SM
BUZ21	TO-220	0.1 Ω (9A, 10V)	100	MOT/SI/SM
IRF513	TO-220	0.8 Ω (2A, 10V)	100	H/IR/MOT/SI
IRF530	TO-220	0.18 Ω (8A, 10V)	100	H/IR/MOT/SI
IRF540	TO-220	0.085 Ω (8A, 10V)	100	H/IR/MOT/SI
IRF620	TO-220	0.8 Ω (2.5A, 10V)	200	H/IR/MOT/SI
IRF640	TO-220	0.18 Ω (10A, 10V)	200	H/IR/MOT/SI

Manufacturer Code: H= Harris, IR= International Rectifier, MOT= Motorola, SM= Siemens, SI= Siliconix

N-Channel Logic-Level Power MOSFETs

PART NUMBER	PKG.	R _{on} AT (I _{DS} , V _{GS} = X)	V(MAX)	MFG.
RFP25N06L	TO-220	0.85 Ω (12.5A, 5V)	50	H
RFP12N10L	TO-220	0.20 Ω (6A, 5V)	100	H
PFP15N06L	TO-220	0.14 Ω (7.5A, 5V)	50	H
IRL540	TO-220AB	0.11 Ω (24A, 4V)	100	IR
IRL734	TO-220AB	0.3 Ω (7.8A, 4V)	60	IR
IRZ14	TO-220AB	0.07 Ω (23A, 4V)	60	IR
MTM25N05L	TO-220AB	0.1 Ω (12.5A, 5V)	50	MOT
MTM15N05L	TO-220AB	0.15 Ω (7.5A, 5V)	50	MOT
MTP12N10L	TO-220AB	0.18 Ω (6A, 5V)	100	MOT

Manufacturer Code: H= Harris, IR= International Rectifier, MOT= Motorola

Note: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Fixed Output 10W CMOS Step-Up Switching Regulators

MAX641/642/643

Table 2. Inductance Values for Commonly Encountered Power Supplies (Figure 5)

MAXIM PART NO.	V _{IN} (V)	V _{OUT} (V)	I _{OUT} (mA)	TYP EFF (%)	I _{pk} (A)	PART NO.*	INDUCTOR (L) μH Ω
MAX641	3	5	200	83	1.3	6860-13	100 .10
	3	5	300	80	2.0	6860-09	47 .05
MAX642	5	12	200	91	1.2	6860-08	39 0.05
	5	12	350	89	2	6860-04	18 0.03
	5	12	550	87	3.5	7200-02	12 0.01
MAX643	5	15	100	92	1.2	6860-08	39 0.05
	5	15	150	89	1.5	6860-06	27 0.04
	5	15	225	89	2	6860-04	18 0.03
	5	15	325	85	3.5	7200-02	12 0.01

* Ferrite Bobbin Coils from Caddell-Burns, NY (516) 746-2310

Inductor Saturation

It is important to be sure that the inductor does not saturate, particularly in high-power circuits. Inductor saturation leads to very high current levels through the external boost transistor, causing excessive power dissipation, poor efficiency, and possible damage to the inductor and the external transistor.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

To ensure that the current rating(s) of the FET(s) is not exceeded, the inductance value of the coil, including the manufacturer's tolerances, should never be lower than that used in the calculations or in Table 2. In addition, to ensure that the core does not saturate, the current rating of the coil should be greater than the peak current, I_{pk}.

Coil resistance has a significant effect on the output current. To increase the output current and raise the overall efficiency, the inductor should have a resistance less than a few tenths of an Ohm.

Inductance Values

Inductance values for commonly encountered power supplies are listed in Table 2. The data in Table 2 refers to the circuit in Figure 5.

Typical Applications

Basic High-Power Hookup

Figure 5 shows the standard circuit configuration for a fixed output step-up DC-DC converter. The output power is determined by the current ratings of the external MOSFET and inductor, as well as, the switching time of the EXT output into the gate capacitance of the MOSFET.

Typical switching times are given in the Electrical Characteristics Table.

Low-Power Step-Up Conversion

In low-power applications, the LX output and internal diode may be used instead of an external MOSFET and diode, as shown in Figure 3. The power handling capability of this circuit is about 250mW. See the MAX631 data sheet for inductor selection information.

High-Voltage Operation

If the external MOSFET or transistor has an adequate voltage rating, the output voltage range of the MAX641/642/643 can be extended (Figure 4). The adjustable output mode must be used (VFB connected to external resistors), and the VOUT pin must be connected to the circuit's INPUT voltage.

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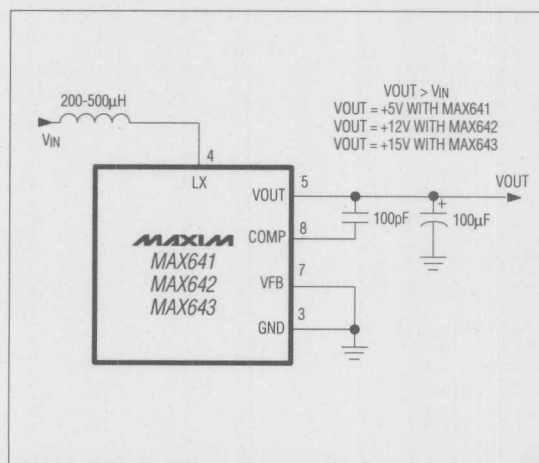


Figure 3. Low-Power, Fixed Output Step-Up Converter Using LX

Fixed Output Low Power Step-up Switching Regulators

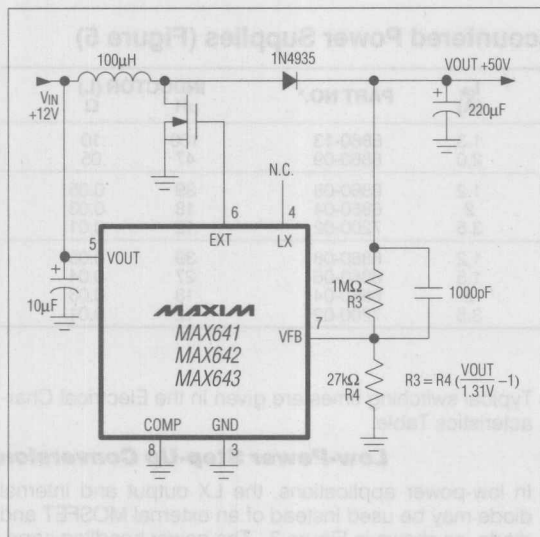


Figure 4. High-Voltage Step-Up Converter

High-Voltage Operation

If the external MOSFET or transistor has an adequate voltage rating, the output voltage range of the MAX641/642/643 can be extended (Figure 4). The adjustable output mode must be used (VFB connected to external resistors), and the VOUT pin must be connected to the circuit's VOUT voltage.

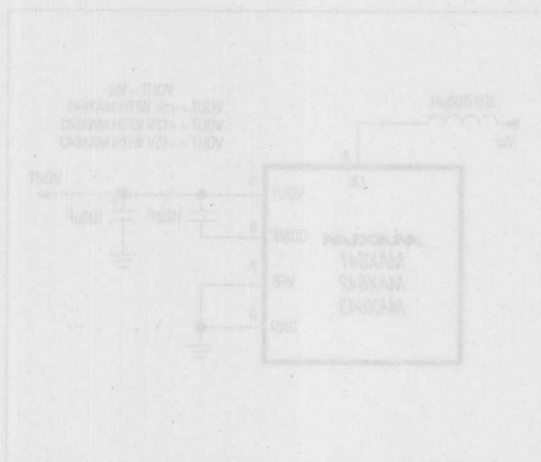


Figure 5. Low-Power Fixed Output Step-Up Converter Using LX

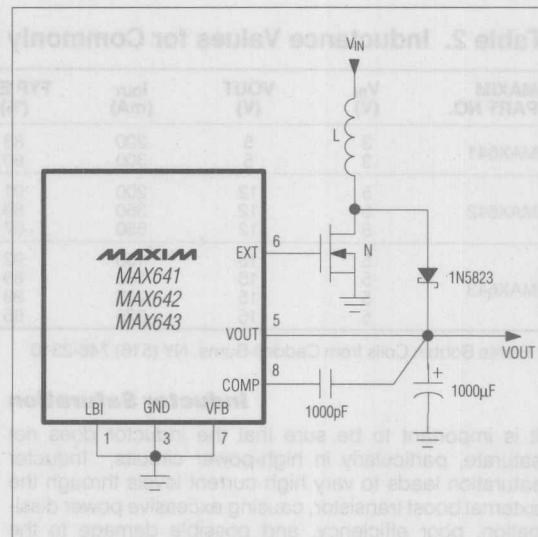


Figure 5. High Output Current Step-Up Converter (See Table 2)

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

To ensure that the current ratings of the FET(s) are not exceeded, the inductance value of the coil, including the manufacturer's tolerances, should never be lower than that used in the calculations or in Table 2. In addition, ensure that the core does not saturate; the current rating of the coil should be greater than the peak current I_{PK} .

Coil resistance has a significant effect on the output current. To increase the output current and raise the overall efficiency, the inductor should have a resistance less than a few tenths of an Ohm.

Inductance Values

Inductance values for commonly encountered power supplies are listed in Table 2. The data in Table 2 refers to the circuit in Figure 5.

Typical Applications

Basic High-Power Hookup

Figure 5 shows the standard circuit configuration for a fixed output step-up DC-DC converter. The output power is determined by the current ratings of the external MOSFET and inductor as well as the switching time of the EXT output into the gate capacitance of the MOSFET.

Fixed Output 10W CMOS Step-Up Switching Regulators

MAX641/642/643

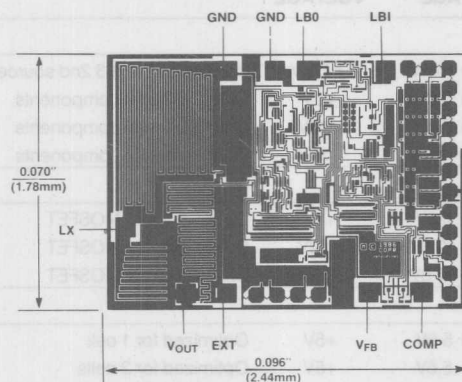
Table 3. Maxim DC-DC Converters

PART NUMBER	DESCRIPTION	INPUT VOLTAGE	OUTPUT VOLTAGE	COMMENTS
Low-Power Boost Converters				
MAX630/4193	DC-DC Boost Converter	2V to 16.5V	$V_{OUT} > V_{IN}$	Improved RC4193 2nd source
MAX631	DC-DC Boost Converter	1.5V to 5.6V	+5V	Only 2 external components
MAX632	DC-DC Boost Converter	1.5V to 12.6V	+12V	Only 2 external components
MAX633	DC-DC Boost Converter	1.5V to 15.6V	+15V	Only 2 external components
High-Power Boost Converters				
MAX641	High-Power Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX642	High-Power Boost Converter	1.5V to 12.6V	+12V	Drives external MOSFET
MAX643	High-Power Boost Converter	1.5V to 15.6V	+15V	Drives external MOSFET
Low-Voltage Boost Converters				
MAX654	Low-Voltage Boost Converter	1.15V to 5.6V	+5V	Optimized for 1 cell
MAX655	Low-Voltage Boost Converter	1.5V to 5.6V	+5V	Optimized for 2 cells
MAX656	Low-Voltage Boost Converter	1.15V to 5.6V	+5V	Drives external MOSFET
MAX657	Low-Voltage Boost Converter	1.15V to 3.6V	+3V	Optimized for 1 cell
MAX658	Low-Voltage Boost Converter	1.5V to 5.6V	+5V	Drives external MOSFET
MAX659	Low-Voltage Boost Converter	1.5V to 3.6V	+3V	Optimized for 2 cells
Inverting Converters				
MAX634/4391	DC-DC Voltage Inverter	2V to 16.5V	up to -20V	Improved RC4391 2nd source
MAX635	DC-DC Voltage Inverter	2V to 16.5V	-5V	Only 3 external components
MAX636	DC-DC Voltage Inverter	2V to 16.5V	-12V	Only 3 external components
MAX637	DC-DC Voltage Inverter	2V to 16.5V	-15V	Only 3 external components
Step-Down Converter				
MAX638	DC-DC Voltage Stepdown	3V to 16.5V	$V_{OUT} < V_{IN}$	Only 3 external components
Charge-Pump Converters				
MAX680	\pm Output Charge Pump	2V to 6V	$\pm 2V_{IN}$	4 external capacitors
MAX681	\pm Output Charge Pump	2V to 6V	$\pm 2V_{IN}$	MAX680 with internal capacitors
ICL7660	Negative Charge Pump	1.5V to 10V	$-V_{IN}$	Not regulated
ICL7662/SI7661	Negative Charge Pump	4.5V to 20V	$-V_{IN}$	Not regulated
Dual Output Converters				
MAX742	Current-Mode Controller	+5V	$\pm 15V/\pm 12V$	Drives external MOSFETs
MAX743	Current-Mode Regulator	+5V	$\pm 15V/\pm 12V$	3W output

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Fixed Output 10W CMOS Step-up Switching Regulators

Chip Topography



Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE
MAX643XCPA	0°C to +70°C	8 Plastic DIP
MAX643XCSA	0°C to +70°C	8 Narrow SO
MAX643XC/D	0°C to +70°C	8 Dice
MAX643XEPA	-40°C to +85°C	8 Plastic DIP
MAX643XESA	-40°C to +85°C	8 Narrow SO
MAX643XEJA	-40°C to +85°C	8 CERDIP
MAX643XMJA	-55°C to +125°C	8 CERDIP

*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.

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INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

-48V to +5V Output Switching DC-DC Converter

General Description

The MAX650 is a low-power fixed +5V output switching DC-DC converter designed for operation from very high negative input voltages. All control functions and a 140V, 250mA PNP transistor are contained in this device, reducing external components. A soft-start eliminates overshoot on turn on, and a Shutdown pin (SHDN) allows the output to be turned on and off. In addition, peak current limiting is provided on the PNP output.

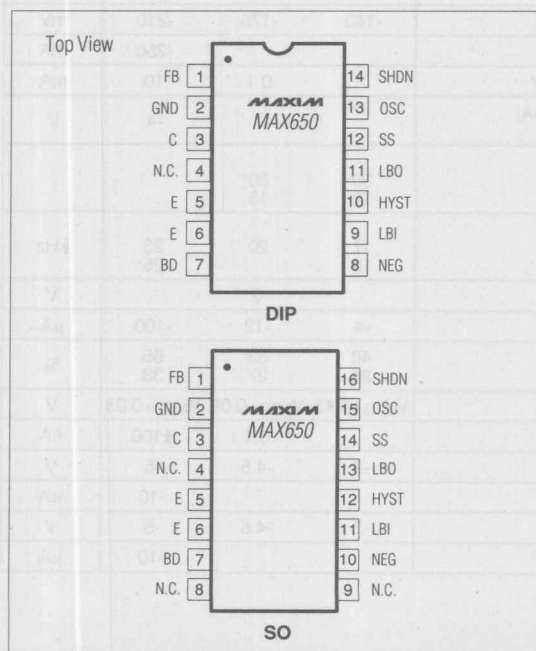
The MAX650 features user-controllable operating frequency and a separate low voltage detector with adjustable hysteresis for monitoring the supply voltage. It can be set to trip at any negative voltage with a simple voltage divider.

The MAX650 is available in an A version with $\pm 5\%$ output voltage tolerance and a B version with $\pm 10\%$ tolerance.

Applications

Telephone (-48V) Powered Devices
Negative Input to +5V Converter

Pin Configurations



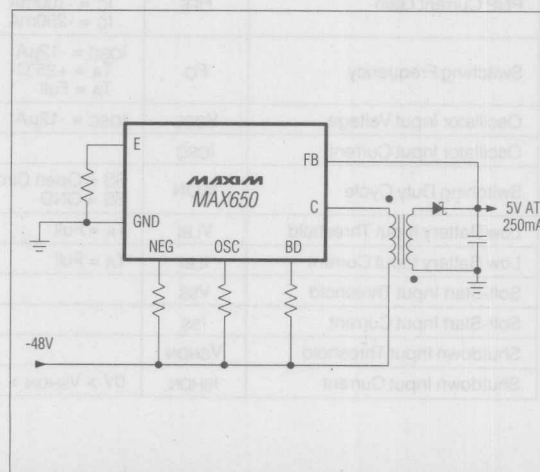
Features

- ◆ +5V at 250mA From a -48V Source
- ◆ Selectable Soft-Start Function
- ◆ Shutdown Pin for Output On-Off Control
- ◆ Internal 140V, 250mA Switching PNP Transistor
- ◆ Low Component Count
- ◆ Low Battery Voltage Detector

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX650ACPD	0°C to +70°C	14 Plastic DIP
MAX650ACWE	0°C to +70°C	16 Wide SO
MAX650AC/D	0°C to +70°C	Dice
MAX650BCPD	0°C to +70°C	14 Plastic DIP
MAX650BCWE	0°C to +70°C	16 Wide SO
MAX650BC/D	0°C to +70°C	Dice
MAX650AEPD	-40°C to +85°C	14 Plastic DIP
MAX650AEWE	-40°C to +85°C	16 Wide SO
MAX650BEPD	-40°C to +85°C	14 Plastic DIP
MAX650BEWE	-40°C to +85°C	16 Wide SO
MAX650AMJD	-55°C to +125°C	14 Ceramic DIP
MAX650BMJD	-55°C to +125°C	14 Ceramic DIP

Typical Operating Circuit



MAXIM

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Maxim Integrated Products 5-37

MAX650

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-48V to +5V Output Switching DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise noted, all voltages are referenced to the GND terminal.)

Collector (C) Current, I_C	-300mA
Collector (C) Voltage, V_C	-140V
Emitter (E) Voltage, V_E	-1V to +0.3V
Base BD Current, I_{BD}	-50mA
FB Voltage, V_{FB}	+7V
LBI, SS and SHDN Currents	±10mA
LBO Voltage, V_{LBO}	(V_{NEG} -0.3) to (V_{NEG} +15) V
Voltage at OSC, BD, HYST, LBI, SS, and SHDN	(V_{NEG} -0.3) to 0V
NEG Current, I_{NEG}	-25mA
OSC Current, I_{OSC}	±10mA
LBO Sink Current, I_{LBO}	-10mA

HYST Source Current, I_{HYST}	±10mA
Power Dissipation	
Plastic DIP (derate 6.5mW/°C above 25°C)	470mW
Small Outline (derate 10mW/°C above 75°C)	750mW
CERDIP (derate 11mW/°C above 75°C)	825mW
Operating Temperature	
MAX650C	0°C to +70°C
MAX650E	-40°C to +85°C
MAX650M	-55°C to +125°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(GND = 0V, T_A = +25°C, unless otherwise noted. MIN and MAX values are based on magnitude without regard to sign.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output (load) Voltage	V_{FB}	T_A = Full MAX650A MAX650B	+4.75 +4.5	+5 +5	+5.25 +5.5	V
Feedback Input Current	I_{FB}	V_{FB} = +5V		40	100	μA
Internal Zener Voltage	V_{NEG}	T_A = Full, I_{NEG} = -500μA	-6	-7	-8	V
Internal Zener Current	I_{NEG}	T_A = Full	-0.3	-0.5	-10	mA
Current Sense Voltage	V_E		-140	-175	-210	mV
Peak Collector Current	I_C				-250	mA
Collector Leakage Current	I_C	T_A = Full, V_C = -140V		0.1	10	mA
Collector (C) Saturation Voltage	V_{SAT}	T_A = Full, I_C = -250mA, I_{BD} = -25mA			-4	V
PNP Current Gain	H_{FE}	T_A = Full, V_C ≤ -4V I_C = -100mA I_C = -250mA	20 10	80 13		
Switching Frequency	F_O	I_{OSC} = -12μA T_A = +25°C T_A = Full	17 15	20	23 25	kHz
Oscillator Input Voltage	V_{OSC}	I_{OSC} = -12μA		-2		V
Oscillator Input Current	I_{OSC}		-4	-12	-100	μA
Switching Duty Cycle	%ON	SS = Open Circuit SS = GND	48 24	53 27	65 33	%
Low Battery Input Threshold	V_{LBI}	T_A = Full	$V_{NEG}+0.13$	$V_{NEG}+0.08$	$V_{NEG}+0.03$	V
Low Battery Input Current	I_{LBI}	T_A = Full		0.1	±100	nA
Soft-Start Input Threshold	V_{SS}		-3	-4.5	-5	V
Soft-Start Input Current	I_{SS}				-10	μA
Shutdown Input Threshold	V_{SHDN}		-3	-4.5	-5	V
Shutdown Input Current	I_{SHDN}	0V > V_{SHDN} > -3V			-10	μA

-48V to +5V Output Switching DC-DC Converter

Pin Description

MAX650

PIN # 14-PIN DIP	PIN # 16-PIN Wide SO	NAME	FUNCTION
1	1	FB	Feedback Input. The 5V output is connected to FB, which regulates the output voltage. This input sinks approximately 40µA to VNEG.
2	2	GND	Ground. This is the positive side of the -48V input supply and the negative side of the +5V output. All specified voltages are referenced to this pin.
3	3	C	Output (collector) of the PNP transistor switch. Connect to the transformer primary. This pin can withstand up to -140V on the flyback cycle and sources up to 250mA from E, depending on the base drive current at BD.
4	4, 8, 9	N.C.	No Connection. These pins are open circuit.
5, 6	5, 6	E	Current sense input (emitter) of PNP transistor. Connect to GND, either directly or through a low-value sense resistor. When the voltage on these pins is more negative than -175mV, the PNP transistor is turned off for an entire cycle.
7	7	BD	Base Drive Input of PNP transistor. Figure 1.
8	10	NEG	Negative Power Connection. Anode of 7V Zener diode whose cathode is connected to GND. An external series limiting resistor is required between this pin and the -48V input supply. This resistor must also sink the LBO current (up to 100µA).

Operating Principle

The MAX650 is a flyback switching converter; energy from the input supply is first transferred to the transformer core through the primary winding, then discharged from the secondary winding into the load. A typical circuit consists of a battery in series with the primary coil of a transformer, a switch, a rectifier, and a filter. (Figure 3). During the first portion of the cycle, the switch is closed, and current builds up in the primary storing energy in the form of a magnetic field in the transformer's core.

During the second portion, or "flyback" part of the cycle, the switch opens, the magnetic field collapses, and the energy stored in the core is discharged through the secondary winding into the rectifier and the load. The switch is controlled by an oscillator whose output is gated

PIN # 14-PIN DIP	PIN # 16-PIN Wide SO	NAME	FUNCTION
9*	11*	LBI*	Low Battery Monitor Input. CMOS input.
10*	12*	HYST*	Low Battery Monitor Hysteresis Output. This P-channel FET sources up to 80µA to GND when the LBI input is 80mV more positive than VNEG; otherwise HYST is an open circuit.
11	13	LBO	Low Battery Monitor Output. Sinks up to 100µA to NEG when LBI is 80mV more positive than VNEG.
12*	14*	SS*	Soft-Start Input. Normally left open circuit for 50% duty cycle. Connect to GND through a capacitor to change the oscillator duty cycle to 25% and reduce input current on startup.
13	15	OSC	Oscillator Frequency Control Input (Figure 2). The voltage on this pin is approximately -2V.
14	16	SHDN	Shutdown Input. Leave open circuit or connect to NEG for normal operation. Connect to GND through a 100kΩ resistor to stop oscillator and turn-off output.

* Voltage limitations on HYST, LBI, and SS terminals.

HYST, LBI, and SS should not be connected to GND. This is because protection diodes associated with these terminals will be forward biased, interfering with correct operation. If low-voltage detection is not required, LBI must be connected to NEG, and the HYST terminal left open circuit. SS may be connected to GND through a 0.1µF, or smaller capacitor, to initiate soft-start on power up. If soft-start is not required, SS should also be connected to NEG.

on and off by a comparator that monitors the output voltage. When the output voltage is below the comparator threshold (+5V) the switch turns on for the first half of the oscillator cycle. When the output voltage is above the comparator threshold, the switch skips an entire oscillator cycle. This "pulse-skipping" technique regulates by varying the average number of cycles over time rather than varying the duty cycle of the switch on each cycle.

Figure 4 shows the block diagram of the MAX650. PNP transistor, Q1, controls the input current to the transformer. The emitter of this transistor can be connected to GND directly or through a low-value current sense resistor. The collector of the transistor connects to the primary of the transformer. Transistor base drive is set by an external resistor connected to BD. The oscillator frequency is set by another external resistor at OSC.

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-48V to +5V Output Switching DC-DC Converter

A CMOS voltage comparator, for low battery or low input voltage detection, is included in the MAX650. Its input threshold voltage, LBI, is biased 80mV above the negative supply pin, NEG. The output, LBO, is an N-channel FET which sinks up to 100 μ A to NEG, and its drain can be connected to positive potentials above GND (up to 15V above VNEG).

Circuit Details

A typical application circuit is shown in Figure 4. The basic operation is set by 4 external resistors, RNEG, ROSC, RBD, and RSENSE. Output current capability is determined by the transformer, as described later.

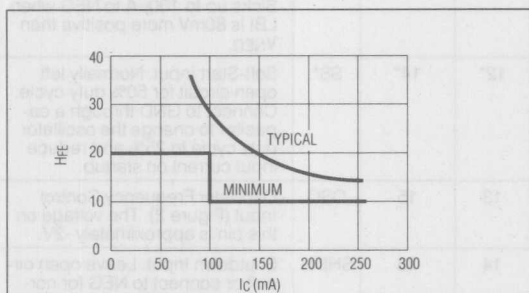


Figure 1. H_{FE} vs. Collector Current

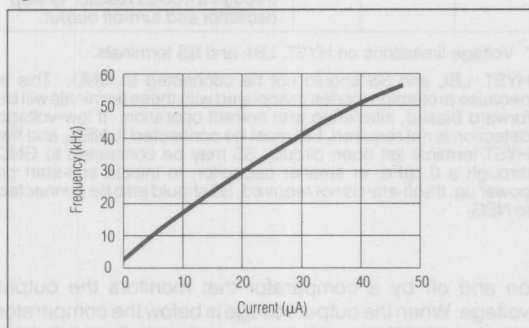


Figure 2. Oscillator Frequency vs. Oscillator Current

Supply Current, RNEG

Although the MAX650 is meant to operate with high negative supply voltages (V_{INMIN} to V_{INMAX}), it uses approximately -7V internally. This is set by an internal 7V zener diode connected between GND and NEG. The current through this diode must be more than 300 μ A and less than 10mA. It is set by the size of the external voltage dropping resistor, RNEG, and the supply voltage, V_{INMIN} .

$$[1] \quad R_{NEG} = (V_{INMIN} - V_{NEG}) / I_{NEG}$$

where,

$$[2] \quad I_{NEG} = 500\mu A + I_{LBO}$$

(Note that V_{INMIN} , V_{NEG} and all currents are negative, but the calculations are simplified by using positive values.) If the low battery function is used, the LBO output sinks or furnishes load current, I_{LBO} , through the NEG pin, and this current must be added to the I_{NEG} current calculation as in Eq. 2.

Resistor, RNEG, should be calculated using the lowest supply voltage, V_{INMIN} , to insure an adequate I_{NEG} current.

Calculations for a typical application look like this:

$$V_{INMIN} = -36V; V_{INMAX} = -50V$$

$$LBO \text{ output current} = -100\mu A$$

The supply resistance is calculated for the lowest supply voltage and the highest current.

$$[2] \quad I_{NEG} = 500\mu A + I_{LBO} \\ = 500\mu A + 100\mu A = 600\mu A$$

$$[1] \quad R_{NEG} = (V_{INMIN} - V_{NEG}) / I_{NEG} \\ = (36V - 7V) / 600\mu A \\ = 48,333\Omega \text{ (use } 47k\Omega)$$

With the highest input voltage, the maximum current is:

$$[3] \quad I_{NEG} = (V_{INMAX} - V_{NEG}) / R_{NEG} \\ = (50V - 7V) / 47,000\Omega \\ = 915\mu A$$

Oscillator Frequency, Rosc

The MAX650 varies its oscillator frequency in order to keep the energy delivered to the primary of the transformer constant with varying input voltages. The oscillator frequency is a nearly linear function of the current into the OSC pin. The frequency is set by resistor, ROSC, connected between OSC and the negative supply volt-

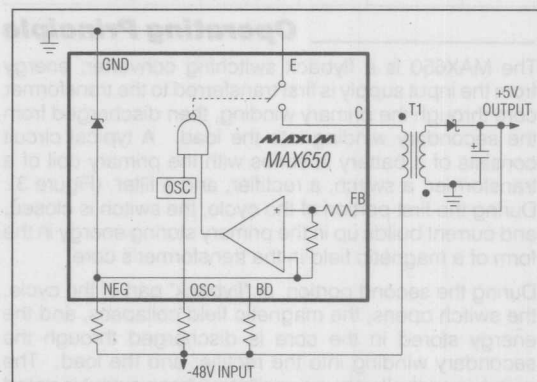


Figure 3. Typical Circuit

-48V to +5V Output Switching DC-DC Converter

MAX650

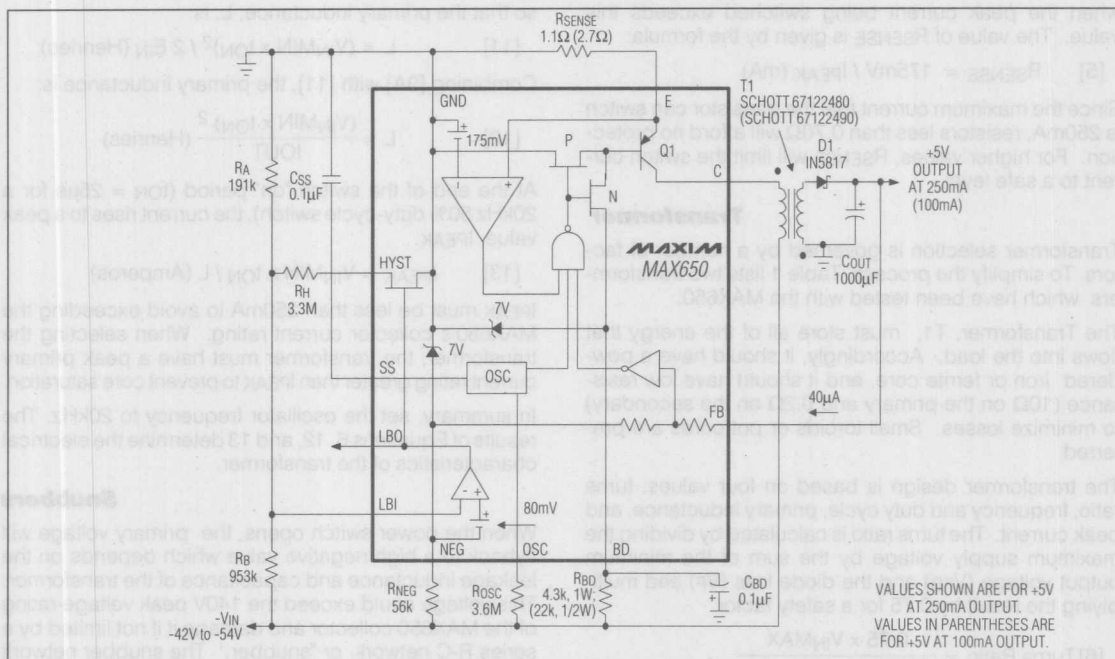


Figure 4. Typical Application Circuit

age. Therefore, the oscillator frequency is nearly linearly proportional to the supply voltage, and the switch "on" period is inversely proportional to the supply voltage. The power stored in the primary is nearly constant with changes in supply voltage since the peak current through the switch and the primary of the transformer are proportional to the product of the "on" period of the switch and the input voltage.

Normally, the oscillator frequency is 20kHz when I_{OSC} is $-12\mu A$, as shown in Figure 2. The value of R_{OSC} is:

$$[4] \quad R_{OSC} = V_{INMIN} / I_{OSC}$$

Soft-Start

The duty cycle of the output transistor is controlled by the SS pin which has a $1\mu A$ pulldown current to the NEG pin. When the SS pin is left open or connected to GND, soft-start is disabled and the duty cycle of the switch is approximately 50%. When it is temporarily grounded through a $0.1\mu F$ capacitor, the switch is on for 25% of the time and off for 75%, until the capacitor is charged to V_{NEG} . The MAX650 starts up slowly each time that power is applied and then switches over to normal operation. The soft-start circuit is shown in Figure 5. Note that the SS pin cannot be connected directly to GND.

Current Sense, R_{SENSE}

The Emitter, E, of the PNP transistor can be connected directly to GND. But, in order to protect the output transistor against destructive short-circuit currents, it should be connected to GND via a low-value current sense resistor, R_{SENSE} . An internal comparator compares the voltage generated across the sense resistor at E to an internal $-175mV$ reference and turns off the transistor

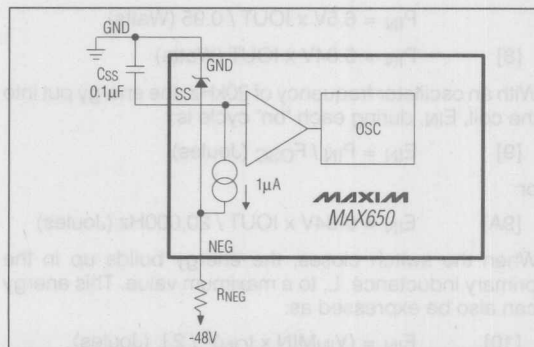


Figure 5. Soft-Start Circuit

-48V to +5V Output Switching DC-DC Converter

when the peak current being switched exceeds this value. The value of R_{SENSE} is given by the formula:

$$[5] \quad R_{SENSE} = 175\text{mV} / I_{PEAK} \text{ (mA)}$$

Since the maximum current that the transistor can switch is 250mA, resistors less than 0.70Ω will afford no protection. For higher values, R_{SENSE} will limit the switch current to a safe level.

Transformer

Transformer selection is governed by a number of factors. To simplify the process, Table 1 lists two transformers which have been tested with the MAX650.

The Transformer, T1, must store all of the energy that flows into the load. Accordingly, it should have a powdered iron or ferrite core, and it should have low resistance (10Ω on the primary and 0.2Ω on the secondary) to minimize losses. Small toroids or pot cores are preferred.

The transformer design is based on four values: turns ratio, frequency and duty cycle, primary inductance, and peak current. The turns ratio is calculated by dividing the maximum supply voltage by the sum of the minimum output voltage (V_{FB}) and the diode loss (V_F) and multiplying the result by 0.75 for a safety factor.

$$[6] \text{ Turns Ratio} = \frac{0.75 \times V_{INMAX}}{(V_{FBMIN} + \text{diode } V_F)}$$

The design works backwards from the load as follows: the diode and transformer secondary resistance losses can be lumped together as "1V" so that the maximum secondary output voltage is 6.5V. Knowing the required output current, I_{OUT} , the Output Power, P_{OUT} , becomes:

$$[7] \quad P_{OUT} = 6.5V \times I_{OUT} \text{ (Watts)}$$

Assuming 95% efficiency in the transformer (transformer only, not the whole circuit), the input power to the primary, P_{IN} is:

$$P_{IN} = 6.5V \times I_{OUT} / 0.95 \text{ (Watts)}$$

$$[8] \quad P_{IN} = 6.84V \times I_{OUT} \text{ (Watts)}$$

With an oscillator frequency of 20kHz, the energy put into the coil, E_{IN} , during each "on" cycle is:

$$[9] \quad E_{IN} = P_{IN} / F_{OSC} \text{ (Joules)}$$

or:

$$[9A] \quad E_{IN} = 6.84V \times I_{OUT} / 20,000\text{Hz} \text{ (Joules)}$$

When the switch closes, the energy builds up in the primary inductance, L , to a maximum value. This energy can also be expressed as:

$$[10] \quad E_{IN} = (V_{INMIN} \times t_{ON})^2 / 2L \text{ (Joules)}$$

so that the primary inductance, L , is:

$$[11] \quad L = (V_{INMIN} \times t_{ON})^2 / 2E_{IN} \text{ (Henries)}$$

Combining [9A] with [11], the primary inductance is:

$$[12] \quad L = \frac{(V_{INMIN} \times t_{ON})^2}{I_{OUT}} \text{ (Henries)}$$

At the end of the switch "on" period ($t_{ON} = 25\mu\text{s}$ for a 20kHz 50% duty-cycle switch), the current rises to a peak value, I_{PEAK} .

$$[13] \quad I_{PEAK} = V_{INMIN} \times t_{ON} / L \text{ (Amperes)}$$

I_{PEAK} must be less than 250mA to avoid exceeding the MAX650's collector current rating. When selecting the transformer, the transformer must have a peak primary current rating greater than I_{PEAK} to prevent core saturation.

In summary, set the oscillator frequency to 20kHz. The results of Equations 6, 12, and 13 determine the electrical characteristics of the transformer.

Snubbers

When the power switch opens, the primary voltage will flyback to a high negative value which depends on the leakage inductance and capacitance of the transformer. This voltage could exceed the 140V peak voltage rating of the MAX650 collector and damage it if not limited by a series R-C network, or "snubber." The snubber network is usually placed in parallel with the transformer primary, and the R-C values depend on the transformer characteristics and must be determined experimentally. 1000Ω in series with 100pF is a good starting place. The snubber does dissipate some power, reducing the overall efficiency, but this can be minimized or eliminated by using a transformer with low leakage inductance.

Larger R and smaller C values improve efficiency, but may not adequately suppress the negative spike at C. Smaller R and larger C values reduce the size of the spike, but then reduce efficiency. The optimum snubber balances these two goals.

Under ideal conditions, the snubber may be omitted. If either of the two transformers shown in Table 1 is used, the snubber is not needed.

Base Drive, R_{BD}

The output transistor, Q1, is turned on by a combination of the oscillator "on" pulse: the output voltage comparator output high, the sense comparator high, and the base drive current. The output transistor is turned off by a P-channel FET that shorts its base to GND.

In order to conserve power, the base drive current to the switching PNP transistor is set by adjusting current through the base drive pin, BD. I_{BD} is set to a value that insures that Q1 nearly saturates when it is turned on,

-48V to +5V Output Switching DC-DC Converter

MAX650

based on the minimum beta for the output current. For example:

$$[14] \quad I_{BD} = I_{PEAK} / HFE$$

The HFE vs. collector current is shown in Figure 1.

The base drive circuit includes a shunt zener that clamps the base drive voltage to VNEG during the off period. Thus, for half of the cycle the current through BD is wasted. This loss can be recovered, however, if a 0.1μF capacitor is placed between BD and GND. This capacitor effectively captures the lost current and makes it available for the whole cycle. More importantly, it effectively halves the required base drive current so that the base resistor is:

$$[15] \quad R_{BD} = 2 \times (V_{INMIN} - 7V) / I_{BD}$$

Note that with high current designs, RBD may need to dissipate up to 600mW.

Capacitors

The output capacitor should be at least 10μF, increasing approximately 1μF/mA of output current. Low ESR capacitors, such as tantalums, are preferred. But, if aluminum electrolytics are used, each should be paralleled with a 0.1μF disk ceramic. Because of possible switching transients, 0.1μF should also be connected between NEG and GND.

Diodes

Schottky diodes are preferred for the secondary rectifier. Their low forward voltage drop and fast switching times make them the best choice for efficiency. The 1N5817 is a good example.

Low Battery Monitor

A low battery monitor with adjustable hysteresis is built into the MAX650. When LBI is connected to NEG (approximately -7V), LBO sinks up to -100μA to NEG, and the HYST pin, a P-channel FET drain, sources up to 100μA to GND. When LBI is connected to a voltage more positive than -7V, LBO and HYST outputs are open circuits. Normally LBI is connected to the negative supply via a voltage divider to GND, and a hysteresis resistor, RH, is connected between HYST and LBI. The resistors are shown in Figure 6 and are calculated by the following formulas:

$$[16] \quad R_B = 20 \times (V_{INMAX} - 7V) (k\Omega)$$

$$[17] \quad R_A = \frac{7V \times R_B}{V_{TL} - 7V}$$

Where VTL is the low threshold voltage input, and VINMAX is the maximum power-supply voltage. Both are positive in these calculations.

When hysteresis is used, the value of RH, which would otherwise be open circuit, is determined by:

$$[18] \quad R_H = \frac{R_A \times R_B \times 7V}{R_A \times (V_{TH} - 7V) - (7V \times R_B)} (k\Omega)$$

or:

$$[18A] \quad R_H = \frac{V_{TL}}{(V_{TH} - V_{TL})} \times \frac{R_A \times R_B}{R_A + R_B} (k\Omega)$$

Where VTL is the lower threshold voltage, and VTH is the higher threshold voltage (again using positive values). The hysteresis is the difference between VTH and VTL.

Since the voltage at NEG has a range of -6V to -8V (over temperature) LBI and, thus, the higher and lower threshold voltages, cannot be set to better than ±16%.

Voltage Limitations at HYST, LBI, and SS

These three terminals may not be connected directly to GND. Connection to GND forward biases diodes associated with these terminals and interferes with the correct operation of the device. If the low voltage monitor is not

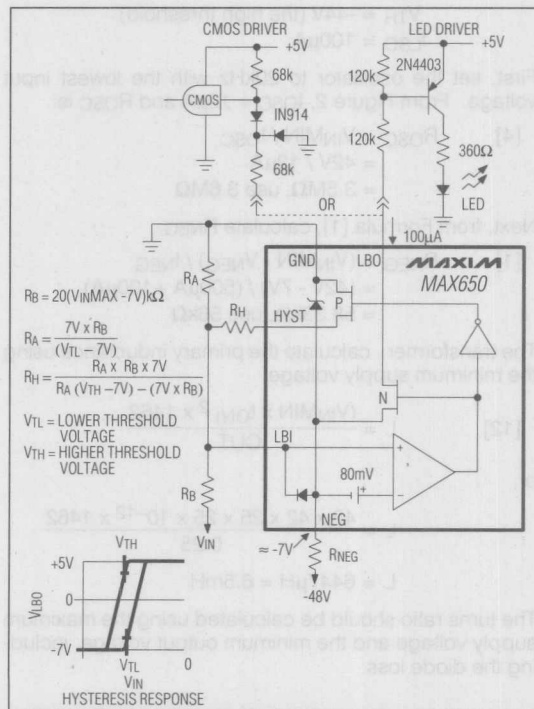


Figure 6. Low Battery Detector Circuit

-48V to +5V Output Switching DC-DC Converter

required, LBI should be connected to NEG and HYST left open circuit. SS may be connected to GND through a capacitor to initiate soft start on power-up. If the soft-start function is not required, SS must be connected to NEG.

Shutdown

The SHDN trip voltage is typically -4.5V. If the function is not required, SHDN may be left open circuit or connected to NEG. The terminal has a 1 μ A pulldown current to NEG. To activate SHDN, this terminal may be raised positively above -4.5V and connected to GND or to a positive voltage of up to +15V with respect to NEG.

A Design Example

Figure 4 shows a complete circuit with all values. Table 1 lists the transformers that may be used to produce +5V at 250mA or 100mA. These values are derived from the following procedure, which may be adjusted for any input voltage range and output current:

$$V_{INMIN} = -42V$$

$$V_{INMAX} = -54V$$

$$\text{Output} = +5V \text{ at } 250mA$$

$$V_{TL} = -42V \text{ (the low threshold)}$$

$$V_{TH} = -44V \text{ (the high threshold)}$$

$$I_{LBO} = 100\mu A$$

First, set the oscillator to 20kHz with the lowest input voltage. From Figure 2, $I_{OSC} = 12\mu A$ and R_{OSC} is:

$$\begin{aligned} [4] \quad R_{OSC} &= V_{INMIN} / I_{OSC} \\ &= 42V / 12\mu A \\ &= 3.5M\Omega, \text{ use } 3.6M\Omega \end{aligned}$$

Next, from Formula [1], calculate R_{NEG} .

$$\begin{aligned} [1] \quad R_{NEG} &= (V_{INMIN} - V_{NEG}) / I_{NEG} \\ &= (42V - 7V) / (500\mu A + 100\mu A) \\ &= 58.33k\Omega, \text{ use } 56k\Omega \end{aligned}$$

The transformer: calculate the primary inductance using the minimum supply voltage.

$$[12] \quad L = \frac{(V_{INMIN} \times t_{ON})^2 \times 1462}{I_{OUT}}$$

or,

$$L = \frac{42 \times 42 \times 25 \times 25 \times 10^{-12} \times 1462}{0.25}$$

$$L = 6447\mu H = 6.5mH$$

The turns ratio should be calculated using the maximum supply voltage and the minimum output voltage, including the diode loss.

$$[6] \quad \text{Turns Ratio} = \frac{0.75 \times V_{INMAX}}{(V_{FBMIN} + \text{diode } V_F)}$$

$$= 0.75 \times 54 / (4.5 + .4) = 40.5 / 4.9$$

$$\text{Turns Ratio} = 8.27, \text{ use } 8$$

Calculate the peak current in the primary and the transistor using the minimum input voltage again.

$$\begin{aligned} [13] \quad I_{PEAK} &= V_{INMIN} \times t_{ON} / L \\ &= 42 \times 25 \times 10^{-6} / (6500 \times 10^{-6}) \\ &= 162mA \end{aligned}$$

From Figure 1, when $I_C = 162mA$ and $H_{FE} = 10$, and from Formula 14:

$$\begin{aligned} [14] \quad I_{BD} &= I_{PEAK} / H_{FE} \\ &= .162 / 10 = 0.0162A \end{aligned}$$

Calculate the Base Drive Resistor, R_{BD} , from Formula 15 using $V_{INMIN} = 42V$.

$$\begin{aligned} [15] \quad R_{BD} &= 2 \times (V_{INMIN} - 7V) / I_{BD} \\ &= 2 \times (42V - 7V) / 0.0162A \\ &= 4321\Omega, \text{ use } 4.3k\Omega \end{aligned}$$

Note that with the maximum supply voltage, the power dissipated by R_{BD} is:

$$\begin{aligned} P_{BD} &= V_{BD}^2 / R_{BD} \\ &= (54 - 7)^2 / 4300 \\ &= 0.52W \end{aligned}$$

Next, calculate value of R_{SENSE} .

$$\begin{aligned} [5] \quad R_{SENSE} &= 175(mV) / I_{PEAK}(mA) \\ &= .175V / .162A \\ &= 1.08\Omega, \text{ use } 1.1\Omega \end{aligned}$$

Last, calculate the LBI resistors.

$$\begin{aligned} [16] \quad R_B &\approx 20 \times (V_{INMAX} - 7V) \text{ (k}\Omega\text{)} \\ &\approx 20 \times (54 - 7) = 940k, \text{ use } 953k\Omega \end{aligned}$$

$$\begin{aligned} [17] \quad R_A &= \frac{7V \times R_B}{V_{TL} - 7V} \\ &= 7 \times 953k / (42 - 7) = 191k\Omega \end{aligned}$$

$$\begin{aligned} [18] \quad R_H &= \frac{R_A \times R_B \times 7}{R_A \times (V_{TH} - 7V) - (7V \times R_B)} \\ &= \frac{191k \times 953k \times 7}{191k \times (44 - 7) - (7 \times 953k)} \\ &= 3218k, \text{ use } 3.3M \end{aligned}$$

-48V to +5V Output Switching DC-DC Converter

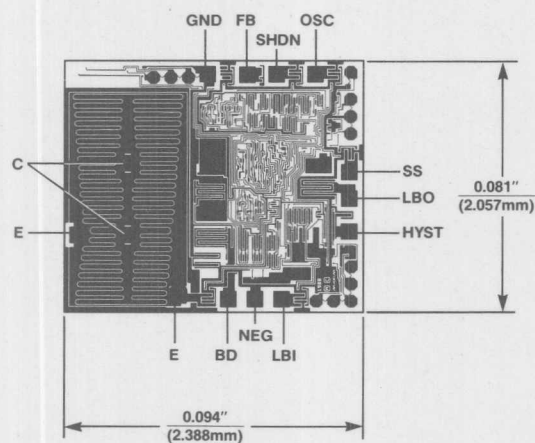
MAX650

Table 1. Transformer and Resistor Selection Guide

SUPPLY V (NEGATIVE)	R _{BD} (k Ω)	I _{OUT} (mA AT 5V)	MANUFACTURER	MODEL #	PRIMARY L TURNS RATIO (PRI:SEC)	
42 to 54	4.3*	250	Schott Corp.	67122480	6.45mH	8:1
42 to 54	22*	100	Schott Corp.	67122490	16.0mH	8:1

* Use 0.1 μ F from BD to GND, R_{NEG} = 56k, R_{OSC} = 3.6M, Schott Corporation: (615) 889-8800.

Chip Topography



5

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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5-45

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

Low Voltage Step-Up DC-DC Converters

General Description

The MAX654-659 step-up DC-DC converters operate from low input voltages such as those supplied by single-cell batteries. They feature a low battery indicator and can run in standby mode to prolong battery life. A Power Ready output provides a means to control external circuitry when standby mode is used.

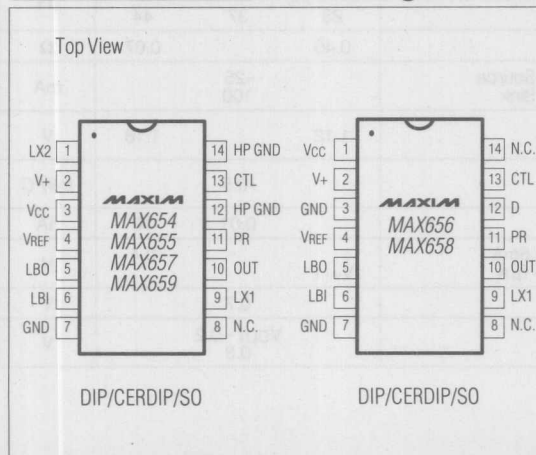
The performance characteristics of each device are listed in the following table. The MAX654/656/657 are optimized for single-cell input, while the MAX655/658/659 work best with two series alkaline or NiCad cells, or one lithium cell. The MAX654/655/657/659 contain an internal power MOSFET, while an external MOSFET is required with the MAX656/658.

PART	TYP INPUT RANGE (V)	OUT (V)	POWER SWITCH	OUTPUT (mA)
MAX654	1.15-1.56	5	Internal	40
MAX655	2.30-3.10	5	Internal	60
MAX656	1.15-1.56	5	Ext MOSFET	170
MAX657	1.15-1.56	3	Internal	60
MAX658	2.30-3.10	5	Ext MOSFET	110
MAX659	2.30-3.10	3	Internal	60

Applications

Battery-Powered Devices
Single-Cell Instruments
Pagers and Radio Controlled Receivers
4-20mA Loop Powered Instruments

Pin Configurations



Features

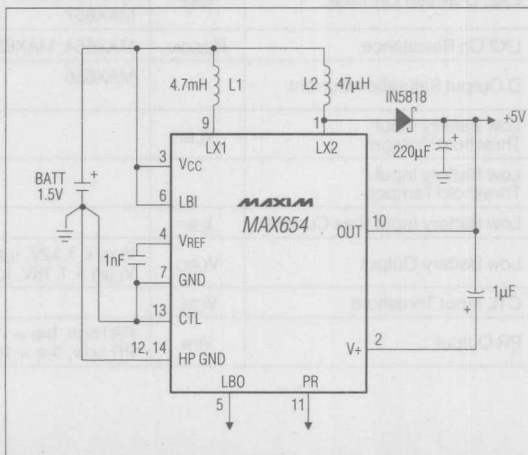
- ◆ +5V at 170mA from a Single-Cell Battery
- ◆ Guaranteed Start-Up at 1.15V
- ◆ Minimum Component Count
- ◆ Shutdown Mode—80μA Quiescent Current
- ◆ Low Battery Indication
- ◆ Power Ready Function

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX654CPD	0°C to +70°C	14 Plastic DIP
MAX654CSD	0°C to +70°C	14 Narrow SO
MAX654C/D	0°C to +70°C	Dice
MAX654EPD	-40°C to +85°C	14 Plastic DIP
MAX654ESD	-40°C to +85°C	14 Narrow SO
MAX654MJD	-55°C to +125°C	14 CERDIP
MAX655CPD	0°C to +70°C	14 Plastic DIP
MAX655CSD	0°C to +70°C	14 Narrow SO
MAX655C/D	0°C to +70°C	Dice
MAX655EPD	-40°C to +85°C	14 Plastic DIP
MAX655ESD	-40°C to +85°C	14 Narrow SO
MAX655MJD	-55°C to +125°C	14 CERDIP

Ordering information continued on page 5-56.

Typical Operating Circuit



MAXIM

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MAX654-659

Low Voltage Step-Up DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Peak Voltage at LX1 Pin	+16V
Peak Voltage at LX2 or V _{CC} Pin	+6.6V
Supply Voltage to L1	+15V
Supply Voltage to L2, V _{CC}	+5.6V
Peak Current, LX1	50mA
Peak Current, LX2	1.6A
LBO Output Current	50mA
Input Voltage, CTL, LBI (Note 1)	-0.3V to (V ₊ + 0.3V)

Operating Temperature	
MAX65XCXX	0°C to +70°C
MAX65XEXX	-40°C to +85°C
MAX65MXX	-55°C to +125°C
Power Dissipation	
Plastic DIP (derate 10mW/°C above 70°C)	800mW
SO (derate 8.7mW/°C above 70°C)	695mW
CERDIP (derate 9.5mW/°C above 70°C)	750mW
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 Sec)	+300°C

Note 1: V₊ is generated at LX1. In low current mode, it is 4.5V to 5.6V (2.6V to 3.6V on MAX657, 659); in high current mode, it is 10V to 15V.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX654, MAX656, MAX657

(GND = 0V, V_{BATT} = 1.2V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V _{OUT}	MAX654, MAX656 T _A = T _{MIN} to T _{MAX}	4.5	5.0	5.5	V
		MAX657 T _A = T _{MIN} to T _{MAX}	2.7	3.0	3.3	
Output Current	I _L		See Table 1			mA
Minimum Input Voltage to LX1	V _{LX1}	I _L = 0μA		0.9	1.0	V
Minimum Startup Voltage to LX1	V _{LX1}	I _L = 0μA		1.1	1.15	V
Input Voltage to LX2	V _{LX2}				5.6	V
Peak LX2 Switch Current	I _{LX2}	MAX654, MAX657			1.5	A
Standby Current	I _Q	I _L = 0μA, CTL = Open		80		μA
Switching Frequency	f ₀	V _{BATT} = 1.0V to 1.6V	15.5	18	24	kHz
		T _A = T _{MIN} to T _{MAX}		18		
LX2, D Switch Duty Cycle	%ON	MAX654, MAX656	66	75	80	%
		MAX657	50	66	75	
LX2, D Switch On Time	t _{ON}	MAX654, MAX656	30	42	46	μs
		MAX657	23	37	44	
LX2 On Resistance	R _{DS(ON)}	MAX654, MAX657	0.40		0.67	Ω
D Output Saturation Current		MAX656 Source Sink		-25 100		mA
Low Battery Input Threshold Voltage	V _{LBI}		1.12		1.18	V
Low Battery Input Threshold Tempco				-0.5		mV/°C
Low Battery Input Bias Current	I _{LBI}			0.01	10	nA
Low Battery Output	V _{LBO}	V _{LBI} < 1.12V, I _{LBO} = 1.6mA V _{LBO} > 1.18V, I _{LBO} = -1μA	V ₊ - 1		0.4	V
CTL Input Threshold	V _{CTL}			0.7		V
PR Output	V _{PR}	PR High, I _{PR} = -1μA PR Low, I _{PR} = 1mA		V _{OUT} - 0.2 0.3		V

Low Voltage Step-Up DC-DC Converters

MAX654-659

ELECTRICAL CHARACTERISTICS: MAX655, MAX658, MAX659

(GND = 0V, VBATT = 2.4V, TA = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	VOUT	MAX655, MAX658	TA = TMIN to TMAX	4.5	5.0	5.5	V
		MAX659	TA = TMIN to TMAX	2.7	3.0	3.3	
Output Current	IL			See Table 1			mA
Minimum Input Voltage to LX1	VLX1	IL = 0μA			0.9	1.0	V
Minimum Startup Voltage to LX1	VLX1	IL = 0μA			1.0	1.5	V
Input Voltage to LX2	VLX2					5.6	V
Peak LX2 Switch Current	ILX2					1.5	A
Standby Current	IQ	IL = 0μA, CTL = Open			40		μA
Switching Frequency	f0	VBATT = 2.0V to 3.2V		15.5	18	24	kHz
		TA = TMIN to TMAX			18		
LX2, D Switch Duty Cycle	%ON	MAX655, MAX658		40	50	60	%
		MAX659		25	33	37	
LX2, D Switch On Time	tON	MAX655, MAX658		18	28	35	μs
		MAX659		12	18	22	
LX2 On Resistance	RDS(ON)			0.40		0.67	Ω
D Output Saturation Current		MAX658	Source Sink		-25 100		mA
Low Battery Input Threshold Voltage	VLBI			1.12		1.18	V
Low Battery Input Threshold Tempco					-0.5		mV/°C
Low Battery Input Bias Current	ILBI				0.01	10	nA
Low Battery Output	VLBO	VLBI < 1.12V, ILBO = 1.6mA VLBI > 1.18V, ILBO = -1μA		V+ -1		0.4	V
CTL Input Threshold	VCTL				0.7		V
PR Output	VPR	PR High, IPR = -1μA PR Low, IPR = 1mA			VOUT - 0.2 0.3		V

Operating Principle

The MAX654-659 are step-up converters; energy from a battery is first stored in a coil and then discharged to the load. Essentially, the circuit consists of a battery in series with a coil (L2) and switch (LX2), along with a rectifier (D1) and filter capacitor (C1) as shown in Figure 1. When the switch is closed, current builds up in the coil, creating a magnetic field. Next, the switch opens, the magnetic field collapses, and the voltage across the inductor reverses polarity. This voltage adds to that of the battery and supplies current to the load via the rectifier.

The switch is controlled by a constant frequency oscillator whose output is gated on and off by a comparator that monitors the output voltage. When VOUT rises above the comparator threshold, the MOSFET at LX2 is held off.

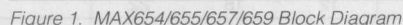
The key to operating CMOS circuitry from a 1V supply depends on a technique called bootstrapping. A specially designed oscillator starts itself up on a very low

voltage and builds up (or bootstraps) a higher voltage that in turn is used as the supply for further operation. The bootstrapped supply yields higher efficiency because it can drive the gate of the internal FET transistors to lower on resistances.

When power is first applied, the circuit is very inefficient for the first cycle until a higher voltage is generated on the flyback half of the cycle. This higher voltage is rectified and filtered and powers the entire IC (and thus the oscillator) for the next cycle. Since each cycle generates a higher voltage for the next cycle, the voltage builds up very rapidly. An internal regulator limits the voltage to about 12V. The load for this supply is only the CMOS chip itself, so the requirements for the external inductor, L1, are not demanding. The +12V supply is brought out to the V+ pin and is connected to a tantalum capacitor for filtering.

The bootstrapped 12V drives an internal N-channel power FET that furnishes the switching power for the load.

MAX654-659



feedback. The MAX654-659 thus have two separate switching circuits and use two separate inductors.

A typical application circuit is shown in Figure 3. The higher value inductor, L1, is typically 4.7mH, and may

MAX656 MAX658 PIN #	MAX654 MAX655 MAX657 MAX659 PIN #	NAME	FUNCTION
–	1	LX2	Output (drain) of high-power N-channel power MOS switch.
1	3	V _{CC}	Connect to positive battery terminal.
2	2	V+	Output of low power-up converter; 10V to 15V in high-power mode, 4.5V to 5.6V in MAX654/655/656/658 standby mode, 2.6V to 3.6V in MAX657/59 standby mode.
3, 7	7	GND	Low-Power Ground.
4	4	V _{REF}	1.25V bandgap reference output; should be decoupled with a capacitor to pin 3. This terminal is high impedance and cannot source or sink current.
5	5	LBO	Low Battery Monitor Output. Sinks 1.6mA when LBI is less than 1.17V, otherwise sources 1μA from V+.

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MAXIM

Low Voltage Step-Up DC-DC Converters

MAX654-659

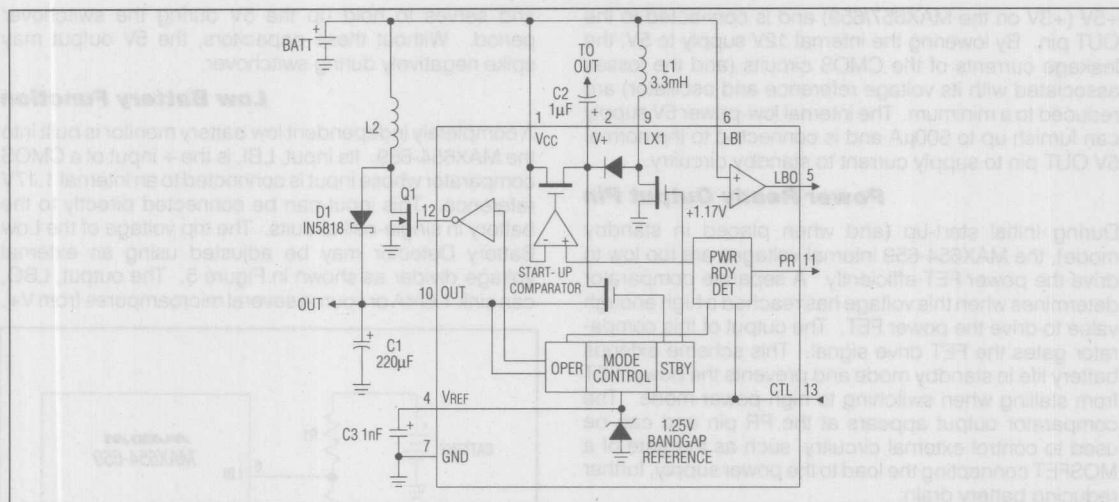


Figure 2. MAX656/658 Block Diagram

have fairly high losses. It is used for the low-power section of the circuit and is rectified by an internal diode and routed to V+, where it is filtered by an external capacitor, C1. The second inductor, L2, ranges from 12µH to 500µH, depending on input voltage and load current. It must have low series resistance and have sufficient core material to handle the load power without saturating. With the MAX654/5/7/8, the inductor, L2, is connected to LX2, which is simply the drain of the high-power FET. Current flowing through L2 is rectified by an external Schottky diode, D1, and filtered by an external capacitor, C2. This is the main +5V output (+3V on the

MAX657/659). It is connected to the OUT pin which is the feedback input in high-power mode. Figure 4 shows a similar circuit with the MAX656 using an external FET for higher power output.

Low-Power Standby Mode

A control pin (CTL) puts the device into standby mode to conserve power. When this pin is held low, the IC operates normally. But if it is driven high or left open, the chip goes into standby. Several things happen in standby mode: the PR pin is driven low, the high-power FET is gated off, the 12V (V+) switching supply is reduced to

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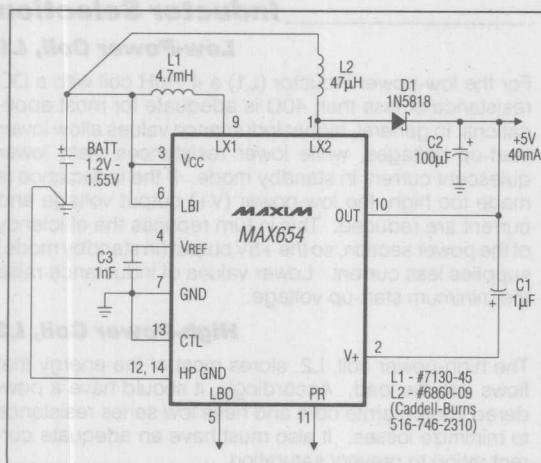


Figure 3. MAX654 Typical Application

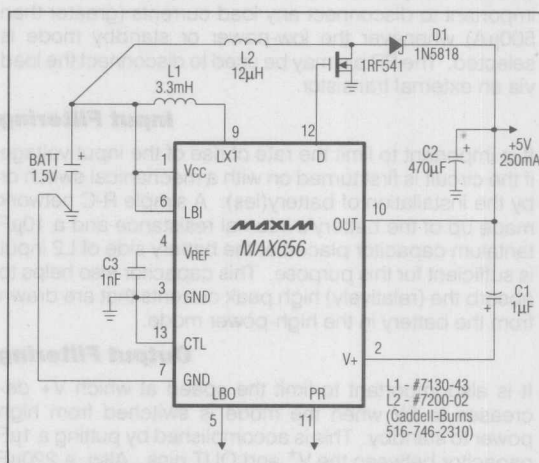


Figure 4. MAX656 Typical Application

Low Voltage Step-Up DC-DC Converters

+5V (+3V on the MAX657/659) and is connected to the OUT pin. By lowering the internal 12V supply to 5V, the leakage currents of the CMOS circuits (and the losses associated with its voltage reference and oscillator) are reduced to a minimum. The internal low-power 5V supply can furnish up to 500 μ A and is connected to the normal 5V OUT pin to supply current to standby circuitry.

Power Ready Output Pin

During initial start-up (and when placed in standby mode), the MAX654-659 internal voltages are too low to drive the power FET efficiently. A separate comparator determines when this voltage has reached a high enough value to drive the power FET. The output of this comparator gates the FET drive signal. This scheme extends battery life in standby mode and prevents the power FET from stalling when switching to high-power mode. The comparator output appears at the PR pin and can be used to control external circuitry, such as the gate of a MOSFET connecting the load to the power supply, further reducing battery drain.

Start-Up and Mode Considerations

The MAX654-659 may be started up in either low-power (standby) or high-power mode. When starting in the high-power mode, both the low-power switch and the high-power switch start immediately. Whether or not the load is connected, the output voltage will rise to 5V in the first few cycles. Note that in the high-power mode, the OUT pin is used as a feedback input.

If a high-power load (greater than about 500 μ A) is connected to the OUT pin and the device is placed in the low-power mode via the CTL pin, the low-power oscillator will have to furnish all of the 5V power via the OUT pin, and the low-power oscillator will stall. Therefore, it is important to disconnect any load currents (greater than 500 μ A) whenever the low-power or standby mode is selected. The PR pin may be used to disconnect the load via an external transistor.

Input Filtering

It is important to limit the rate of rise of the input voltage if the circuit is first turned on with a mechanical switch or by the installation of battery(ies). A simple R-C network made up of the battery's internal resistance and a 10 μ F tantalum capacitor placed at the battery side of L2 input is sufficient for this purpose. This capacitor also helps to absorb the (relatively) high peak currents that are drawn from the battery in the high-power mode.

Output Filtering

It is also important to limit the speed at which V+ decreases to 5V when the mode is switched from high power to standby. This is accomplished by putting a 1 μ F capacitor between the V+ and OUT pins. Also, a 220 μ F capacitor placed on the OUT pin provides both filtering

and serves to hold up the 5V during the switchover period. Without these capacitors, the 5V output may spike negatively during switchover.

Low Battery Function

A completely independent low battery monitor is built into the MAX654-659. Its input, LBI, is the + input of a CMOS comparator whose input is connected to an internal 1.17V reference. This input can be connected directly to the battery in single-cell circuits. The trip voltage of the Low Battery Detector may be adjusted using an external voltage divider as shown in Figure 5. The output, LBO, can sink 1.6mA or source several microamperes from V+.

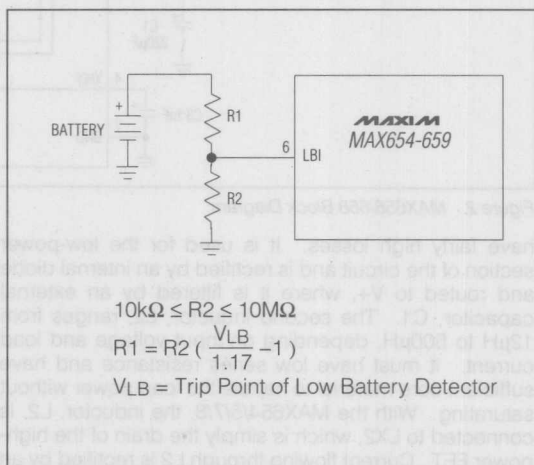


Figure 5. Setting Low Battery Detector Trip Point

Inductor Selection

Low-Power Coil, L1

For the low-power inductor (L1) a 4.7mH coil with a DC resistance of less than 40 Ω is adequate for most applications. In general, higher inductance values allow lower start-up voltages, while lower resistances yield lower quiescent current in standby mode. If the inductance is made too high, the low-power (V+) output voltage and current are reduced. This in turn reduces the efficiency of the power section, so the +5V output (in standby mode) supplies less current. Lower values of inductance raise the minimum start-up voltage.

High-Power Coil, L2

The high-power coil, L2, stores most of the energy that flows into the load. Accordingly, it should have a powdered iron or ferrite core and have low series resistance to minimize losses. It also must have an adequate current rating to prevent saturation.

Low Voltage Step-Up DC-DC Converters

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A coil must be selected that keeps the peak current at LX2 below the maximum rating of the switch. This maximum is 1.5A for the MAX654/55/57/59 and depends on the current rating of the external FET and inductor when using the MAX656/58. The optimum inductance can be found using Figures 6-11 (refer to the Output Current vs. Input Voltage Section), or inductance values may be approximated from Table 1, or finally, the inductance may be calculated as follows:

The first step is to calculate the minimum permissible inductance that keeps the peak current below the current rating of the individual components. This is done using the highest expected input voltage ($V_{IN(MAX)}$), the longest on time per cycle for the LX2 switch ($t_{ON(MAX)}$), and the lowest total series resistance, R_{MIN} , where R_{MIN} is the sum of the minimum coil and FET resistances. These are the conditions under which the highest coil current flows.

For the MAX654, from the Electrical Characteristics table:

I_{pk} of LX2 = 1.5A
 $R_{DS(ON)(MIN)}$ = 0.4 Ω
 $f_0(MIN)$ = 15,500Hz
 duty cycle maximum, %ON(MAX) = 0.8
 $t_{ON(MAX)}$ = 46 μ s

Assume that the minimum coil resistance, $R_{COIL(MIN)}$ is:

$$R_{COIL(MIN)} = 0.1\Omega$$

The minimum total resistance, $R(MIN)$ is:

$$R(MIN) = R_{DS(ON)(MIN)} + R_{COIL(MIN)} = 0.4 + 0.1 = 0.5\Omega$$

Then:

$$I_{pk} = 1.5A = \frac{V_{IN(MIN)}}{R(MIN)} \times [1 - e^{-R(MIN) t_{ON(MAX)} / L(MIN)}]$$

or:

$$L(MIN) = \frac{-R(MIN) t_{ON(MAX)}}{\ln[1 - R(MIN) I_{pk} / V_{IN(MAX)}]}$$

The above two equations "blow up" if $R(MIN) = 0$, but work fine for $R(MIN) \geq 0.001\Omega$. For a maximum input voltage of 1.56V (single alkaline cell) and a minimum coil resistance of 0.1 Ω , the minimum permissible inductance for the MAX654/57 is 35.1 μ H.

Having determined the minimum inductance that keeps the peak current below the individual component ratings, we next calculate a new peak current (I'_{pk}) using the highest resistance ($R(MAX)$) and the lowest input voltage ($V_{IN(MIN)}$). Using these parameters, we will calculate the minimum available output (DC) current.

From the Electrical Characteristics table:

$R_{DS(ON)(MAX)}$ = 0.67 Ω
 $f_0(MAX)$ = 24,000Hz
 duty cycle minimum, %ON(MIN) = 0.66
 $t_{ON(MIN)}$ = 30 μ s

The inductance tolerance of L2 has some impact on these calculations. In the following equations, a new $L(MIN)$ based on the manufacturer's tolerance specification is used. This example assumes $\pm 10\%$ tolerance, so 90% of the nominal inductance is used.

Assume that the maximum coil resistance, $R_{COIL(MAX)}$ is:

$$R_{COIL(MAX)} = 0.15\Omega$$

The maximum total charging resistance, $R(MAX)$ is:

$$R(MAX) = R_{DS(ON)(MAX)} + R_{COIL(MAX)} = 0.82\Omega$$

At the end of the ON period:

$$I'_{pk} = \frac{V_{IN(MIN)}}{R(MAX)} \times [1 - e^{-R(MAX) t_{ON(MIN)} / L(MIN)}]$$

The energy stored in the in the coil is:

$$E_{COIL} = \frac{L(MIN) \times I'_{pk}^2}{2}$$

And the power put into the coil is:

$$P_{COIL} = f_0(MAX) \times E_{COIL} \\ = \frac{L(MIN) \times I'_{pk}^2 \times f_0(MAX)}{2}$$

The minimum available DC output current, I_{OUT} , is:

$$I_{OUT} = \frac{P_{LOAD}}{V_{LOAD}} = \frac{P_{COIL} - P_{LOSS}}{V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)}} \\ = \frac{P_{COIL} - I'_{pk}^2 \times R_{COIL(MAX)} / 3 \times (1 - \%ON(MIN))}{V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)}}$$

Using a $47 \pm 10\%$ μ H coil with a resistance of 0.15 Ω and an input voltage of 1.1V, the minimum available 5V output current at the highest output voltage (5.5V) would be 36.3mA. This assumes a 0.3V forward drop in the IN5818 diode.

When selecting a coil, care should be exercised to insure that the minimum inductance value, including all the manufacturing tolerances, is never lower than the calculated inductance. Otherwise, the peak current rating of LX2 may be exceeded. In addition, the current rating of the coil should be greater than the peak current used in the calculation (1.5A normally) to avoid saturating the core.

If the worst case output current is too small, either the minimum input voltage must be increased or the maximum input voltage should be decreased. It is always desirable to decrease the ratio between maximum and

Table 1. Operation with Common Batteries

MAXIM PART #	BATTERY TYPE	BATTERY VOLTAGE		OUTPUT		COIL SPECIFICATIONS (L2)		
		MIN	MAX			μH^*	OHMS	PART #
MAX654	1 NiCad	1.15V	1.35V	5V	43mA	39	0.05	6860-08
MAX654	1 Alkaline	1.2V	1.55V	5V	43mA	47	0.05	6860-09
MAX654*	1 Alkaline	1.2V	1.55V	5V	10mA	120	0.14	6860-14
MAX655	2 NiCads	2.3V	2.7V	5V	64mA	68	0.07	6860-11
MAX655	2 Alkalines	2.4V	3.1V	5V	62mA	82	0.07	6860-12
MAX655	1 Lithium	2.6V	3.6V	5V	64mA	100	0.10	6860-13
MAX656**	1 NiCad	1.15V	1.35V	5V	250mA	12	0.025	6860-02
MAX656**	1 Alkaline	1.2V	1.55V	5V	275mA	12	0.01	7200-02
MAX657	1 Alkaline	1.2V	1.55V	3V	60mA	39	0.05	6860-08

* Coils are from Caddell-Burns Co. NY (516) 746-2310. Inductance (μH) is the MINIMUM allowed for the listed battery voltage range (Battery Voltage: MIN, MAX). Lower values are not recommended, except when using the MAX656/658 converters since they use an external MOSFET. If less current than listed in the Output column is needed, a higher inductance coil will reduce losses. The optimum inductance varies inversely with required output current if all other conditions are unchanged. For example, refer to line 3 and the 10mA output. 120 μH supplies this current more efficiently than the 39 μH coil of line 2. L2 may also be calculated using the equations in the Inductor Selection Section.

** These MAX656 circuits (see Figure 4) use an IRF541 as an external current switch. Peak switch current is typically 3.5A.

minimum input voltages. The coil resistance also has a significant effect on the output current. So, selecting a coil with the lower resistance will increase the output current and increase the overall efficiency.

If no satisfactory value of inductance can be found for the desired output current, the MAX656/58 may be used with an external FET whose current rating exceeds 1.5A. The calculations are similar for the MAX654, except the external FET's $R_{\text{DS(on)}}$ and the current rating of the FET or coil (whichever is lower) should be substituted in the above equations.

If the worst case output current is significantly higher than the required load current, a higher inductance value should be used. This will tend to reduce the peak current and ripple voltage, and tend to raise the overall efficiency. Be sure to adjust the coil resistance and recalculate all values when using another coil.

When the maximum battery voltage exceeds 1.65V, the MAX655/58/59 should be used. Calculations are identical to the MAX654 calculations, except different values must be used for the duty cycle and t_{ON} .

In general, if a choice of batteries is available, higher input voltages are preferred for two reasons. First, as the input voltage approaches 1V, the load on the battery increases while the losses increase. The losses become so dominant that efficiency suffers, and little output current can be maintained. Second, certain losses, such as the coil resistance and the FET on resistance, are less significant with higher input voltages. This means higher efficiency and a greater range of input voltages are tolerable. This in turn means that more of the chemical energy can be converted into electricity.

The inductance values for commonly encountered battery-operated power supplies are tabulated in Table 1.

Capacitor Selection

The high-current, fast rise-time pulses associated with switching power supplies demand good grounding and bypassing techniques. The MAX654/55/57/59 have 3 ground pins to improve grounding. In addition, the internal voltage reference is brought out for connection to an external 1nF capacitor, minimizing noise and modulation of the reference.

In order to minimize transients, the two output voltages, V_+ and +5V, should be filtered with tantalum capacitors or other types of capacitors with low effective series resistance. If aluminum electrolytic capacitors are used, they should be paralleled with 0.1 μF disc ceramic capacitors.

Rectifier Selection

The MAX654-659 use one external rectifier. To achieve specified performance at low voltages, a Schottky type, such as the 1N5818, is recommended because it combines low forward voltage drop with fast switching speed. This maximizes power conversion efficiency and output current when the DC-DC converter is in high-power mode. One drawback of Schottky rectifiers is relatively high reverse leakage current (at 5V reverse, 1N5818 leakage is typically 60 μA at 25°C and 450 μA at 75°C), which is quite large with respect to the circuit's quiescent current in standby mode (typical standby current MAX654/56/57: 80 μA , MAX655/58/59: 40 μA). If standby mode is not used or used only for short periods, reverse leakage is not a significant additional loss compared to the normal load current, and need not be considered.

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If quiescent operating current is a primary concern, or if the MAX654-659 spends most of its time in standby mode, a silicon rectifier such as the 1N4933 or Unitrode UES1001 may be preferred. Silicon rectifiers have less reverse leakage current than do Schottky rectifiers (1N4933 leakage current is typically $1\mu\text{A}$ at 25°C and $50\mu\text{A}$ at 100°C). In circuits where the standby mode is the predominant mode of operation, battery life may be extended by trading conversion efficiency for lower standby quiescent current.

Output Current vs. Input Voltage

Figures 6 through 11 show output current versus input voltage using typical inductor values for each part in the MAX654-659 Family. Where curves end in the middle of the graphs, the peak current limit of the internal LX2 switch has been reached. A higher input voltage than indicated by that line (for the given inductor) may damage the device. Figures 8 and 10 assume that an IRF541 MOSFET is used (0.085Ω maximum on resistance).

Dashed lines indicate regions where the LX2 current limit hasn't been exceeded, but the current rating of the selected coil (Caddell-Burns 6860 series) has. The actual voltages where lines end or become dashed are indicated by arrows on the graphs. The output currents indicated by dashed lines can be achieved only with inductors of higher current rating than the indicated coil (such as Caddell-Burns 7200 series or a toroid, for example). The coils used in Figures 6, 7, 9, and 11 are as follows:

33 μH - 6860-07	Caddell-Burns
47 μH - 6860-09	(516) 746-2310
100 μH - 6860-13	
150 μH - 6860-15	
220 μH - 6860-17	

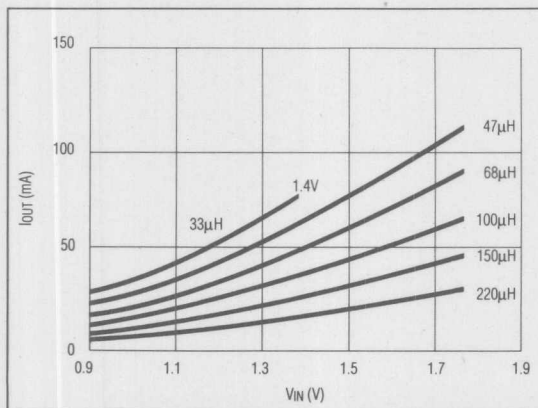


Figure 6. MAX654, I_{OUT} vs. V_{IN} ($V_{OUT} = 5\text{V}$)

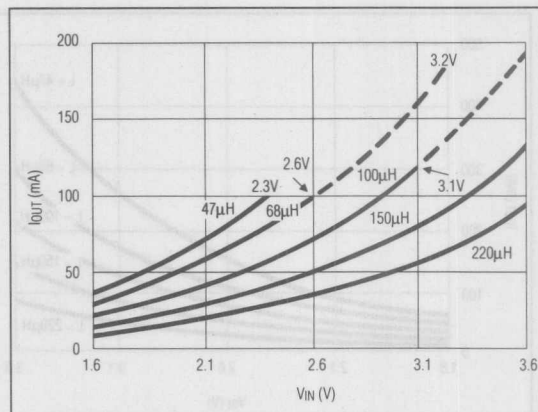


Figure 7. MAX655, I_{OUT} vs. V_{IN} ($V_{OUT} = 5\text{V}$)

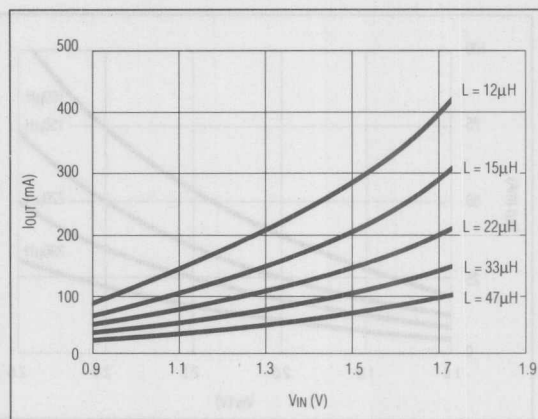


Figure 8. MAX656, I_{OUT} vs. V_{IN} ($V_{OUT} = 5\text{V}$)

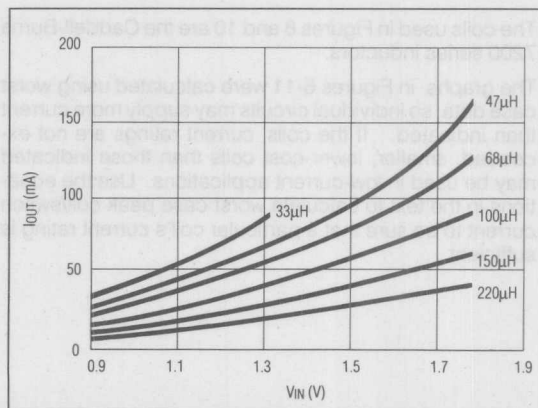


Figure 9. MAX657, I_{OUT} vs. V_{IN} ($V_{OUT} = 3\text{V}$)

Low Voltage Step-Up DC-DC Converters

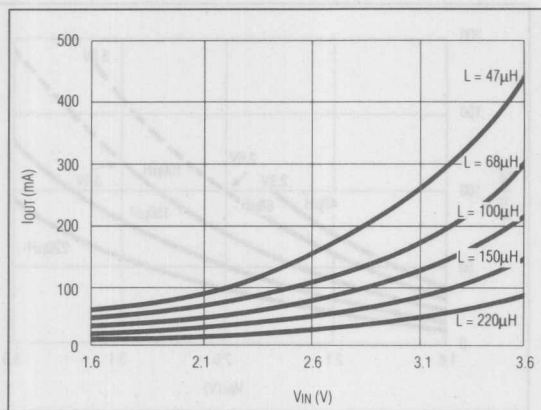


Figure 10. MAX658, I_{OUT} vs. V_{IN} ($V_{OUT} = 5V$)

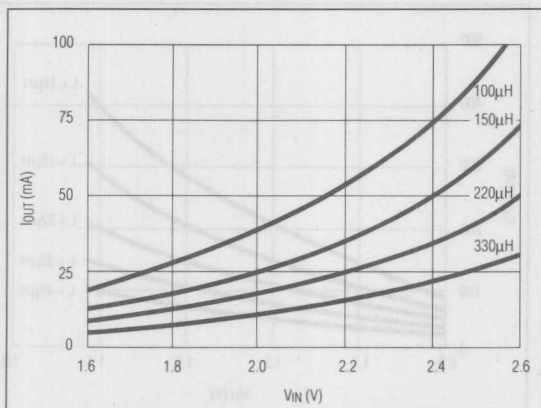


Figure 11. MAX659, I_{OUT} vs. V_{IN} ($V_{OUT} = 3V$)

The coils used in Figures 8 and 10 are the Caddell-Burns 7200 series inductors.

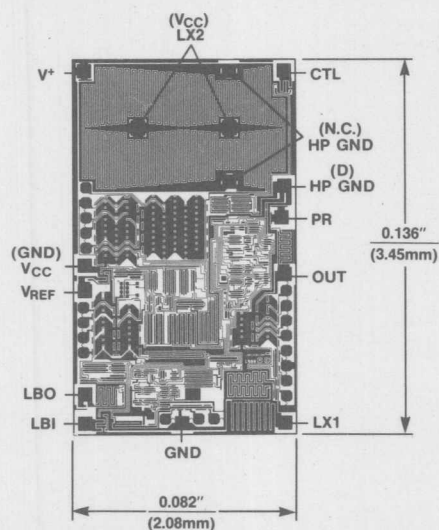
The graphs in Figures 6-11 were calculated using worst case data, so individual circuits may supply more current than indicated. If the coils' current ratings are not exceeded, smaller, lower-cost coils than those indicated may be used in low-current applications. Use the equations in the text to calculate worst case peak coil/switch current to be sure that a particular coil's current rating is sufficient.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX656CPD	0°C to +70°C	14 Plastic DIP
MAX656CSD	0°C to +70°C	14 Narrow SO
MAX656C/D	0°C to +70°C	Dice
MAX656EPD	-40°C to +85°C	14 Plastic DIP
MAX656ESD	-40°C to +85°C	14 Narrow SO
MAX656MJD	-55°C to +125°C	14 CERDIP
MAX657CPD	0°C to +70°C	14 Plastic DIP
MAX657CSD	0°C to +70°C	14 Narrow SO
MAX657C/D	0°C to +70°C	Dice
MAX657EPD	-40°C to +85°C	14 Plastic DIP
MAX657ESD	-40°C to +85°C	14 Narrow SO
MAX657MJD	-55°C to +125°C	14 CERDIP
MAX658CPD	0°C to +70°C	14 Plastic DIP
MAX658CSD	0°C to +70°C	14 Narrow SO
MAX658C/D	0°C to +70°C	Dice
MAX658EPD	-40°C to +85°C	14 Plastic DIP
MAX658ESD	-40°C to +85°C	14 Narrow SO
MAX658MJD	-55°C to +125°C	14 CERDIP
MAX659CPD	0°C to +70°C	14 Plastic DIP
MAX659CSD	0°C to +70°C	14 Narrow SO
MAX659C/D	0°C to +70°C	Dice
MAX659EPD	-40°C to +85°C	14 Plastic DIP
MAX659ESD	-40°C to +85°C	14 Narrow SO
MAX659MJD	-55°C to +125°C	14 CERDIP

Low Voltage Step-Up DC-DC Converters

Chip Topography



Note: Labels in () are for MAX656/MAX658 only

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Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

5-57

MAXIM

Dual Mode™ 5V/Programmable Micropower Voltage Regulators

General Description

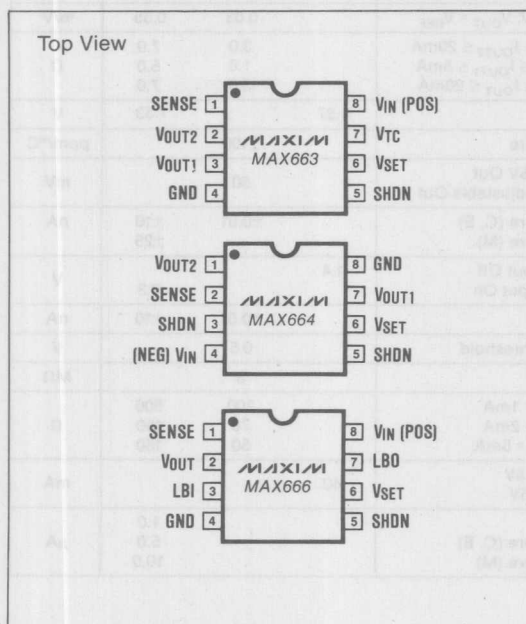
The MAX663/664/666 CMOS voltage regulators have a maximum quiescent current of $12\mu\text{A}$. They can be used either as 5 volt, fixed output regulators with no additional components, or can be adjusted from 1.3V to 16V using two external resistors. Fixed or adjustable operation is automatically selected via the V_{SET} input. The MAX66X series, ideally suited for battery powered systems, has an input voltage range of 2 to 16.5V, an output current capability of 40mA, and can operate with low input-output differentials. Other features include current limiting and low power shut down.

The MAX663 positive regulator and MAX664 negative regulator are both pin and electrically compatible with the ICL7663 and ICL7664 and can plug-in replace these devices, improving performance and eliminating the need for external resistors in 5V applications. The MAX666 has a positive output and includes on-chip low-battery detection circuitry.

Applications

Handheld Instruments
LCD Display Systems
Pagers
Remote Data Acquisition and Telemetry
Radio Controlled Devices
Long-life Battery Powered Systems

Pin Configuration



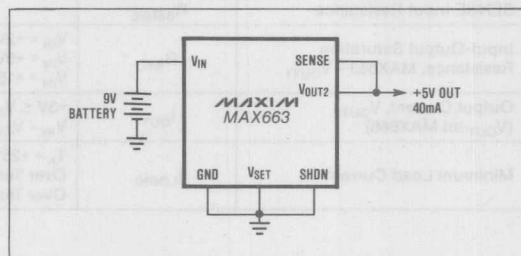
Features

- ◆ Dual Mode Operation: Fixed +5V or Adjustable from +1.3V to +16V
- ◆ Low Power CMOS: $12\mu\text{A}$ Max Quiescent Current
- ◆ 40mA Output Current, with Current Limiting
- ◆ Pin-Compatible Upgrade of ICL7663 and ICL7664
- ◆ +2V to +16.5V Operating Range
- ◆ Low Battery Detector (MAX666)
- ◆ No Output Over-Shoot on Power Up

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX663C/D	0°C to +70°C	Dice
MAX663CPA	0°C to +70°C	8 Lead Plastic DIP
MAX663CSA	0°C to +70°C	8 Lead Small Outline
MAX663EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX663ESA	-40°C to +85°C	8 Lead Small Outline
MAX663EJA	-40°C to +85°C	8 Lead Cerdip
MAX663MJA	-55°C to +125°C	8 Lead Cerdip
MAX664C/D	0°C to +70°C	Dice
MAX664CPA	0°C to +70°C	8 Lead Plastic DIP
MAX664CSA	0°C to +70°C	8 Lead Small Outline
MAX664EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX664ESA	-40°C to +85°C	8 Lead Small Outline
MAX664EJA	-40°C to +85°C	8 Lead Cerdip
MAX664MJA	-55°C to +125°C	8 Lead Cerdip
MAX666C/D	0°C to +70°C	Dice
MAX666CPA	0°C to +70°C	8 Lead Plastic DIP
MAX666CSA	0°C to +70°C	8 Lead Small Outline
MAX666EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX666ESA	-40°C to +85°C	8 Lead Small Outline
MAX666EJA	-40°C to +85°C	8 Lead Cerdip
MAX666MJA	-55°C to +125°C	8 Lead Cerdip

Typical Operating Circuit



Dual Mode 5V/Programmable Micropower Voltage Regulators

ABSOLUTE MAXIMUM RATINGS

MAX663 and MAX666

Input Supply Voltage	+18V
Terminal Voltage	
Pins 1,3,5,6, MAX663 — Pin 7, and MAX666 — Pin 2,	GND -0.3V to $V_{IN} + 0.3V$
MAX663 — Pin 2	GND -0.3V to $V_{OUT1} + 0.3V$
MAX666 — Pin 7	GND -0.3V to +16.5V
Output Source Current	
MAX663,666 — Pin 2 (V_{OUT2} , V_{OUT})	50mA
MAX663 — Pin 3 (V_{OUT1})	25mA
Output Sink Current, Pin 7	-20mA

MAX664

Input Supply Voltage	-18V
Terminal Voltage	
Pins 1,3,5,6,7	$V_{IN} - 0.3V$ to GND +0.3V
Pin 2	$V_{IN} - 0.3V$ to $V_{OUT1} + 0.3V$
Output Sink Current, (Pins 1,7)	-25mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, MAX663 AND MAX666

($V_{IN} = +9V$, $V_{OUT} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	Over Temperature (C) Over Temperature (E, M)	2.0 2.2		16.5	V
Quiescent Current	I_Q	No Load, $V_{IN} = +16.5V$ $T_A = +25^\circ C$ Over Temperature (C) Over Temperature (E, M)		6 12 15 20		μA
Output Voltage	V_{OUT}	$V_{SET} = GND$ Over Temperature (C, E) Over Temperature (M)	4.75 4.5	5.0 5.0	5.25 5.5	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	$+2V \leq V_{IN} \leq +15V$, $V_{OUT} = V_{REF}$		0.03	0.35	%/V
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	MAX663: $1mA \leq I_{OUT2} \leq 20mA$ MAX663: $50\mu A \leq I_{OUT1} \leq 5mA$ MAX666: $1mA \leq I_{OUT} \leq 20mA$		3.0 1.0 3.0	7.0 5.0 7.0	Ω
Reference Voltage	V_{SET}	$V_{OUT} = V_{SET}$	1.27		1.33	V
Reference Tempco.	$\Delta V_{SET} / \Delta T$	Over Temperature		± 100		ppm/ $^\circ C$
V_{SET} Internal Threshold for Fixed +5V or Adjustable Output	$V_{F/A}$	$V_{SET} < V_{F/A}$ for +5V Out $V_{SET} > V_{F/A}$ for Adjustable Out		50		mV
V_{SET} Input Current	I_{SET}	Over Temperature (C, E) Over Temperature (M)		± 0.01	± 10 ± 25	nA
Shutdown Input Voltage	V_{SHDN}	$V_{SHDN} HI =$ Output Off $V_{SHDN} LO =$ Output On	1.4		0.3	V
Shutdown Input Current	I_{SHDN}			± 0.01	± 10	nA
SENSE Input Threshold	$V_{OUT} - V_{SENSE}$	Current Limit Threshold		0.5		V
SENSE Input Resistance	R_{SENSE}			3		M Ω
Input-Output Saturation Resistance, MAX663 - V_{OUT1}	R_{SAT}	$V_{IN} = +2V$, $I_{OUT} = 1mA$ $V_{IN} = +9V$, $I_{OUT} = 2mA$ $V_{IN} = +15V$, $I_{OUT} = 5mA$		200 70 50	500 150 150	Ω
Output Current, V_{OUT2} (V_{OUT} on MAX666)	I_{OUT}	$+3V \leq V_{IN} \leq +16.5V$ $V_{IN} - V_{OUT} = +1.5V$	40			mA
Minimum Load Current	$I_{L(MIN)}$	$T_A = +25^\circ C$ Over Temperature (C, E) Over Temperature (M)			1.0 5.0 10.0	μA

ALL DEVICES

Power Dissipation	
Plastic DIP (Derate 8.3mW/ $^\circ C$ above $+50^\circ C$)	625mW
Small Outline (Derate 6mW/ $^\circ C$ above $+50^\circ C$)	450mW
CERDIP (Derate 8mW/ $^\circ C$ above $+50^\circ C$)	800mW
Operating Temperature Range	
MAX66XC	$0^\circ C$ to $+70^\circ C$
MAX66XE	$-40^\circ C$ to $+85^\circ C$
MAX66XM	$-55^\circ C$ to $+125^\circ C$
Storage Temperature	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering 10 seconds)	$+300^\circ C$

Dual Mode 5V/Programmable Micropower Voltage Regulators

ELECTRICAL CHARACTERISTICS, MAX663 AND MAX666 (continued)

($V_{IN} = +9V$, $V_{OUT} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LBI Input Threshold	V_{LBI}	MAX666	1.21	1.28	1.37	V
LBI Input Current	I_{LBI}	MAX666		± 0.01	± 10	nA
LBO Output Saturation Resistance	R_{SAT}	MAX666, $I_{SAT} = 2mA$		35	100	Ω
LBO Output Leakage Current		MAX666, $LBI = +1.4V$		10		nA
V_{TC} Open-Circuit Voltage (Note 1)	V_{TC}	MAX663		0.9		V
V_{TC} Sink Current (Note 1)	I_{TC}	MAX663		8.0	2.0	mA
V_{TC} Temperature Coefficient (Note 1)		MAX663		+2.5		mV/ $^\circ C$

Note 1: This output (MAX663 only) has a positive temperature coefficient. Using it in conjunction with the input of the regulator at V_{SET} , a negative coefficient results in the output voltage. The V_{TC} pin will not source current.

ELECTRICAL CHARACTERISTICS, MAX664

($V_{IN} = -9V$, $V_{OUT} = -5V$, $T_A = +25^\circ C$, unless otherwise noted.)

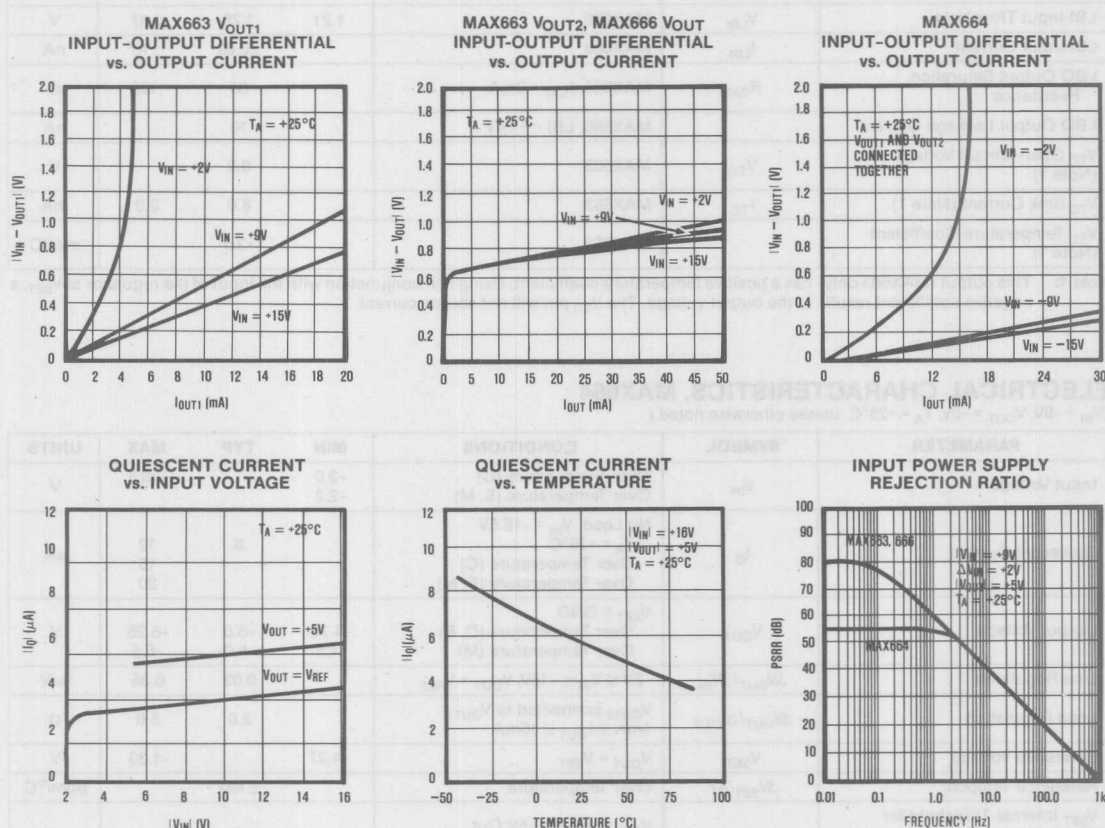
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	Over Temperature (C) Over Temperature (E, M)	-2.0 -2.2		-16.5	V
Quiescent Current	I_Q	No Load, $V_{IN} = -16.5V$ $T_A = +25^\circ C$ Over Temperature (C) Over Temperature (E, M)		6	12 15 20	μA
Output Voltage	V_{OUT}	$V_{SET} = GND$ Over Temperature (C, E) Over Temperature (M)	-4.75 -4.5	-5.0 -5.0	-5.25 -5.5	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	$-2V \leq V_{IN} \leq -15V$, $V_{OUT} = V_{REF}$		0.03	0.35	%/V
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	V_{OUT2} connected to V_{OUT1} , $1mA \leq I_{OUT} \leq 15mA$		2.0	5.0	Ω
Reference Voltage	V_{SET}	$V_{OUT} = V_{SET}$	-1.27		-1.33	V
Reference Tempco.	$\Delta V_{SET} / \Delta T$	Over Temperature		± 100		ppm/ $^\circ C$
V_{SET} Internal Threshold for Fixed -5V or Adjustable Output Operation	$V_{F/A}$	$V_{SET} < V_{F/A}$ for -5V Out, $V_{SET} > V_{F/A}$ for Variable Out		-50		mV
V_{SET} Input Current	I_{SET}	Over Temperature (C, E) Over Temperature (M)		± 0.01	± 10 ± 25	nA
Shutdown Input Voltage	V_{SHDN}	$V_{SHDN} HI =$ Output Off $V_{SHDN} LO =$ Output On	-1.4		-0.3	V
Shutdown Input Current	I_{SHDN}			± 0.01	± 10	nA
SENSE Input Threshold	$V_{OUT} - V_{SENSE}$	Current Limit Threshold		-0.6		V
SENSE Input Resistance	R_{SENSE}			3		M Ω
Input-Output Saturation Resistance	R_{SAT}	V_{OUT2} connected to V_{OUT1} $V_{IN} = -2V$, $I_{OUT} = -1mA$ $V_{IN} = -9V$, $I_{OUT} = -2mA$ $V_{IN} = -15V$, $I_{OUT} = -5mA$		150 40 30	500 80 60	Ω
Minimum Load Current	$I_{L(MIN)}$	$T_A = +25^\circ C$ Over Temperature (C, E) Over Temperature (M)			-1.0 -5.0 -10.0	μA

MAX663/664/666

5

Dual Mode 5V/Programmable Micropower Voltage Regulators

Typical Operating Characteristics



Pin Description

NAME	FUNCTION (See text for details)
$V_{OUT(1)(2)}$	Regulator Output(s)
V_{IN}	Regulator Input
SENSE	Current limit sense input
LBI	Low battery detection input
LBO	Low battery detection output
SHUTDOWN	Disables output for minimum power consumption
V_{SET}	Ground this pin for 5V output or Connect to external resistive divider for adjustable output
V_{TC}	Temperature-proportional voltage for negative TC output

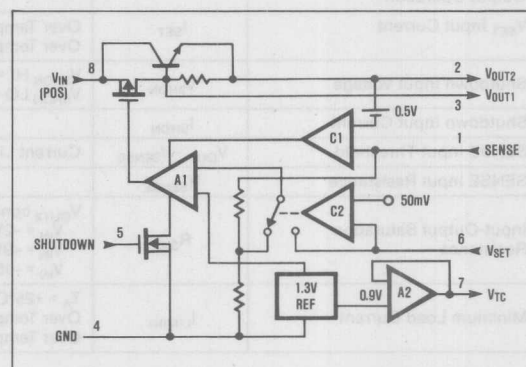


Figure 1. MAX663 Positive Regulator, Block Diagram

Dual Mode 5V/Programmable Micropower Voltage Regulators

MAX663/664/666

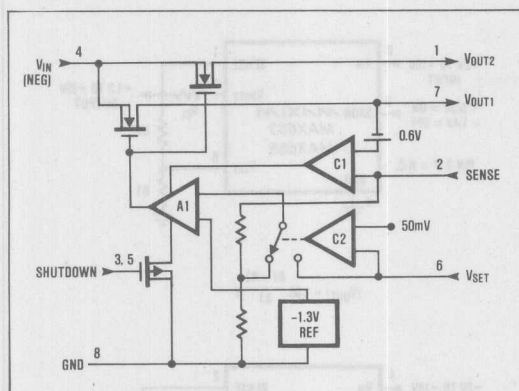


Figure 2. MAX664 Negative Regulator, Block Diagram

Detailed Description

As shown in the block diagrams for each device (Figures 1, 2, and 3), the main elements of the MAX66X family of regulators are a micropower bandgap reference, an error amplifier, and one or two series pass output devices. A P-channel FET and an NPN transistor are used on the MAX663, two N-channel FETs are used in the MAX664, and one NPN output transistor is used in the MAX666. All regulators also contain two comparators, one for current limiting (C1) and another which selects fixed 5V or adjustable output operation (C2).

The bandgap reference, which is trimmed to 1.30V \pm 30mV, is internally connected to one input of the error amplifier, A1. The feedback signal from the regulator output is supplied to the A1's other input by either an on-chip voltage divider or by two external resistors. When VSET is grounded the internal divider provides the error amplifier's feedback signal for a fixed 5V output. When VSET is more than 50mV above ground (below ground for the MAX664) the error amplifier's input is switched directly to the VSET pin and external resistors set the output voltage.

Comparator C1 monitors the output current via the SENSE input and shuts down the regulator's output(s) by disabling A1. An external current sense resistor, RCL, sets the limit value. The MAX663 and MAX666 current-limit when the voltage on RCL exceeds 0.5V. The MAX664 current limits at 0.6V.

The MAX663 has an additional amplifier, A2, which provides a temperature-proportional output, VTC. When this is summed into the inverting input of the error amplifier, a negative temperature coefficient results at the output. This is useful when powering liquid crystal displays over wide temperature ranges.

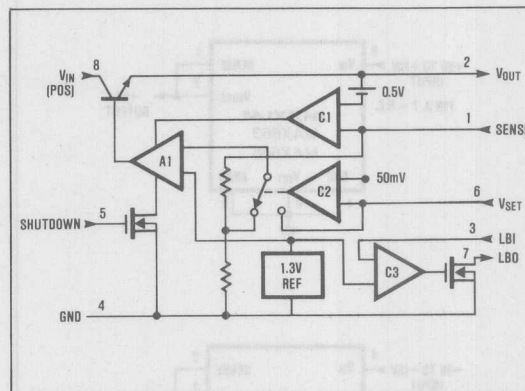


Figure 3. MAX666 Positive Regulator With Low Battery Detector, Block Diagram

The MAX666 has a third comparator, C3, which compares the LBI input to the internal 1.30V reference. The Low Battery Output, LBO, is an open drain FET connected to Ground. The Low Battery threshold can also be set with a voltage divider at LBI. In addition, all devices also have a SHUTDOWN input which disables the error amplifier and regulator output(s).

Basic Circuit Operation

Figure 4 shows the connections for fixed 5V output positive and negative regulators. The VSET input is grounded and no external resistors are required. Figure 5 shows adjustable output operation with current limiting. The output voltage is set by R1 and R2 and the current limit threshold is set by RCL. VOUT should be connected to SENSE if current limiting is not used and the SHUTDOWN input should be grounded if not used.

Output Voltage Selection

If VSET is not connected to Ground, the output voltage is set by the equation:

$$V_{OUT} = V_{SET} \times \frac{R1 + R2}{R1}, \text{ where } V_{SET} = 1.30V$$

or, to simplify resistor selection:

$$R2 = R1 \times \left(\frac{V_{OUT}}{1.30V} - 1 \right)$$

Since the input bias current at VSET has a maximum value of 10nA, relatively large values can be used for R1 and R2 with no loss of accuracy. 1M Ω is a typical value for R1. The tolerance on VSET is guaranteed to be less than \pm 30mV. This allows the output to be preset without trim pots, using only fixed resistors in most cases.

Dual Mode 5V/Programmable Micropower Voltage Regulators

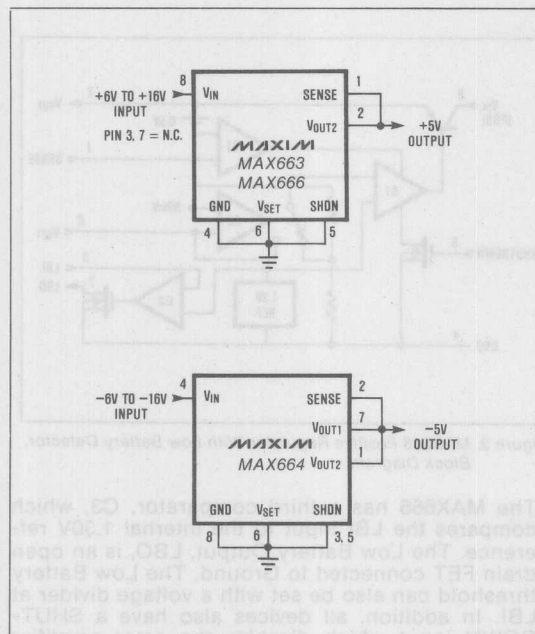


Figure 4. Connections for Fixed 5V Output

Current Limiting

Internal current limiting is activated on all MAX66X devices when the voltage difference between V_{OUT} and the SENSE input exceeds an internal threshold. The limit value is externally set by R_{CL} using the equation:

$$R_{CL} = \frac{V_{CL}}{I_{CL}} \quad \begin{array}{l} V_{CL} = 0.5V \text{ for MAX663 and MAX666} \\ V_{CL} = -0.6V \text{ for MAX664} \\ (V_{CL} = V_{OUT} - V_{SENSE}) \end{array}$$

where R_{CL} is the current limit sense resistor and I_{CL} is the maximum current. R_{CL} should be chosen so that neither the 50mA absolute maximum output current specification nor the maximum power dissipation is exceeded.

If current limiting is used, remember that the additional voltage drop across R_{CL} must be considered when determining the regulator's dropout voltage. If current limiting is not used, the SENSE input should be connected to the output(s).

Shutdown Input

The SHUTDOWN input allows the regulator to be turned off with a logic level signal. Since the current drain in shutdown mode is limited to the regulator's quiescent current (12 μ A Max) this is sometimes desirable in applications where very low power consumption is needed. The SHUTDOWN input

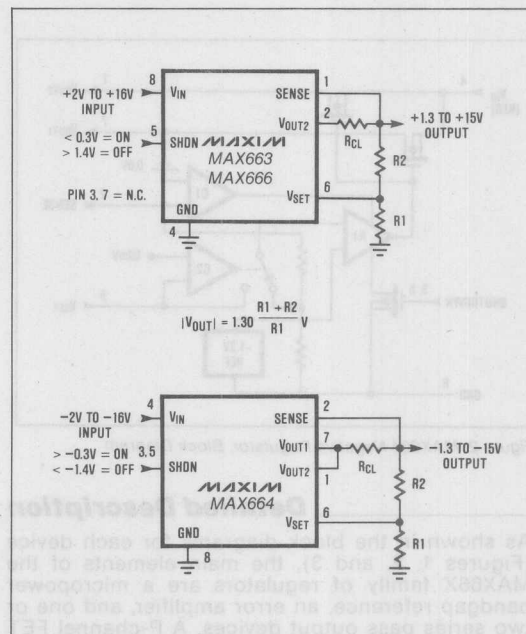


Figure 5. Connections for Adjustable Output

should be driven with a CMOS logic level since the input threshold is only 0.3V (-0.3V on the MAX664). In TTL systems, an open-collector driver with a pullup resistor will work with the MAX663/666 if a small collector current is used to keep the output's V_{SAT} below 0.3V. Collector currents as low as 1 μ A are suitable since the SHUTDOWN pin's input current is less than 10nA. Note that the MAX664's SHUTDOWN input is activated by a negative level. On both positive and negative regulators the SHUTDOWN input should be grounded for normal operation.

Low Battery Detection

The MAX666 contains on-chip circuitry for low battery or low power supply detection. If the voltage at LBI (Low Battery Input, pin 3) falls below the regulator's internal reference (1.30V) then LBO (Low Battery Output, pin 7), an open drain output, goes low. The threshold can be set to any level above the reference voltage by connecting a resistive divider to LBI (Figure 6) based on the equation:

$$R3 = R4 \times \left(\frac{V_{BATT}}{1.30V} - 1 \right)$$

where V_{BATT} is the desired threshold of the Low Battery Detector and R3 and R4 are the LBI input divider resistors. Since LBI's input current is no more than 10nA, then R3 and R4 can have high

Dual Mode 5V/Programmable Micropower Voltage Regulators

MAX663/664/666

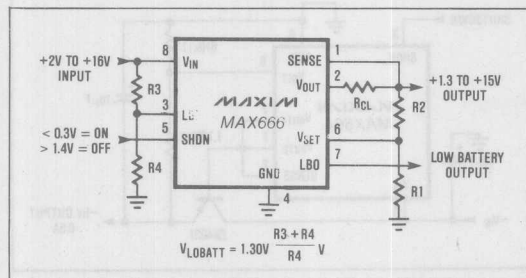


Figure 6. Adjustable Positive Output With Low Battery Detection

values to minimize loading. If, for example, V_{OUT} were 5V, then a 6V low-battery threshold could be set using $10M\Omega$ for R_3 and $2.7M\Omega$ for R_4 . When megohm resistor values are used, special attention should be paid to PC board leakage which can introduce error at the LBI input.

Temperature-Proportional Output

The V_{TC} output (MAX663 only) has a positive temperature coefficient of about $+2.5mV/^{\circ}C$. When connected to the summing junction of the error amplifier (V_{SET}) through a resistor, this positive coefficient results in a controllable negative temperature coefficient at the output of the MAX663. At $25^{\circ}C$ the voltage at the V_{TC} output is typically 0.9V. Figure 7 shows a simplified diagram of the MAX663 and the equations for setting both the output voltage and the tempco when V_{TC} is used. When not used, V_{TC} should be left unconnected.

Negative output temperature coefficients are most commonly used in multiplexed LCD modules or display systems to compensate for the inherent negative tempco of the LCD threshold. Figure 8 shows a MAX663 generating a temperature compensated V_{DISP} for the Maxim ICM7233 triplexed LCD display driver.

Application Hints

Input-Output (Dropout) Voltage

A regulator's minimum input-output differential, or dropout voltage, determines the lowest usable input voltage. In battery powered systems this will determine the useful end-of-life battery voltage. The MAX663 and MAX666 have a dropout voltage of 1V at full output. This means that as 5V regulators, for example, they will provide a regulated 5V output at 40mA as long as the input voltage is 6V or greater.

For low current applications ($I_{OUT} < 5mA$) the MAX663 can operate with input-output differentials below 1V when V_{OUT1} is used. The dropout voltage will then depend on the P-channel output FET's saturation resistance multiplied by the load current (see MAX663 Electrical Specifications, R_{SAT}).

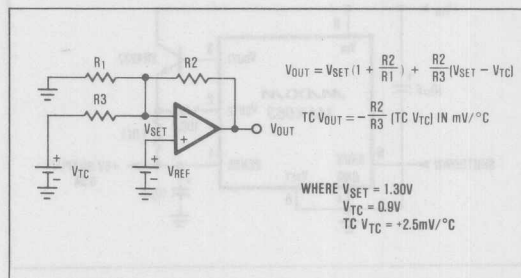


Figure 7. Temperature-Proportional Output Equations, MAX663

The MAX664 (negative output) uses two N-channel FETs as output devices so its dropout voltage is also a function of R_{SAT} times its load current (see Electrical Specifications).

Output Connections

When using V_{OUT1} on the MAX663 for low current, low dropout applications, V_{OUT2} and V_{OUT1} must be connected together since the current limit circuitry is referenced only to V_{OUT2} (Figure 1). V_{OUT2} does not supply load current in this configuration since the base of the NPN output transistor is shorted by the output connection. For high current operation V_{OUT2} should be used alone and V_{OUT1} should be left unconnected. V_{OUT1} is not provided on the MAX666. On the MAX664, V_{OUT1} and V_{OUT2} should always be connected together for proper operation and lowest dropout voltage.

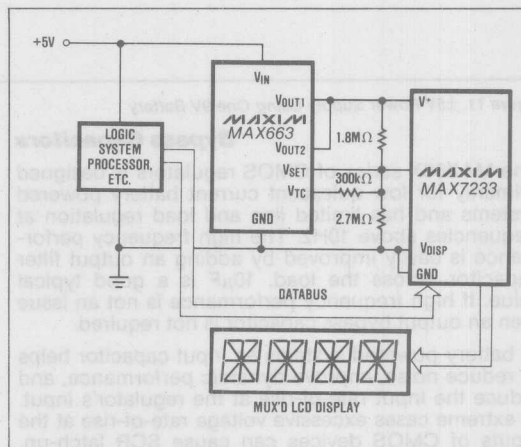
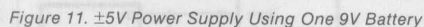
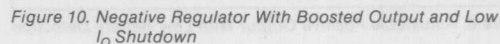
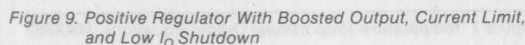


Figure 8. Driving a Multiplexed LCD Display. Consistent operation over more than $40^{\circ}C$ temperature span, as opposed to about $10^{\circ}C$ with fixed drive voltage, is allowed by negative temperature coefficient drive voltage to the displays. Based on EPSON LDB-728 Display or equivalent.

MAX663/664/666



Chip Topography

In battery powered systems an input capacitor helps to reduce noise, improve dynamic performance, and reduce the input rate-of-rise at the regulator's input. In extreme cases excessive voltage rate-of-rise at the inputs of CMOS devices can cause SCR latch-up. The low impedance of Ni-Cad and Lead-Acid batteries make this possible when they are switched directly to the regulator input with no current limiting resistance, inductance, or input filtering. The addition of a $0.1\mu\text{F}$ or greater input capacitor limits the input rate-of-rise to a safe level.

(See Pin Configurations (front page) for pin functions)

+5V/Programmable Low-Dropout Voltage Regulator

MAX667

General Description

The MAX667 low-dropout, positive-series linear regulator supplies up to 250mA of output current while maintaining a maximum quiescent current of 25 μ A. At 100mA of output current, the input/output voltage differential is typically 0.3V. Other features include a low voltage detector to indicate power failure, as well as, early warning and low-dropout detectors to indicate an imminent loss of output voltage regulation. A system shutdown control disables the output and puts the circuit into a low quiescent-current mode.

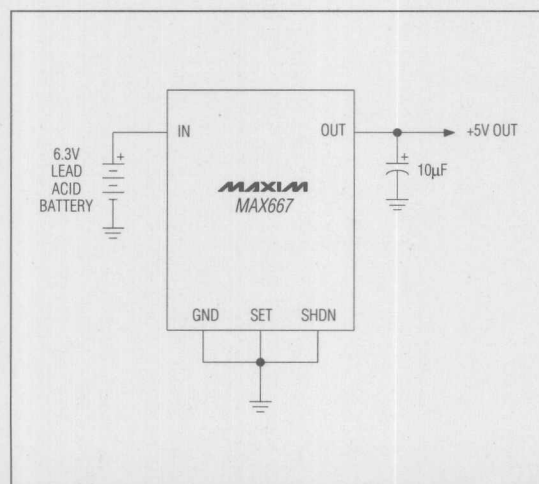
The MAX667 has a dual mode of operation. In one mode, an output of 5V is available using the internally trimmed feedback resistors. The output may also be varied from 1.3V to 15V by connecting 2 external resistors.

The MAX667 is pin and electrically compatible with the MAX666. The MAX667 should be chosen when high output currents and/or low-dropout voltages are desired.

Applications

Battery-Powered Devices
 Pagers and Radio Control Receivers
 Portable Instruments
 Solar-Powered Instruments

Typical Operating Circuit



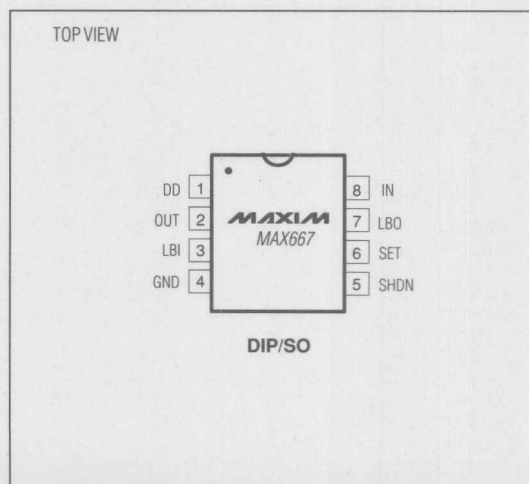
Features

- ◆ 0.3V Typ Dropout at 100mA
- ◆ 250mA Max Output Current
- ◆ Normal Mode: 12 μ A Quiescent Current
- ◆ Shutdown Mode: 3 μ A Quiescent Current
- ◆ Low Battery Detector
- ◆ Fixed 5V (Min Component Count) or Variable Output
- ◆ 3.5V to 16V Input
- ◆ Dropout Detector Output

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX667CPA	0°C to +70°C	8 Plastic DIP
MAX667CSA	0°C to +70°C	8 Narrow SO
MAX667C/D	0°C to +70°C	Dice
MAX667EPA	-40°C to +85°C	8 Plastic DIP
MAX667ESA	-40°C to +85°C	8 Narrow SO
MAX667MJA	-55°C to +125°C	8 CERDIP

Pin Configuration



General Description

The MAX680/MAX681 are monolithic CMOS dual charge pump voltage converters that provide $\pm 10V$ outputs from a +5V input voltage. The MAX680/MAX681 provide both a positive stepup charge pump to develop +10V from +5V input and an inverting charge pump to generate the -10V output. Both parts have an on-chip 8kHz oscillator. The MAX681 has the capacitors internal to the package, and the MAX680 requires 4 external capacitors to produce both positive and negative voltages from a single supply.

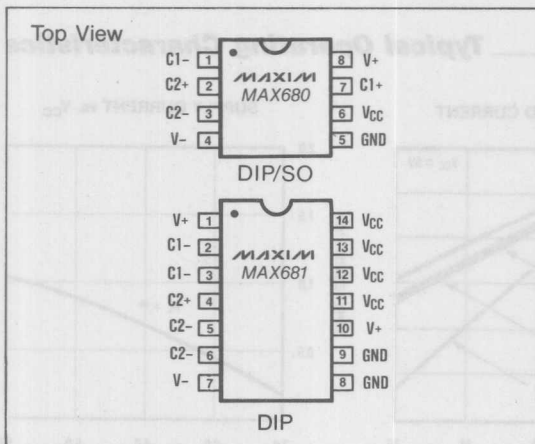
The output source impedances are typically 150 Ω , providing useful output currents up to 10mA. The low quiescent current and high efficiency make this device suitable for a variety of applications that need both positive and negative voltages generated from a single supply.

Applications

The MAX680/MAX681 can be used wherever a single positive supply is available and positive and negative voltages are required. Common applications include the generation of $\pm 6V$ from a 3V battery and generation of $\pm 10V$ from the standard +5V logic supply for use with analog circuitry. Typical applications include:

- $\pm 10V$ from +5V Logic Supply
- $\pm 6V$ from a 3V Lithium Cell
- Handheld Instruments
- Battery Operated Equipment
- Data Acquisition Systems
- Panel Meters
- Operational Amplifier Power Supplies

Pin Configurations



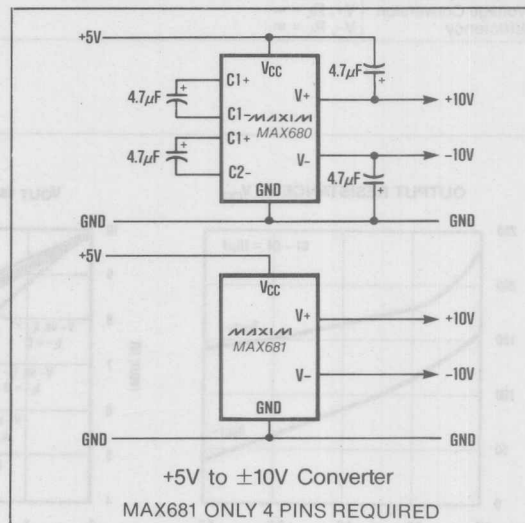
Features

- ◆ 95% Voltage Conversion Efficiency
- ◆ 85% Power Conversion Efficiency
- ◆ Wide Voltage Range: +2.0V to +6.0V
- ◆ Only 4 External Capacitors Required — MAX680
- ◆ No Capacitors Required — MAX681
- ◆ 500 μA Supply Current
- ◆ Monolithic CMOS Design

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX680CPA	0°C to +70°C	8 Plastic DIP
MAX680CSA	0°C to +70°C	8 Narrow SO
MAX680C/D	0°C to +70°C	Dice
MAX680EPA	-40°C to +85°C	8 Plastic DIP
MAX680ESA	-40°C to +85°C	8 Narrow SO
MAX680EJA	-40°C to +85°C	8 Cerdip
MAX680MJA	-55°C to +125°C	8 Cerdip
MAX681CPD	0°C to +70°C	14 Plastic DIP
MAX681BCPD	0°C to +70°C	14 Plastic DIP
MAX681EPD	-40°C to +85°C	14 Plastic DIP

Typical Operating Circuit



+5V to ±10V Voltage Converters

ABSOLUTE MAXIMUM RATINGS

V_{CC}	+6.2V
$V+$	+12V
$V-$	-12V
$V-$ Short-Circuit Duration	Continuous
$V+$ Current	75mA
V_{CC} dV/dT	1V/ μ s

Power Dissipation	
Plastic DIP (derate 8.33mW/°C above +50°C)	625mW
Small Outline (derate 6mW/°C above +50°C)	450mW
CERDIP (derate 8mW/°C above +50°C)	800mW
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

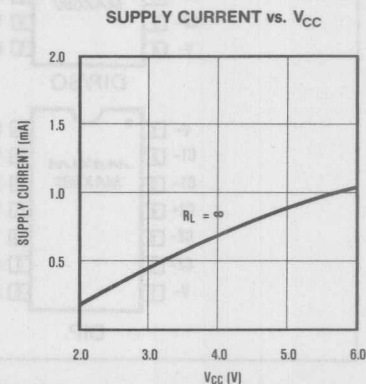
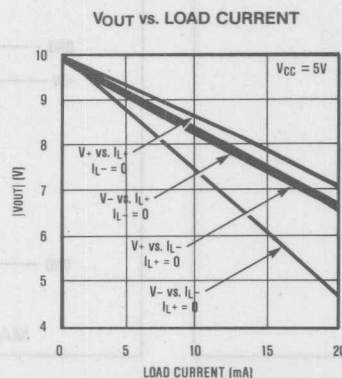
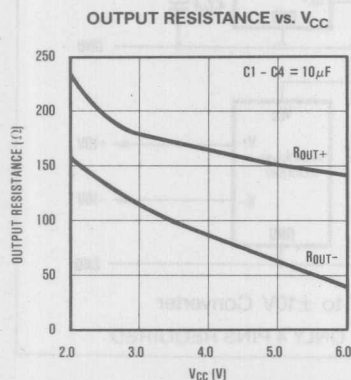
Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V$, $T_A = +25^\circ C$, test circuit Figure 1, unless otherwise noted.)

PARAMETER	CONDITIONS	MAX680/MAX681			MAX681B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	$V_{CC} = 3V$, $T_A = +25^\circ C$, $R_L = \infty$		0.5	1		0.5	1	mA
	$V_{CC} = 5V$, $T_A = +25^\circ C$, $R_L = \infty$		1	2		1	2	
	$V_{CC} = 5V$, $0^\circ C \leq T_A \leq +70^\circ C$, $R_L = \infty$			2.5			2.5	
	$V_{CC} = 5V$, $-40^\circ C \leq T_A \leq +85^\circ C$, $R_L = \infty$			3				
	$V_{CC} = 5V$, $-55^\circ C \leq T_A \leq +125^\circ C$, $R_L = \infty$			3				
Supply Voltage Range	$MIN. \leq T_A \leq MAX.$, $R_L = 10k\Omega$	2.0	1.5 to 6.0	6.0	2.0	1.5 to 6.0	6.0	V
Positive Charge Pump Output Source Resistance	$I_{L+} = 10mA$, $I_{L-} = 0mA$, $V_{CC} = 5V$, $T_A = +25^\circ C$ $I_{L+} = 5mA$, $I_{L-} = 0mA$, $V_{CC} = 2.8V$, $T_A = +25^\circ C$ $I_{L+} = 10mA$, $I_{L-} = 0mA$, $V_{CC} = 5V$		150 180	250 300		150 180	250 300	Ω
Negative Charge Pump Output Source Resistance	$0^\circ C \leq T_A \leq +70^\circ C$			325		380	600	
	$-40^\circ C \leq T_A \leq +85^\circ C$			350				
	$-55^\circ C \leq T_A \leq +125^\circ C$			400				
	$I_{L-} = 10mA$, $I_{L+} = 0mA$, $V+ = 10V$, $T_A = +25^\circ C$ $I_{L-} = 5mA$, $I_{L+} = 0mA$, $V+ = 5.6V$, $T_A = +25^\circ C$ $I_{L-} = 10mA$, $I_{L+} = 0mA$, $V+ = 10V$		90 110	150 175		175 180	300 325	
Oscillator Frequency	$0^\circ C \leq T_A \leq +70^\circ C$ $-40^\circ C \leq T_A \leq +85^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$			200 200 250		300	500	
Power Efficiency	$R_L = 10k\Omega$		85			85		%
Voltage Conversion Efficiency	$V+$, $R_L = \infty$ $V-$, $R_L = \infty$	95 90	99 97		95 90	99 97		

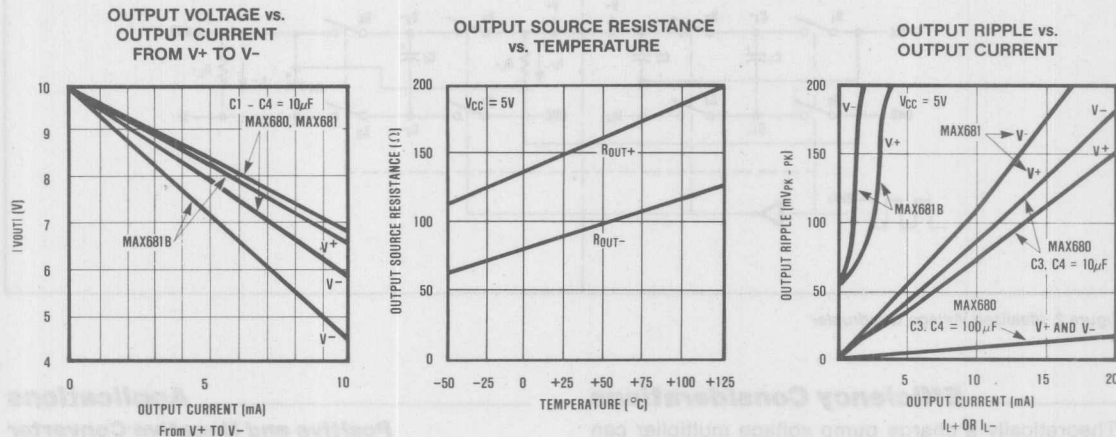
Typical Operating Characteristics



+5V to $\pm 10V$ Voltage Converters

Typical Operating Characteristics

MAX680/MAX681



Detailed Description

All circuitry needed to implement a dual charge pump is contained in the MAX681. Only four capacitors are needed on the MAX680. These may be inexpensive electrolytic capacitors with values in the range of $1\mu F$ to $100\mu F$. The MAX681B contains $1\mu F$ capacitor and exhibits somewhat more output ripple than the MAX681. See Typical Operating Characteristics.

Figure 2A illustrates the idealized operation of the positive voltage converter. The on-chip oscillator generates a 50% duty cycle clock signal. During the first half of the cycle, switches S2 and S4 are open, switches S1 and S3 are closed, and the capacitor C1 is charged to the input voltage V_{CC} . During the second half cycle, switches S1 and S3 are open, S2 and S4 are closed, and the capacitor C1 is translated upward by V_{CC} volts. Assuming ideal switches and no load on C3, charge is transferred onto C3 from C1 such that the voltage on C3 will be $2V_{CC}$, generating the positive supply.

Figure 2B illustrates the negative converter. The switches of the negative converter are out of phase from the positive converter. During the second half of the clock cycle, S6 and S8 are open, S5 and S7 are closed, thus charging C2 from V^+ (pumped up to

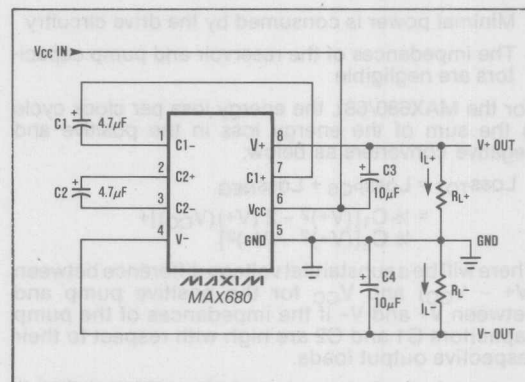


Figure 1. Test Circuit

$2V_{CC}$ by the positive charge pump) to GND. In the first half of the clock cycle, S5 and S7 are open, S6 and S8 are closed, and the charge on C2 is transferred to C4, generating the negative supply. The eight switches are CMOS power MOSFETs. Switches S1, S2, S4 and S5 are P-channel devices while switches S3, S6, S7, and S8 are N-channel devices.

+5V to ±10V Voltage Converters

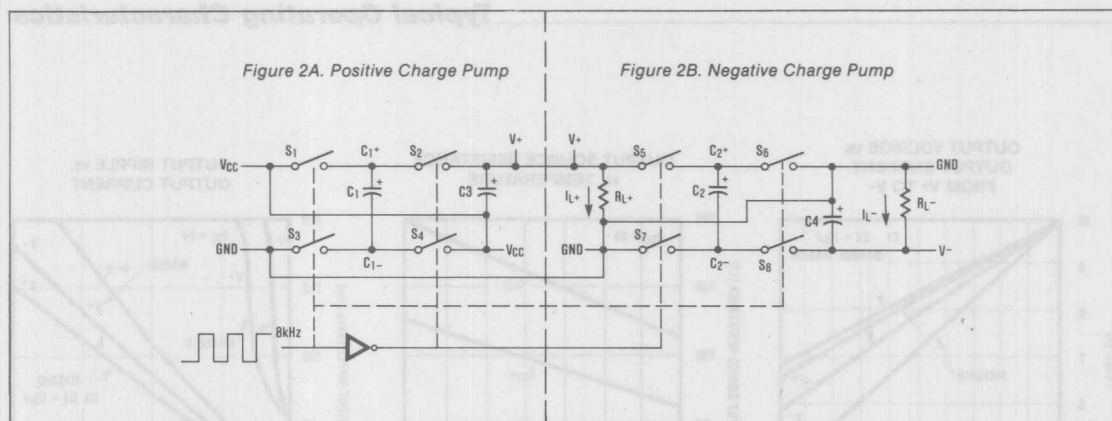


Figure 2. Idealized Voltage Quadrupler

Efficiency Considerations

Theoretically a charge pump voltage multiplier can approach 100% efficiency under the following conditions:

- The charge pump switches have virtually no offset and extremely low on resistance
- Minimal power is consumed by the drive circuitry
- The impedances of the reservoir and pump capacitors are negligible

For the MAX680/681, the energy loss per clock cycle is the sum of the energy loss in the positive and negative converters as below:

$$\begin{aligned} \text{LOSS}_{\text{TOT}} &= \text{LOSS}_{\text{POS}} + \text{LOSS}_{\text{NEG}} \\ &= \frac{1}{2} C_1 [(V_+)^2 - 2(V_+)(V_{CC})] + \\ &\quad \frac{1}{2} C_2 [(V_+)^2 - (V_-)^2] \end{aligned}$$

There will be a substantial voltage difference between $(V_+ - V_{CC})$ and V_{CC} for the positive pump and between V_+ and V_- if the impedances of the pump capacitors C_1 and C_2 are high with respect to their respective output loads.

Larger values of reservoir capacitors C_3 and C_4 will reduce output ripple. Larger values of both pump and reservoir capacitors improve the efficiency.

Maximum Operating Limits

The MAX680/MAX681 have on-chip zener diodes that clamp V_{CC} to approximately 6.2V, V_+ to 12.4V, and V_- to -12.4V. Never exceed the maximum supply voltage or excessive current may be shunted by these diodes, potentially damaging the chip. The MAX680/MAX681 will operate over the entire operating temperature range with an input voltage of 2V to 6V.

Applications

Positive and Negative Converter

The most common application of the MAX680/MAX681 is as a dual charge pump voltage converter which provides positive and negative outputs of two times a positive input voltage. For applications where PC board space is at a premium, the MAX681 with its capacitors internal to the package offers the smallest footprint. The simple circuit of Figure 3 performs the same function using the MAX680 and external capacitors, C_1 and C_3 for the positive pump and C_2 and C_4 for the negative pump. In most applications, all four capacitors are low-cost 10 μ F or 22 μ F polarized electrolytics. When using the MAX680 for low current applications, 1 μ F may be used for C_1 and C_2 charge pump capacitors, and 4.7 μ F for the reservoir capacitors C_3 and C_4 . Capacitors C_1 and C_3 must be rated at 6V or greater, and capacitors C_2 and C_4 must be rated at 12V or greater.

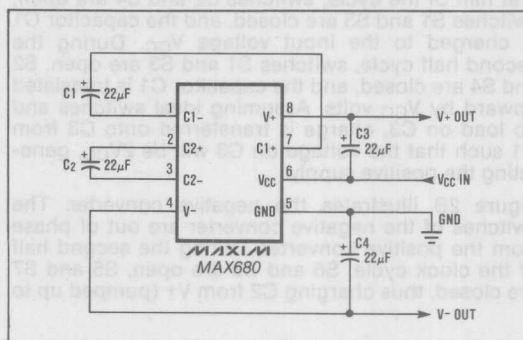


Figure 3. Positive and Negative Converter

+5V to ±10V Voltage Converters

MAX680/MAX681

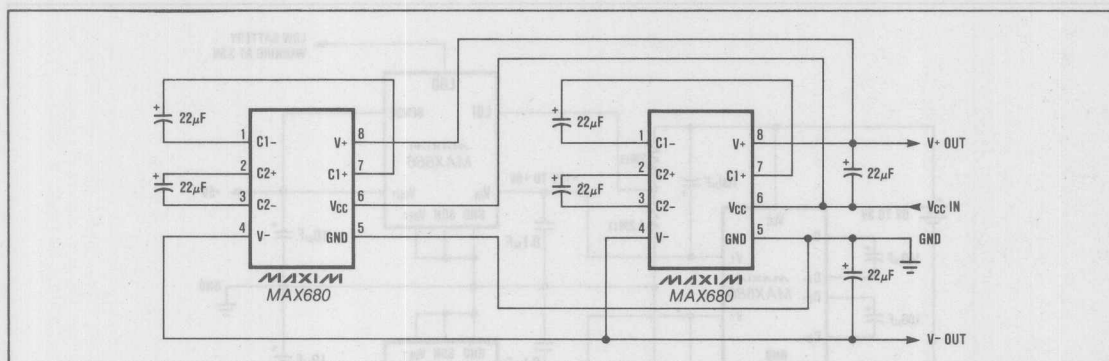


Figure 4. Paralleling MAX680s For Lower Source Resistance

The MAX680/MAX681 are NOT voltage regulators: the output source resistance of either charge pump is approximately 150Ω at room temperature with V_{CC} at 5V. This means that with an input V_{CC} of 5V, under light load $V+$ will approach +10V and $V-$ will be at -10V, but BOTH $V+$ and $V-$ will droop towards GND as the current drawn from EITHER $V+$ or $V-$ increases since the negative converter draws its power from the output of the positive converter. To predict the output voltages, treat the chips as two separate converters and analyze them separately. First, the droop of the negative supply (V_{DROP-}) equals the current drawn from $V-$ (I_{L-}) times the source resistance of the negative converter ($RS-$):

$$V_{DROP-} = I_{L-} \times RS-$$

Likewise, the droop of the positive supply (V_{DROP+}) equals the current drawn from the positive supply (I_{L+}) times the source resistance of the positive converter ($RS+$), except that the current drawn from the positive supply is the sum of the current drawn by the load on the positive supply (I_{L+}) plus the current drawn by the negative converter (I_{L-}):

$$(V_{DROP+}) = I_{L+} \times RS+ = (I_{L+} + I_{L-}) \times RS+$$

The positive output voltage will be:

$$V+ = 2V_{CC} - V_{DROP+}$$

The negative output voltage will be:

$$V- = (V+ - V_{DROP}) = -(2V_{CC} - V_{DROP+} - V_{DROP-})$$

The positive and negative charge pumps are tested and specified separately to provide the separate values of output source resistance for use in the above formulas. When the positive charge pump is tested, the negative charge pump is unloaded. When the negative charge pump is tested, the positive supply $V+$ is from an external source, isolating the negative charge pump.

The ripple voltage on either output can be calculated by noting that the current drawn from the output is supplied by the reservoir capacitor alone during one half cycle of the clock. This results in a ripple of:

$$V_{RIPPLE} = \frac{1}{2} I_{OUT} (1/f_{PUMP}) (1/CR)$$

For the nominal f_{PUMP} of 8kHz with 10µF reservoir capacitors, the ripple will be 30mV with I_{OUT} at 5mA. Remember that in most applications, the I_{OUT} of the positive charge pump is the load current PLUS the current taken by the negative charge pump.

Paralleling Devices

Paralleling multiple MAX680/MAX681s reduces the output resistance of both the positive and negative converters. The effective output resistance is the output resistance of a single device divided by the number of devices. As illustrated in Figure 4, each MAX680 requires separate pump capacitors C1 and C2, but all can share a single set of reservoir capacitors.

±5V Regulated Supplies From A Single 3V Battery

Figure 5 shows a complete ±5V power supply using one 3V battery. The MAX680/MAX681 provide +6V at $V+$, which is regulated to +5V by the MAX666, and -6V, which is regulated to -5V by the MAX664. The

+5V to ±10V Voltage Converters

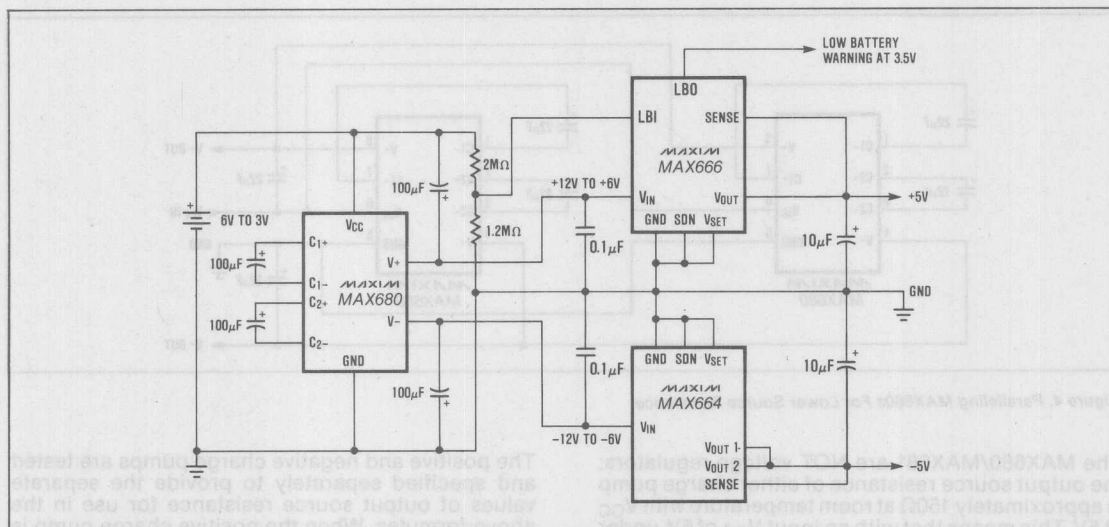


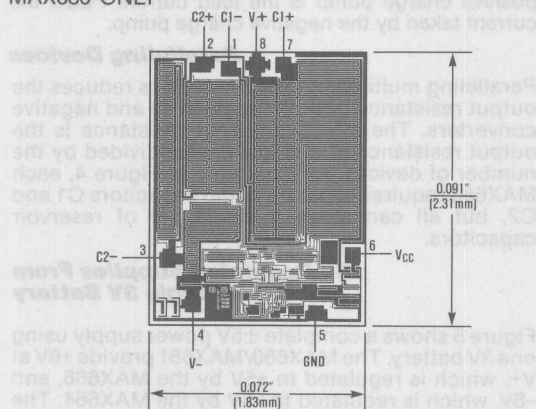
Figure 5. Regulated +5V and -5V From a Single Battery

MAX666 and MAX664 are pre-trimmed at wafer sort and require no external setting resistors, minimizing parts count. The combined quiescent current of the MAX680/MAX681, MAX663, and MAX664 is less than 500µA, while the output current capability is 5mA. The input to the MAX680/MAX681 can vary from 3V to 6V without affecting regulation appreciably. With higher input voltage, more current can be drawn from the outputs of the MAX680/MAX681. With 5V at

V_{CC}, 10mA can be drawn from both regulated outputs simultaneously. Assuming 150Ω source resistance for both converters, with (I_{L+} + I_{L-}) = 20mA, the positive charge pump will droop 3V, providing +7V for the negative charge pump. The negative charge pump will droop another 1.5V due to its 10mA load, leaving -5.5V at V₋ sufficient to maintain regulation for the MAX664 at this current.

Chip Topography

MAX680 ONLY



Note: Connect substrate to V₊.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

Microprocessor Supervisory Circuits

General Description

The MAX690 Family of supervisory circuits reduce the complexity and number of components required for power supply monitoring and battery control functions in microprocessor systems. These include μ P reset and backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The MAX690 Family significantly improves system reliability and accuracy compared to that obtainable with separate ICs or discrete components.

The MAX690, MAX692 and MAX694 are supplied in 8-pin packages and provide four functions:

- 1) A Reset output during power-up, power-down and brownout conditions.
- 2) Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
- 3) A Reset pulse if the optional watchdog timer has not been toggled within a specified time.
- 4) A 1.3V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5V.

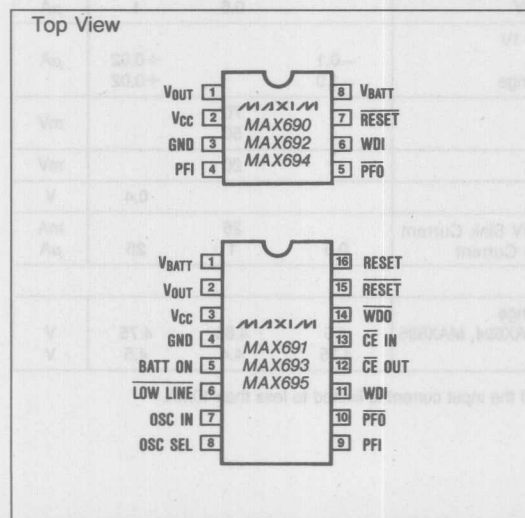
The MAX691, MAX693 and MAX695 are supplied in 16-pin packages and perform all MAX690/692/694 functions, plus:

- 1) Write protection of CMOS RAM or EEPROM.
- 2) Adjustable reset and watchdog timeout periods.
- 3) Separate outputs for indicating a watchdog timeout, backup-battery switchover, and low V_{CC} .

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μ P Power Monitoring

Pin Configuration



Features

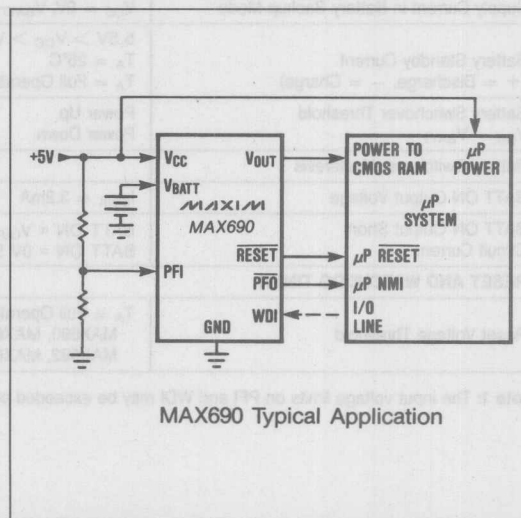
- ◆ Precision Voltage Monitor
4.65V in MAX690, MAX691, MAX694 and MAX695
4.40V in MAX692 and MAX693
- ◆ Power OK/Reset Time Delay – 50, 200ms, or adjustable
- ◆ Watchdog Timer – 100ms, 1.6 sec, or adjustable
- ◆ Minimum Component Count
- ◆ 1 μ A Standby Current
- ◆ Battery Backup Power Switching
- ◆ Onboard Gating of Chip Enable Signals
- ◆ Voltage Monitor for Power Fail or Low Battery Warning

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX690CPA	0°C to +70°C	8 Lead Plastic DIP
MAX690EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX690EJA	-40°C to +85°C	8 Lead Cerdip
MAX690MJA	-55°C to +125°C	8 Lead Cerdip
MAX691C/D	0°C to +70°C	Dice
MAX691CPE	0°C to +70°C	16 Lead Plastic DIP
MAX691CWE	0°C to +70°C	16 Lead Wide SO
MAX691EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX691EJE	-40°C to +85°C	16 Lead Cerdip
MAX691EWE	-40°C to +85°C	16 Lead Wide SO
MAX691MJE	-55°C to +125°C	16 Lead Cerdip

(Ordering information is continued on last page.)

Typical Operating Circuit



MAX690/91/92/93/94/95

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MAXIM

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Maxim Integrated Products 5-75

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)	
V_{CC}	-0.3V to 6.0V
V_{BATT}	-0.3V to 6.0V
All Other Inputs (Note 1) .. -0.3V to ($V_{OUT} + 0.5V$)	
Input Current	
V_{CC}	200mA
V_{BATT}	50mA
GND	20mA
Output Current	
V_{OUT}	short circuit protected
All Other Outputs	20mA
Rate-of-Rise, V_{BATT} , V_{CC}	
Operating Temperature Range	
C suffix	0°C to +70°C
E suffix	-40°C to +85°C
M suffix	-55°C to +125°C

Power Dissipation

8 Pin Plastic DIP	
(Derate 5mW/°C above +70°C)	400mW
8 Pin Cerdip	
(Derate 8mW/°C above +85°C)	500mW
16 Pin Plastic DIP	
(Derate 7mW/°C above +70°C)	600mW
16 Pin Small Outline	
(Derate 7mW/°C above +70°C)	600mW
16 Pin Cerdip	
(Derate 10mW/°C above +85°C)	600mW
Storage Temperature Range	
Lead Temperature (Soldering, 10 seconds)	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full operating range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BATTERY BACKUP SWITCHING					
Operating Voltage Range MAX690, MAX691, MAX694, MAX695 V_{CC} MAX690, MAX691, MAX694, MAX695 V_{BATT} MAX692, MAX693 V_{CC} MAX692, MAX693 V_{BATT}		4.75 2.0 4.5 2.0		5.5 4.25 5.5 4.0	V
V_{OUT} Output Voltage	$I_{OUT} = 1mA$ $I_{OUT} = 50mA$	$V_{CC} - 0.3$ $V_{CC} - 0.5$	$V_{CC} - 0.1$ $V_{CC} - 0.25$		V
V_{OUT} in Battery Backup Mode	$I_{OUT} = 250\mu A$, $V_{CC} < V_{BATT} - 0.2V$	$V_{BATT} - 0.1$	$V_{BATT} - 0.02$		V
Supply Current (excludes I_{OUT})	$I_{OUT} = 1mA$ $I_{OUT} = 50mA$		2 3.5	5 10	mA
Supply Current in Battery Backup Mode	$V_{CC} = 0V$, $V_{BATT} = 2.8V$		0.6	1	μA
Battery Standby Current (+ = Discharge, - = Charge)	$5.5V > V_{CC} > V_{BATT} + 1V$ $T_A = 25^\circ C$ $T_A = \text{Full Operating Range}$	-0.1 -1.0		+0.02 +0.02	μA
Battery Switchover Threshold $V_{CC} - V_{BATT}$	Power Up Power Down		70 50		mV
Battery Switchover Hysteresis			20		mV
BATT ON Output Voltage	$I_{SINK} = 3.2mA$			0.4	V
BATT ON Output Short Circuit Current	BATT ON = $V_{OUT} = 4.5V$ Sink Current BATT ON = 0V Source Current	0.5	25 1	25	mA μA
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold	$T_A = \text{Full Operating Range}$ MAX690, MAX691, MAX694, MAX695 MAX692, MAX693	4.5 4.25	4.65 4.4	4.75 4.5	V V

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

Microprocessor Supervisory Circuits

MAX690/91/92/93/94/95

5

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = full operating range, $V_{BATT} = 2.8V$, $T_A = 25^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Threshold Hysteresis			40		mV
Reset Timeout Delay (MAX690/91/92/93)	Figure 6. OSC SEL HIGH, $V_{CC} = 5V$	35	50	70	ms
Reset Timeout Delay (MAX694/95)	Figure 6. OSC SEL HIGH, $V_{CC} = 5V$	140	200	280	ms
Watchdog Timeout Period, Internal Oscillator	Long Period, $V_{CC} = 5V$	1.0	1.6	2.25	sec
	Short Period, $V_{CC} = 5V$	70	100	140	ms
Watchdog Timeout Period, External Clock	Long Period	3840		4097	Clock
	Short Period	768		1025	Cycles
Minimum WDI Input Pulse Width	$V_{IL} = 0.4$, $V_{IH} = 0.8V_{CC}$	200			ns
RESET and LOW LINE Output Voltage	$I_{SINK} = 1.6mA$, $V_{CC} = 4.25V$ $I_{SOURCE} = 1\mu A$, $V_{CC} = 5V$	3.5		0.4	V
RESET and WDO Output Voltage	$I_{SINK} = 1.6mA$ $I_{SOURCE} = 1\mu A$, $V_{CC} = 5V$	3.5		0.4	V
Output Short Circuit Current	RESET, RESET, WDO, LOW LINE	1	3	25	μA
WDI Input Threshold Logic Low Logic High	$V_{CC} = 5V$ (Note 2)			0.8	V
		3.5			
WDI Input current	$WDI = V_{OUT}$		20	50	μA
	$WDI = 0V$	-50	-15		
POWER FAIL DETECTOR					
PFI Input Threshold	$V_{CC} = +5V$, $T_A = \text{Full}$	1.2	1.3	1.4	V
PFI Input Current			± 0.01	± 25	nA
PFO Output Voltage	$I_{SINK} = 3.2mA$ $I_{SOURCE} = 1\mu A$	3.5		0.4	V
PFO Short Circuit Source Current	PFI = 0V, PFO = 0V	1	3	25	μA
CHIP ENABLE GATING					
CE IN Thresholds	V_{IL}	3.0		0.8	V
	V_{IH}				
CE IN Pullup Current			3		μA
CE OUT Output Voltage	$I_{SINK} = 3.2mA$ $I_{SOURCE} = 3.0mA$ $I_{SOURCE} = 1\mu A$, $V_{CC} = 0V$	$V_{OUT} - 1.5$ $V_{OUT} - 0.05$		0.4	V
CE Propagation Delay	$V_{CC} = 5V$		50	200	ns
OSCILLATOR					
OSC IN Input Current			± 2		μA
OSC SEL Input Pullup Current			5		μA
OSC IN Frequency Range	OSC SEL = 0V	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V $C_{OSC} = 47pF$		4		kHz

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the input current is limited to less than 10mA.

Note 2: WDI is guaranteed to be in the mid-level (inactive) state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 38% of V_{CC} with an impedance of approximately 125 kilohms.

Microprocessor Supervisory Circuits

MAX690/91/92/93/94/95

Pin Description

NAME	PIN		FUNCTION
	MAX690/ 692/694	MAX691/ 693/695	
V _{CC}	2	3	The +5V input.
V _{BATT}	8	1	Backup battery input. Connect to Ground if a backup battery is not used.
V _{OUT}	1	2	The higher of V _{CC} or V _{BATT} is internally switched to V _{OUT} . Connect V _{OUT} to V _{CC} if V _{OUT} and V _{BATT} are not used.
GND	3	4	0V Ground reference for all signals.
RESET	7	15	RESET goes low whenever V _{CC} falls below either the reset voltage threshold or the V _{BATT} input voltage. The reset threshold is typically 4.65V for the MAX690/691/694/695, and 4.4V for the MAX692 and MAX693. RESET remains low for 50ms after V _{CC} returns to 5V, (except 200ms in MAX694/695). RESET also goes low for 50ms if the Watchdog Timer is enabled but not serviced within its timeout period. The RESET pulse width can be adjusted as shown in Table 1.
WDI	6	11	The watchdog input, WDI, is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, RESET pulses low and WDO goes low. The Watchdog Timer is disabled when WDI is left floating or is driven to mid-supply. The timer resets with each transition at the Watchdog Timer Input.
PFI	4	9	PFI is the non-inverting input to the Power Fail Comparator. When PFI is less than 1.3V, PFO goes low. Connect PFI to GND or V _{OUT} when not used. See Figure 1.
PFO	5	10	PFO is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3V. The comparator is turned off and PFO goes low when V _{CC} is below V _{BATT} .
CE IN	—	13	The input to the CE gating circuit. Connect to GND or V _{OUT} if not used.
CE OUT	—	12	CE OUT goes low only when CE IN is low and V _{CC} is above the reset threshold (4.65V for MAX691 and MAX695, 4.4V for MAX693). See Figure 6.
BATT ON	—	5	BATT ON goes high when V _{OUT} is internally switched to the V _{BATT} input. It goes low when V _{OUT} is internally switched to V _{CC} . The output typically sinks 25mA and can directly drive the base of an external PNP transistor to increase the output current above the 50mA rating of V _{OUT} .
LOW LINE	—	6	LOW LINE goes low when V _{CC} falls below the reset threshold. It returns high as soon as V _{CC} rises above the reset threshold. See Figure 6, Reset Timing.
RESET	—	16	RESET is an active high output. It is the inverse of RESET.
OSC SEL	—	8	When OSC SEL is unconnected or driven high, the internal oscillator sets the reset time delay and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3μA internal pullup. See Table 1.
OSC IN	—	7	When OSC SEL is low, OSC IN can be driven by an external clock to adjust both the reset delay and the watchdog timeout period. The timing can also be adjusted by connecting an external capacitor to this pin. See Figure 8. When OSC SEL is high or floating, OSC IN selects between fast and slow Watchdog timeout periods.
WDO	—	14	The Watchdog Output, WDO, goes low if WDI remains either high or low for longer than the Watchdog timeout period. WDO is set high by the next transition at WDI. If WDI is unconnected or at mid-supply, WDO remains high. WDO also goes high when LOW LINE goes low.

MAX690/91/92/93/94/95

MAX691, MAX693 and MAX695

Reset Output

The crystal oscillator normally used to generate the clock for microprocessors takes several milliseconds to start. Since most microprocessors need several clock cycles to reset, RESET must be held low until the microprocessor clock oscillator has started. The

*200ms for MAX695

Power Fail Detector

RAM Write Protection

The MAX691/93/95 $\overline{\text{CE OUT}}$ line drives the $\overline{\text{Chip Select}}$ inputs of the CMOS RAM. $\overline{\text{CE OUT}}$ follows $\overline{\text{CE IN}}$ as long as V_{CC} is above the 4.65V (4.4V for MAX693) reset threshold. If V_{CC} falls below the reset threshold, $\overline{\text{CE OUT}}$ goes high, independent of the logic level at $\overline{\text{CE IN}}$. This prevents the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions. The LOW LINE output goes low when V_{CC} falls below 4.65V (4.4V for MAX693).



Figure 1. MAX691/693/695 Typical Application

Microprocessor Supervisory Circuits

Watchdog Timer

The microprocessor drives the WATCHDOG INPUT (WDI) with an I/O line. When OSC IN and OSC SEL are unconnected, the microprocessor must toggle the WDI pin once every 1.6 seconds to verify proper software execution. If a hardware or software failure occurs such that WDI not toggled, the MAX691/93 will issue a 50ms* RESET pulse after 1.6 seconds. This typically restarts the microprocessor's power-up routine. A new RESET pulse is issued every 1.6 seconds until WDI is again strobed.

The WATCHDOG OUTPUT (\overline{WDO}) goes low if the watchdog timer is not serviced within its timeout period. Once \overline{WDO} goes low it remains low until a transition occurs at WDI. The watchdog timer feature can be disabled by leaving WDI unconnected. OSC IN and OSC SEL also allow other watchdog timing options, as shown in Table 1 and Figure 8.

MAX690, MAX692 and MAX694

The 8 pin MAX690, MAX692 and MAX694 have most of the features of the MAX691, MAX693 and MAX695.

*200ms for MAX695

Figure 2 shows the MAX690/692/694 in a typical application. Operation is much the same as with the MAX691/693/695 (Figure 1) but in this case the Power Fail Input (PFI) monitors the unregulated input to the 7805 regulator. The MAX690/694 RESET output goes low when V_{CC} falls below 4.65V. The RESET output of the MAX692 goes low when V_{CC} drops below 4.4V.

The current consumption of the battery-backed-up power bus must be less than 50mA. The MAX690/692/694 does not have a BATT ON output to drive an external transistor. The MAX690/92/94 also does not include chip enable gating circuitry that is available on the MAX691/93/95. In many systems though, CE gating is not needed since a low input to the microprocessor RESET line prevents the processor from writing to RAM during power-up and power-down transients.

The MAX690/92/94 watchdog timer has a fixed 1.6 second timeout period. If WDI remains either low or high for more than 1.6 seconds, a RESET pulse is sent to the microprocessor. The watchdog timer is disabled if WDI is left floating.

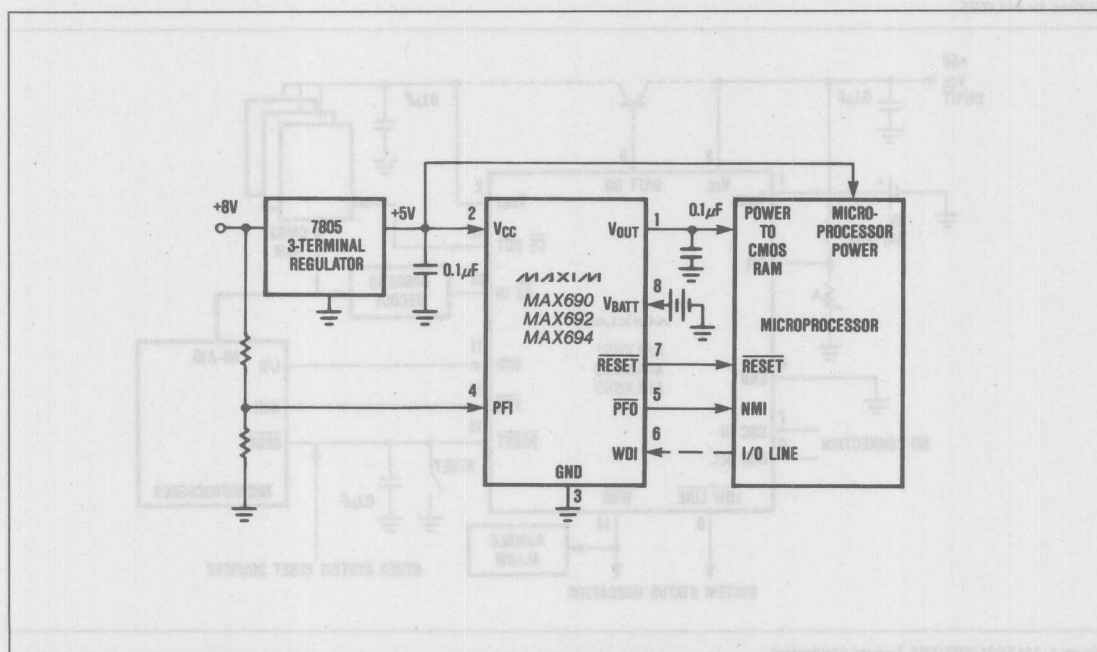


Figure 2. MAX690/692/694 Typical Application

Microprocessor Supervisory Circuits

MAX690/91/92/93/94/95

Detailed Description

Battery-Switchover and V_{OUT}

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. Switchover occurs when V_{CC} is 50mV greater than V_{BATT} as V_{CC} falls, and when V_{CC} is 70mV more than V_{BATT} as V_{CC} rises (see Figure 4). The switchover comparator has 20mV of hysteresis to prevent repeated, rapid switching if V_{CC} falls very slowly or remains nearly equal to the battery voltage.

When V_{CC} is higher than V_{BATT} , V_{CC} is internally switched to V_{OUT} via a low saturation PNP transistor. V_{OUT} has 50mA output current capability. Use an external PNP pass transistor in parallel with internal transistor if the output current requirement at V_{OUT} exceeds 50mA or if a lower V_{CC} - V_{OUT} voltage differential is desired. The BATT ON output (MAX691/693/695 only) can directly drive the base of the external transistor.

It should be noted that the MAX690/91/92/93/94/95 need only supply the average current drawn by the CMOS RAM if there is adequate filtering. Many RAM data sheets specify a 75mA maximum supply current, but this peak current spike lasts only 100ns. A 0.1 μ F bypass capacitor at V_{OUT} supplies the high instantaneous current, while V_{OUT} need only supply the average load current, which is much less. A capacitance of 0.1 μ F or greater must be connected to the V_{OUT} terminal to ensure stability.

A 200 Ω MOSFET connects the V_{BATT} input to V_{OUT}

during battery backup. This MOSFET has very low input-to-output differential (dropout voltage) at the low current levels required for battery backup of CMOS RAM or other low power CMOS circuitry. When V_{CC} equals V_{BATT} the supply current is typically 12 μ A. When V_{CC} is between 0V and (V_{BATT} - 700mV) the typical supply current is only 600nA typical, 1 μ A maximum.

The MAX690/691/694/695 operates with battery voltages from 2.0V to 4.25V while the MAX692/693 operates with battery voltages from 2.0V to 4.0V. High value capacitors, either standard electrolytic or the farad-size double layer capacitors, can also be used for short-term memory backup. The charging resistor for both capacitors and rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists if the resistor is connected to V_{CC} .

A small charging current of typically 10nA (0.1 μ A max) flows out of the V_{BATT} terminal. This current varies with the amount of current that is drawn from V_{OUT} but its polarity is such that the backup battery is always slightly charged, and is never discharged while V_{CC} is in its operating voltage range. This extends the shelf life of the backup battery by compensating for its self-discharge current. Also note that this current poses no problem when lithium batteries are used for backup since the maximum charging current (0.1 μ A) is safe for even the smallest lithium cells.

If the battery-switchover section is not used, connect V_{BATT} to GND and connect V_{OUT} to V_{CC} . Table 2 shows the state of the inputs and output in the low power battery backup mode.

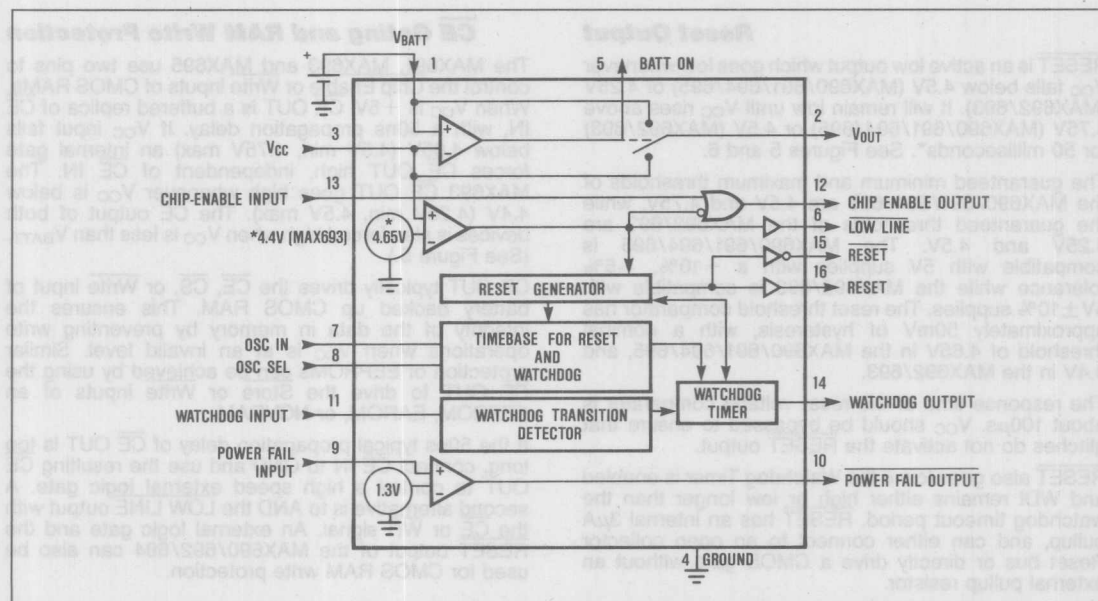


Figure 3. MAX691/693/695 Block Diagram

Microprocessor Supervisory Circuits

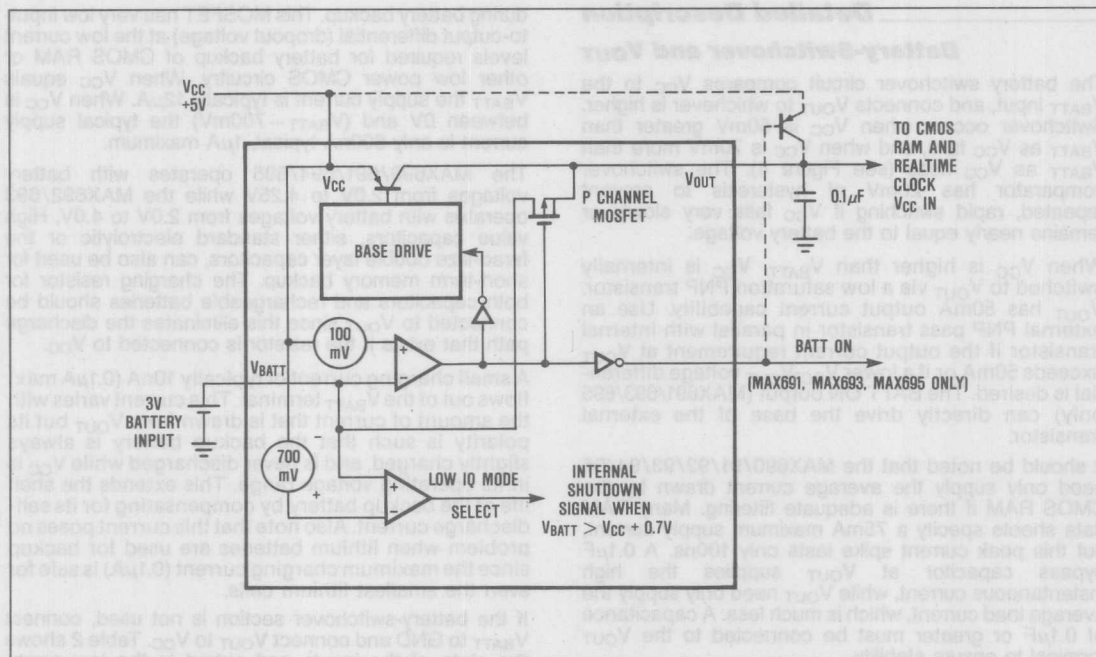


Figure 4. Battery-Switchover Block Diagram

Reset Output

RESET is an active low output which goes low whenever V_{CC} falls below 4.5V (MAX690/691/694/695) or 4.25V (MAX692/693). It will remain low until V_{CC} rises above 4.75V (MAX690/691/694/695) or 4.5V (MAX692/693) for 50 milliseconds*. See Figures 5 and 6.

The guaranteed minimum and maximum thresholds of the MAX690/691/694/695 are 4.5V and 4.75V, while the guaranteed thresholds of the MAX692/693 are 4.25V and 4.5V. The MAX690/691/694/695 is compatible with 5V supplies with a +10%, -5% tolerance while the MAX692/693 is compatible with $5V \pm 10\%$ supplies. The reset threshold comparator has approximately 50mV of hysteresis, with a nominal threshold of 4.65V in the MAX690/691/694/695, and 4.4V in the MAX692/693.

The response time of the reset voltage comparator is about 100 μ s. V_{CC} should be bypassed to ensure that glitches do not activate the **RESET** output.

RESET also goes low if the Watchdog Timer is enabled and WDI remains either high or low longer than the watchdog timeout period. **RESET** has an internal 3 μ A pullup, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pullup resistor.

*200ms for MAX694 and MAX695

\overline{CE} Gating and RAM Write Protection

The MAX691, MAX693 and MAX695 use two pins to control the Chip Enable or Write inputs of CMOS RAMs. When V_{CC} is +5V, \overline{CE} OUT is a buffered replica of \overline{CE} IN, with a 50ns propagation delay. If V_{CC} input falls below 4.65V (4.5V min, 4.75V max) an internal gate forces \overline{CE} OUT high, independent of \overline{CE} IN. The MAX693 \overline{CE} OUT goes high whenever V_{CC} is below 4.4V (4.25V min, 4.5V max). The \overline{CE} output of both devices is also forced high when V_{CC} is less than V_{BATT} . (See Figure 5.)

\overline{CE} OUT typically drives the \overline{CE} , \overline{CS} , or \overline{Write} input of battery backed up CMOS RAM. This ensures the integrity of the data in memory by preventing write operations when V_{CC} is at an invalid level. Similar protection of EEPROMs can be achieved by using the \overline{CE} OUT to drive the Store or Write inputs of an EEPROM, EAROM, or NOVRAM.

If the 50ns typical propagation delay of \overline{CE} OUT is too long, connect \overline{CE} IN to GND and use the resulting \overline{CE} OUT to control a high speed external logic gate. A second alternative is to AND the LOW LINE output with the \overline{CE} or WR signal. An external logic gate and the **RESET** output of the MAX690/692/694 can also be used for CMOS RAM write protection.

Microprocessor Supervisory Circuits

MAX690/91/92/93/94/95

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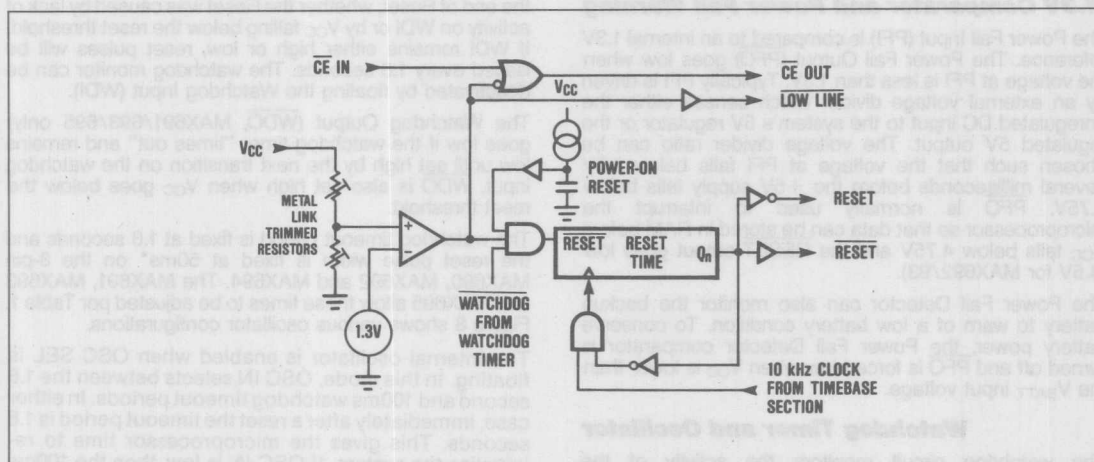


Figure 5. Reset Block Diagram

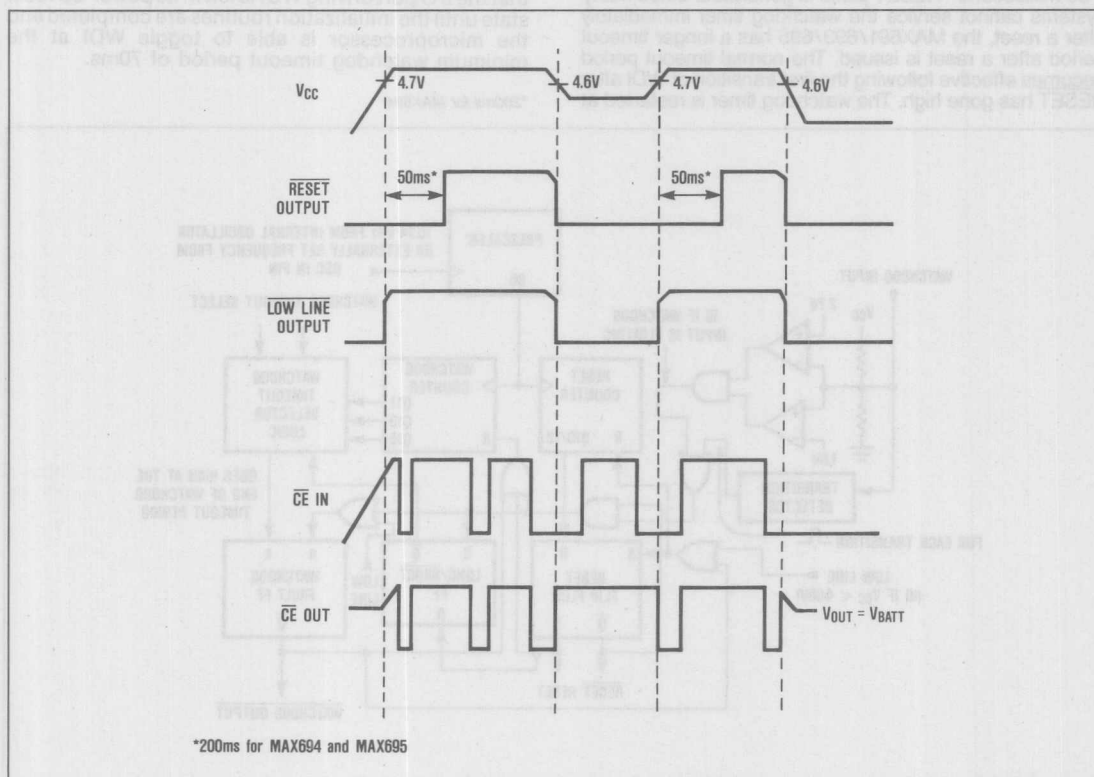


Figure 6. Reset Timing

MAXIM

The Power Fail Input (PFI) is compared to an internal 1.3V reference. The Power Fail Output (PFO) goes low when the voltage at PFI is less than 1.3V. Typically PFI is driven by an external voltage divider which senses either the unregulated DC input to the system's 5V regulator or the regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI falls below 1.3V several milliseconds before the +5V supply falls below 4.75V. PFO is normally used to interrupt the microprocessor so that data can be stored in RAM before V_{CC} falls below 4.75V and the RESET output goes low (4.5V for MAX692/93).

The Power Fail Detector can also monitor the backup battery to warn of a low battery condition. To conserve battery power, the Power Fail Detector comparator is turned off and PFO is forced low when V_{CC} is lower than the V_{BATT} input voltage.

The watchdog circuit monitors the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the selected timeout period, a 50 millisecond* RESET pulse is generated. Since many systems cannot service the watchdog timer immediately after a reset, the MAX691/693/695 has a longer timeout period after a reset is issued. The normal timeout period becomes effective following the first transition of WDI after RESET has gone high. The watchdog timer is restarted at

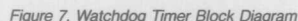
the end of Reset, whether the Reset was caused by lack of activity on WDI or by V_{CC} falling below the reset threshold. If WDI remains either high or low, reset pulses will be issued every 1.6 seconds. The watchdog monitor can be deactivated by floating the Watchdog Input (WDI).

The Watchdog Output ($\overline{\text{WDO}}$, MAX691/693/695 only) goes low if the watchdog timer “times out” and remains low until set high by the next transition on the watchdog input. WDO is also set high when V_{CC} goes below the reset threshold.

The watchdog timeout period is fixed at 1.6 seconds and the reset pulse width is fixed at 50ms* on the 8-pin MAX690, MAX692 and MAX694. The MAX691, MAX693 and MAX695 allow these times to be adjusted per Table 1. Figure 8 shows various oscillator configurations.

The internal oscillator is enabled when OSC SEL is floating. In this mode, OSC IN selects between the 1.6 second and 100ms watchdog timeout periods. In either case, immediately after a reset the timeout period is 1.6 seconds. This gives the microprocessor time to re-initialize the system. If OSC IN is low, then the 100ms watchdog period becomes effective after the first transition of WDI. The software should be written such that the I/O port driving WDI is left in its power-up reset state until the initialization routines are completed and the microprocessor is able to toggle WDI at the minimum watchdog timeout period of 70ms.

*200ms for MAX694



Microprocessor Supervisory Circuits

MAX690/91/92/93/94/95

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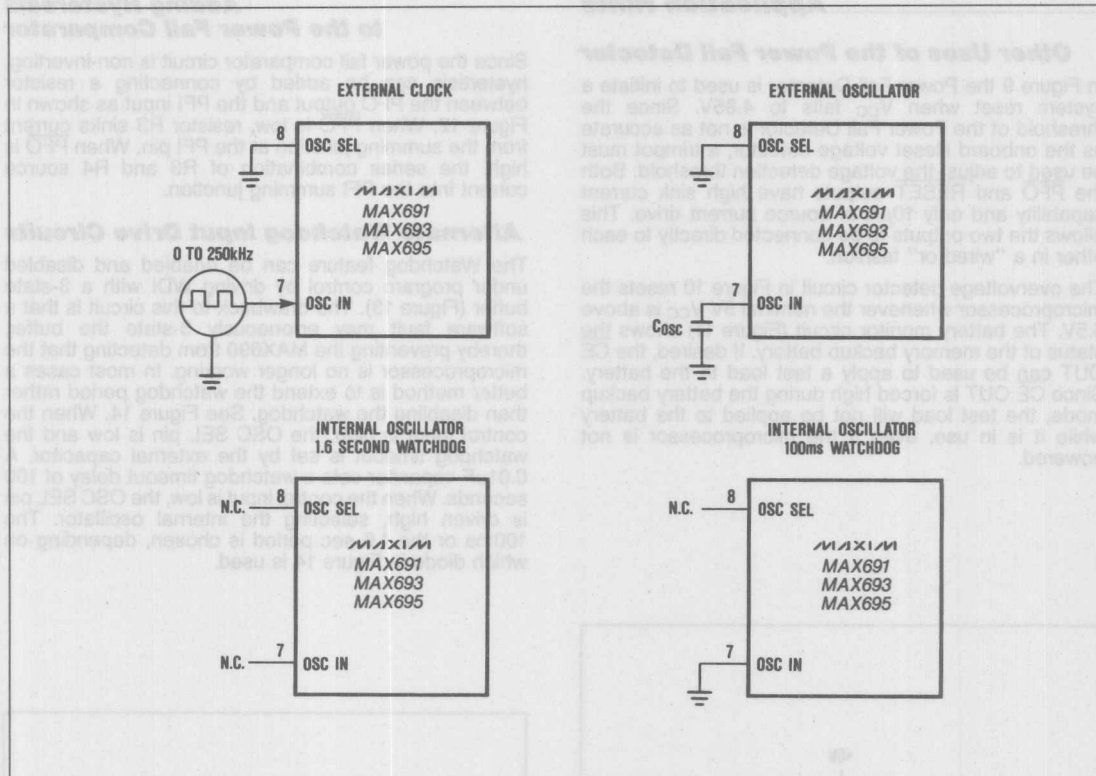


Figure 8. Oscillator Circuits

Table 1. MAX691, MAX693 and MAX695 Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period	
		Normal	Immediately After Reset	MAX691/93	MAX695
Low	External Clock Input	1024 clks	4096 clks	512 clks	2048 clks
Low	External Capacitor	$\frac{400\text{ms}}{47\text{pF}} \times C$	$\frac{1.6 \text{ sec}}{47\text{pF}} \times C$	$\frac{200\text{ms}}{47\text{pF}} \times C$	$\frac{800\text{ms}}{47\text{pF}} \times C$
Floating	Low	100ms	1.6 sec	50ms	200ms
Floating	Floating	1.6 sec	1.6 sec	50ms	200ms

Note 1: The MAX690/692/694 watchdog timeout period is fixed at 1.6 seconds nominal, the MAX690/692 Reset pulse width is fixed at 50ms nominal and the MAX694 is 200ms nominal.

Note 2: When the MAX691 OSC SEL pin is low, OSC IN can be driven by an external clock signal, or an external capacitor can be connected between OSC IN and GND. The nominal internal oscillator frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is

$$F_{\text{osc}}(\text{Hz}) = \frac{184,000}{C(\text{pF})}$$

Note 3: See Electrical Characteristics Table for minimum and maximum timing values.

Microprocessor Supervisory Circuits

Application Hints

Other Uses of the Power Fail Detector

In Figure 9 the Power Fail Detector is used to initiate a system reset when V_{CC} falls to 4.85V. Since the threshold of the Power Fail Detector is not as accurate as the onboard Reset voltage detector, a trimpot must be used to adjust the voltage detection threshold. Both the PFO and RESET outputs have high sink current capability and only 10 μ A of source current drive. This allows the two outputs to be connected directly to each other in a "wired or" fashion.

The overvoltage detector circuit in Figure 10 resets the microprocessor whenever the nominal 5V V_{CC} is above 5.5V. The battery monitor circuit (Figure 11) shows the status of the memory backup battery. If desired, the CE OUT can be used to apply a test load to the battery. Since CE OUT is forced high during the battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

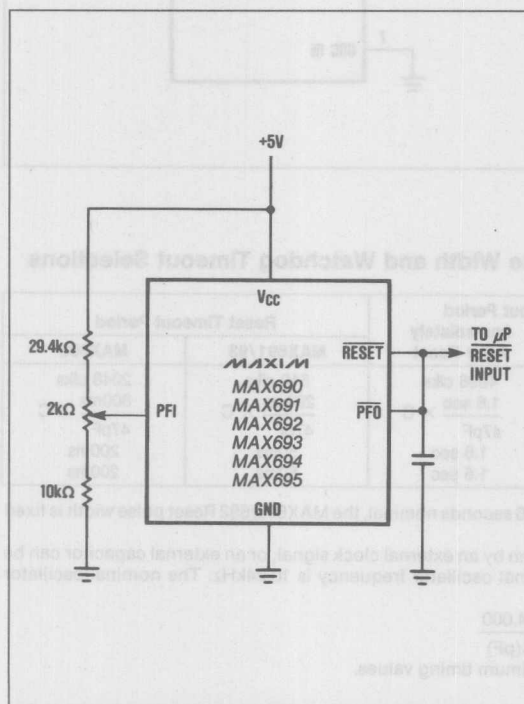


Figure 9. Externally Adjustable V_{CC} Reset Threshold

Adding Hysteresis to the Power Fail Comparator

Since the power fail comparator circuit is non-inverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 12. When PFO is low, resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, the series combination of R3 and R4 source current into the PFI summing junction.

Alternate Watchdog Input Drive Circuits

The Watchdog feature can be enabled and disabled under program control by driving WDI with a 3-state buffer (Figure 13). The drawback to this circuit is that a software fault may erroneously 3-state the buffer, thereby preventing the MAX690 from detecting that the microprocessor is no longer working. In most cases a better method is to extend the watchdog period rather than disabling the watchdog. See Figure 14. When the control input is high, the OSC SEL pin is low and the watchdog timeout is set by the external capacitor. A 0.01 μ F capacitor sets a watchdog timeout delay of 100 seconds. When the control input is low, the OSC SEL pin is driven high, selecting the internal oscillator. The 100ms or the 1.6 sec period is chosen, depending on which diode in Figure 14 is used.

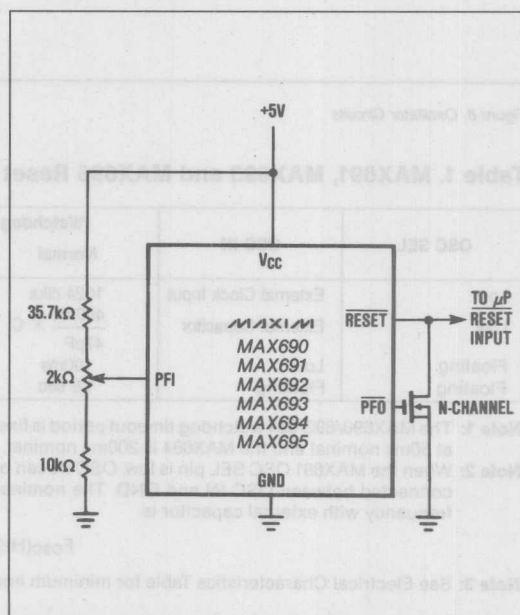


Figure 10. Reset on Overvoltage or Undervoltage

Microprocessor Supervisory Circuits

MAX690/91/92/93/94/95

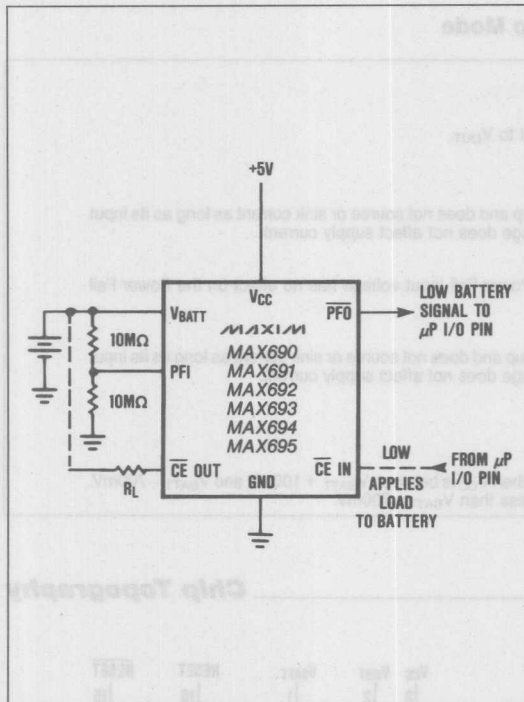


Figure 11. Backup Battery Monitor with Optional Test Load

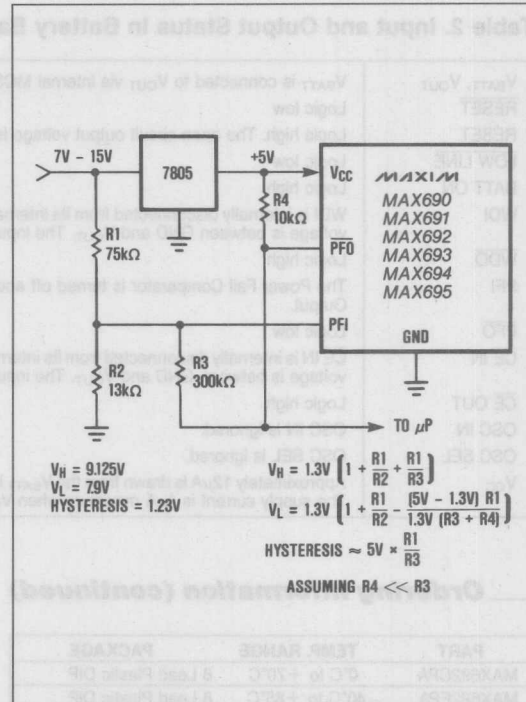


Figure 12. Adding Hysteresis to the Power Fail Voltage Comparator

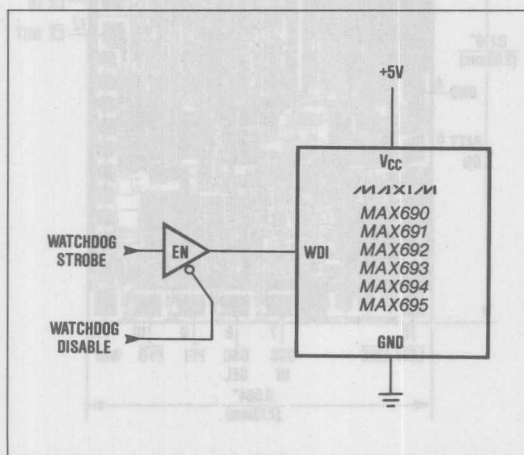


Figure 13. Disabling the Watchdog Under Program Control

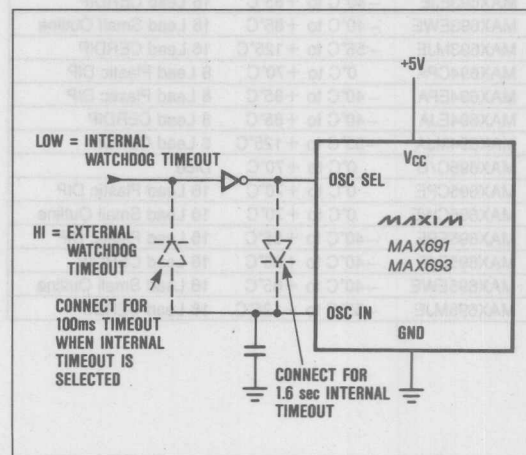


Figure 14. Selecting Internal or External Watchdog Timeout

Microprocessor Supervisory Circuits

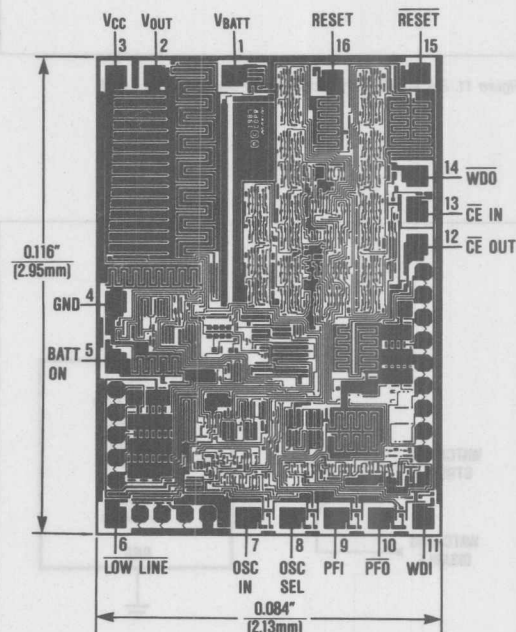
Table 2. Input and Output Status In Battery Backup Mode

V_{BATT} , V_{OUT}	V_{BATT} is connected to V_{OUT} via internal MOSFET.
RESET	Logic low
RESET	Logic high. The open circuit output voltage is equal to V_{OUT} .
LOW LINE	Logic low
BATT ON	Logic high
WDI	WDI is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT} . The input voltage does not affect supply current.
WDO	Logic high
PFI	The Power Fail Comparator is turned off and the Power Fail Input voltage has no effect on the Power Fail Output.
PFO	Logic low
\overline{CE} IN	\overline{CE} IN is internally disconnected from its internal pullup and does not source or sink current as long as its input voltage is between GND and V_{OUT} . The input voltage does not affect supply current.
\overline{CE} OUT	Logic high
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.
V_{CC}	Approximately 12 μ A is drawn from the V_{BATT} input when V_{CC} is between $V_{BATT} + 100\text{mV}$ and $V_{BATT} - 700\text{mV}$. The supply current is 1 μ A maximum when V_{CC} is less than $V_{BATT} - 700\text{mV}$.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX692CPA	0°C to +70°C	8 Lead Plastic DIP
MAX692EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX692EJA	-40°C to +85°C	8 Lead CERDIP
MAX692MJA	-55°C to +125°C	8 Lead CERDIP
MAX693C/D	0°C to +70°C	Dice
MAX693CPE	0°C to +70°C	16 Lead Plastic DIP
MAX693CWE	0°C to +70°C	16 Lead Small Outline
MAX693EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX693EJE	-40°C to +85°C	16 Lead CERDIP
MAX693EWE	-40°C to +85°C	16 Lead Small Outline
MAX693MJE	-55°C to +125°C	16 Lead CERDIP
MAX694CPA	0°C to +70°C	8 Lead Plastic DIP
MAX694EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX694EJA	-40°C to +85°C	8 Lead CERDIP
MAX694MJA	-55°C to +125°C	8 Lead CERDIP
MAX695C/D	0°C to +70°C	Dice
MAX695CPE	0°C to +70°C	16 Lead Plastic DIP
MAX695CWE	0°C to +70°C	16 Lead Small Outline
MAX695EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX695EJE	-40°C to +85°C	16 Lead CERDIP
MAX695EWE	-40°C to +85°C	16 Lead Small Outline
MAX695MJE	-55°C to +125°C	16 Lead CERDIP

Chip Topography



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MAXIM

Low Cost Power-On Reset and Watchdog Controllers

General Description

The MAX698 and MAX699 monitor the +5V supply in microprocessor and digital systems. They supply a RESET pulse of at least 140ms duration on power-up, power-down, and during low voltage "brown out" conditions. Circuit reliability is increased at reduced cost by eliminating all external components and adjustments.

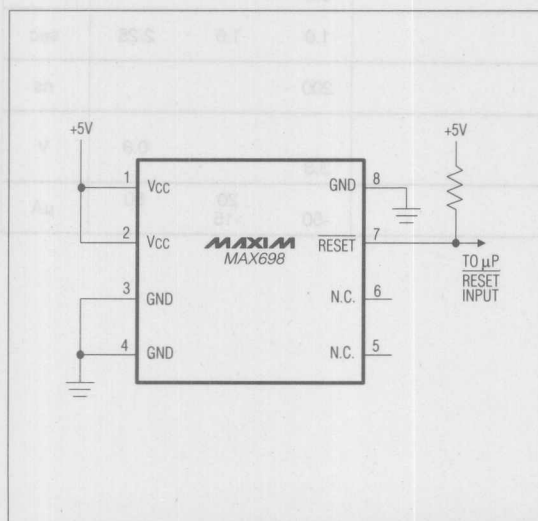
The MAX699 includes all features of the MAX698 but also provides a "watchdog" input to monitor microprocessor activity. The RESET output goes low if the watchdog input (WDI) is not toggled within 1 second. The watchdog feature can be disabled by leaving WDI open.

Both parts are supplied in 8 lead DIP and 16 lead 0.3" wide Small Outline (SO) packages and are specified from 0°C to +70°C for "C" grade devices and -40°C to +85°C for "E" devices. The Small Outline versions, with more pins than the 8 lead DIP, have additional outputs not available in DIP packages. These are RESET (without inversion) and Watchdog Output (WDO).

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μ P Power Monitoring

Typical Operating Circuit



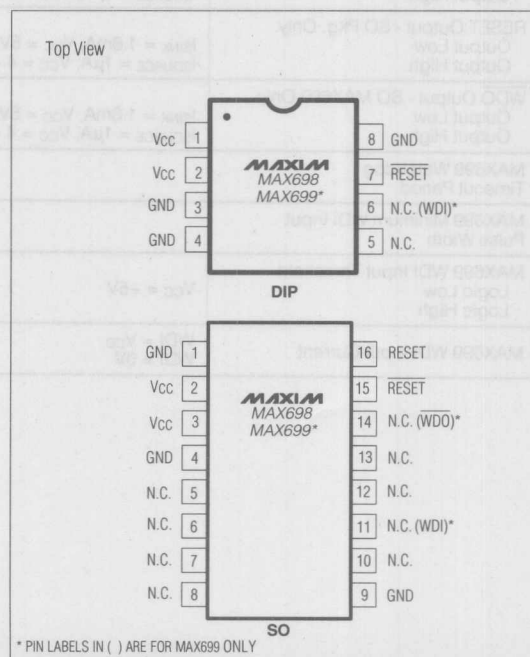
Features

- ◆ Precision Voltage Monitor
- ◆ Power OK/Reset Time Delay
- ◆ Watchdog Timer
- ◆ Minimum Component Count

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX698CPA	0°C to +70°C	8 Lead Plastic DIP
MAX698CWE	0°C to +70°C	16 Lead Wide SO
MAX698EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX698EWE	-40°C to +85°C	16 Lead Wide SO
MAX699CPA	0°C to +70°C	8 Lead Plastic DIP
MAX699CWE	0°C to +70°C	16 Lead Wide SO
MAX699EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX699EWE	-40°C to +85°C	16 Lead Wide SO

Pin Configurations



MAX698/MAX699

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MAXIM

Maxim Integrated Products 5-89

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Low Cost Power-On Reset and Watchdog Controllers

ABSOLUTE MAXIMUM RATINGS

V _{CC}	-0.3V to 6.0V	Rate of Rise, V _{CC}	100V/μs
Input Voltage (with respect to GND)		Power Dissipation	
WDI, WDO, RESET, RESET	-0.3V to V _{CC}	Plastic DIP (Derate 5mW/°C above 70°C)	400mW
Operating Temperature Range		Small Outline (Derate 7mW/°C above 70°C)	600mW
MAX69XC	0°C to +70°C	Storage Temperature	-65°C to +150°C
MAX69XE	-40°C to +85°C	Lead Temperature (Soldering 10 seconds)	+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operations sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = +5V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	T _A = Full	3.0		5.5	V
Supply Current				5	mA
Power Up Reset De-Assertion	T _A = Full	4.5	4.65	4.75	V
Power Down Reset Assertion	T _A = Full	4.4			V
Hysteresis			40		mV
Reset Output Pulse Width		140		500	ms
RESET Output Output Low Output High	(Open Drain) I _{SINK} = 1.6mA, V _{CC} = 4.4V I _{SOURCE} = 1μA, V _{CC} = 5V	3.5		0.4	V
RESET Output - SO Pkg. Only Output Low Output High	I _{SINK} = 1.6mA, V _{CC} = 5V I _{SOURCE} = 1μA, V _{CC} = 4.4V	3.5		0.4	V
WDO Output - SO MAX699 Only Output Low Output High	I _{SINK} = 1.6mA, V _{CC} = 5V I _{SOURCE} = 1μA, V _{CC} = 4.4V	3.5		0.4	V
MAX699 Watchdog Timeout Period		1.0	1.6	2.25	sec
MAX699 Minimum WDI Input Pulse Width		200			ns
MAX699 WDI Input Threshold Logic Low Logic High	V _{CC} = +5V	3.8		0.8	V
MAX699 WDI Input Current	WDI = V _{CC} WDI = 0V	-50	20 -15	50	μA

Low Cost Power-On Reset and Watchdog Controllers

Pin Description

NAME	FUNCTION
V _{CC}	+5V sense input and MAX698/699 chip power.
GND	Chip power GND.
RESET	Goes low when V _{CC} falls below internally set threshold (See Electrical Characteristics).
RESET	(Small Outline devices only) Goes high when V _{CC} falls below internally set threshold.
WDI	(MAX699 only) A three level input. If WDI remains high or low for more than the watchdog timeout period, RESET pulses low (WDO also goes low on Small Outline MAX699). If WDI is unconnected or at mid supply, the watchdog circuit is disabled.
WDO	(Small Outline MAX699 only) Goes low when WDI remains high or low for more than the watchdog timeout period. WDO is set high at the next WDI transition. If WDI is unconnected or at mid supply, WDO remains high. WDO also remains high when V _{CC} falls below 4.4V.

MAX698/MAX699

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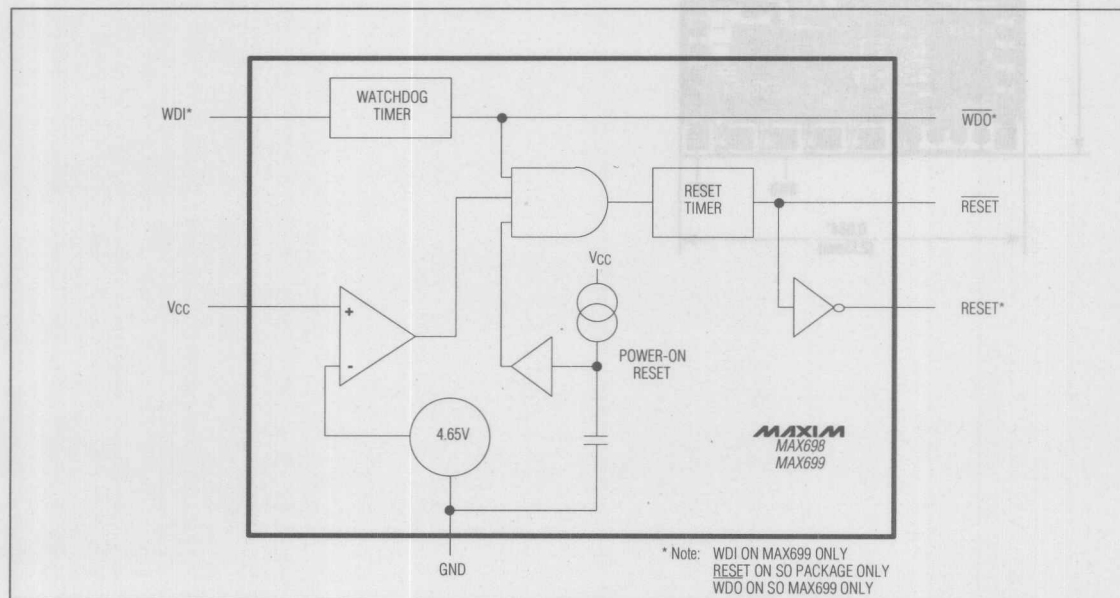
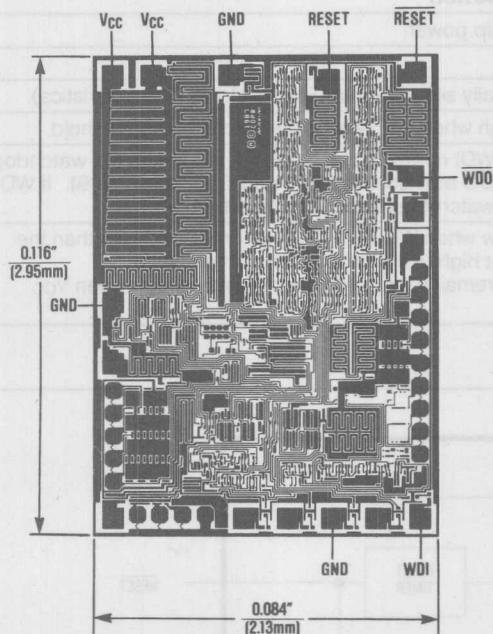


Figure 1. MAX698/699 Block Diagram

Low Cost Power-On Reset and Watchdog Controllers

Chip Topography

MAX698/MAX699



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INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

Power-Supply Monitor with Reset

General Description

The MAX700/701/702 are supervisory circuits used to monitor the power supplies in μ P and digital systems. The RESET/RESET outputs of the MAX700/701/702 are guaranteed to be in the correct state for V_{CC} voltages down to +1V (Figure 4). They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V powered circuits.

The MAX702 is the simplest part in the family. When V_{CC} falls to 4.65V, RESET goes low. The MAX702 also provides a debounced manual reset input. The MAX701 performs the same functions but has both RESET and RESET outputs. Their primary function is to provide a system reset. Accordingly, an active reset signal is supplied for low supply voltages and for at least 200ms after the supply voltage reaches its operating value.

In addition to the features of the MAX701 and MAX702, the MAX700 provides preset or adjustable voltage detection so thresholds other than 4.65V can be selected, and adjustable hysteresis. All parts are supplied in 8-pin Plastic DIP and Narrow SO packages and extended temperature ranges.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical μ P Power Monitoring

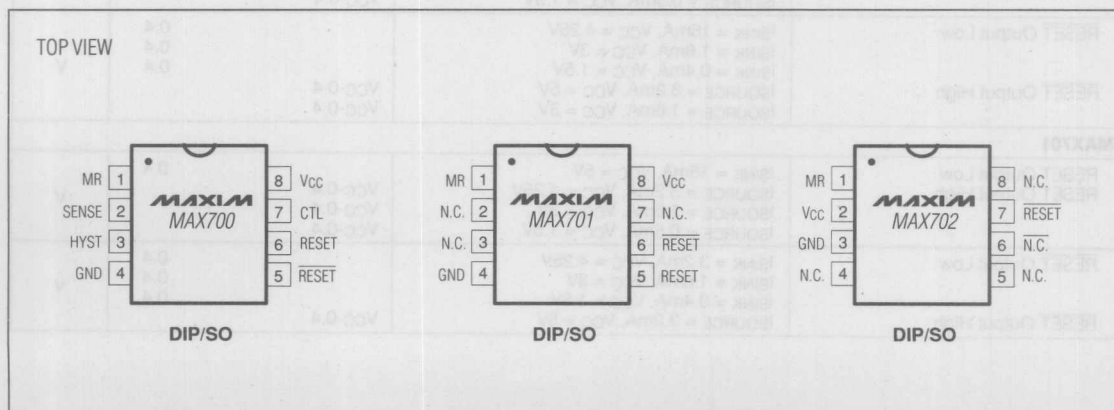
Features

- ◆ Min 200ms RESET Pulse on Power-Up, Power-Down, and During Low-Voltage Conditions
- ◆ Reset Threshold Factory Trimmed for +5V Systems
- ◆ No External Components or Adjustments With +5V Powered Circuits
- ◆ Debounced Manual Reset Input
- ◆ Preset or Adjustable Voltage Detection (MAX700)
- ◆ Adjustable Hysteresis (MAX700)
- ◆ 8-Pin Plastic DIP and Narrow SO Packages

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX700CPA	0°C to +70°C	8 Plastic DIP
MAX700CSA	0°C to +70°C	8 Narrow SO
MAX700C/D	0°C to +70°C	Dice
MAX700EPA	-40°C to +85°C	8 Plastic DIP
MAX700ESA	-40°C to +85°C	8 Narrow SO
MAX701CPA	0°C to +70°C	8 Plastic DIP
MAX701CSA	0°C to +70°C	8 Narrow SO
MAX701C/D	0°C to +70°C	Dice
MAX701EPA	-40°C to +85°C	8 Plastic DIP
MAX701ESA	-40°C to +85°C	8 Narrow SO
MAX702CPA	0°C to +70°C	8 Plastic DIP
MAX702CSA	0°C to +70°C	8 Narrow SO
MAX702C/D	0°C to +70°C	Dice
MAX702EPA	-40°C to +85°C	8 Plastic DIP
MAX702ESA	-40°C to +85°C	8 Narrow SO

Pin Configurations



MAXIM

Maxim Integrated Products 5-93

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MAX700/701/702

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Power-Supply Monitor with Reset

ABSOLUTE MAXIMUM RATINGS

V _{CC}	-0.3V to +15.5V
Voltage (with respect to GND) at RESET, RESET, HYST,	
CTL, SENSE	-0.3V to V _{CC}
Operating Temperature Range	
MAX70_C	0°C to +70°C
MAX70_E	-40°C to +85°C

Rate of Rise, V _{CC}	100V/μs
Power Dissipation, any package	380mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = +5V, CTL = GND on MAX700, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CC} Monitor Voltage Range MAX700 Only	T _A = T _{MIN} to T _{MAX} CTL = V _{CC}	3		15	V
Min V _{CC} For Valid Reset Output, Declining Supply	T _A = T _{MIN} to T _{MAX} RESET ≤ 0.4V when sinking 1mA	1.5	1		V
Supply Current			100	200	μA
Reset Threshold Power-up Power-down	T _A = T _{MIN} to T _{MAX}	4.5 4.5	4.65 4.62	4.75 4.75	V
Internal Hysteresis	HYST not connected		30		mV
Reset Output Pulse Width		200	350	500	ms
RESET Fall Time	MAX700/701 Only, C _{LOAD} = 100pF		200		ns
V _{CC} Pulse Duration Guaranteeing No Reset Reset	5V to 4V V _{CC} Pulse	100	10 10	1	μs
MR Input Threshold			0.7		V
MR Pullup Current			-5	-30	μA
MAX700					
RESET Output Low	ISINK = 3.2mA, V _{CC} = 5V ISINK = 1.6mA, V _{CC} = 3V			0.4 0.4	V
RESET Output High	ISOURCE = 3.2mA, V _{CC} = 4.25V ISOURCE = 1.6mA, V _{CC} = 3V ISOURCE = 0.5mA, V _{CC} = 1.5V	V _{CC} -0.4 V _{CC} -0.4 V _{CC} -0.4			
RESET Output Low	ISINK = 16mA, V _{CC} = 4.25V ISINK = 1.6mA, V _{CC} = 3V ISINK = 0.4mA, V _{CC} = 1.5V			0.4 0.4 0.4	V
RESET Output High	ISOURCE = 3.2mA, V _{CC} = 5V ISOURCE = 1.6mA, V _{CC} = 3V	V _{CC} -0.4 V _{CC} -0.4			
MAX701					
RESET Output Low RESET Output High	ISINK = 16mA, V _{CC} = 5V ISOURCE = 3.2mA, V _{CC} = 4.25V ISOURCE = 1.6mA, V _{CC} = 3V ISOURCE = 0.5mA, V _{CC} = 1.5V			0.4 V _{CC} -0.4 V _{CC} -0.4 V _{CC} -0.4	V
RESET Output Low	ISINK = 3.2mA, V _{CC} = 4.25V ISINK = 1.6mA, V _{CC} = 3V ISINK = 0.4mA, V _{CC} = 1.5V			0.4 0.4 0.4	V
RESET Output High	ISOURCE = 3.2mA, V _{CC} = 5V	V _{CC} -0.4			

Power-Supply Monitor with Reset

MAX700/701/702

ELECTRICAL CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$, $CTL = \text{GND}$ on MAX700, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAX702					
RESET Output Low	$I_{\text{SINK}} = 3.2\text{mA}$, $V_{CC} = 4.25\text{V}$ $I_{\text{SINK}} = 1.6\text{mA}$, $V_{CC} = 3\text{V}$ $I_{\text{SINK}} = 0.4\text{mA}$, $V_{CC} = 1.5\text{V}$			0.4 0.4 0.4	V
RESET Output High	$I_{\text{SOURCE}} = 3.2\text{mA}$, $V_{CC} = 5\text{V}$	$V_{CC}-0.4$			
MAX700 ONLY (CTL = V_{CC}, unless otherwise noted.)					
SENSE Input Threshold	$T_A = T_{\text{MIN}}$ to T_{MAX}	1.25	1.29	1.35	V
SENSE Input Current			0.1		nA
HYST Input On Resistance			0.5		k Ω
CTL Input Threshold			2		V
CTL Pulldown Current			30	100	μA

Pin Description

NAME	FUNCTION
V_{CC}	Chip power and +5V sensing input (when $CTL = \text{GND}$ on MAX700).
GND	Ground
RESET	Goes low when V_{CC} falls below 4.65V, or when $CTL = V_{CC}$ on the MAX700 goes low when SENSE falls below 1.9V.
RESET	MAX700, 701 only – Inverted Version of RESET.
MR	Input for manual push button reset. Has internal $5\mu\text{A}$ pull up. Low input activates the RESET/RESET outputs.
CTL	MAX700 only – When $CTL = \text{GND}$, V_{CC} is monitored by the reset circuit. When $CTL = V_{CC}$, V_{CC} is ignored and SENSE is monitored, allowing the threshold to be set with external resistors.
HYST	MAX700 only – Normally NOT used when voltage is monitored through V_{CC} ($CTL = \text{GND}$). When monitoring through SENSE ($CTL = V_{CC}$), HYST allows hysteresis to be added, reducing noise and spurious reset activity (Figure 3). HYST turns on $5\mu\text{s}$ before the RESET/RESET outputs are activated, and its on resistance to GND is typically $1\text{k}\Omega$.
SENSE	MAX700 only – The voltage sense input when $CTL = V_{CC}$. Its threshold is 1.29V. Sense always remains connected to the internal comparator. So, when V_{CC} is being monitored internally ($CTL = \text{GND}$), SENSE should be left open circuit.

Power-Supply Monitor with Reset

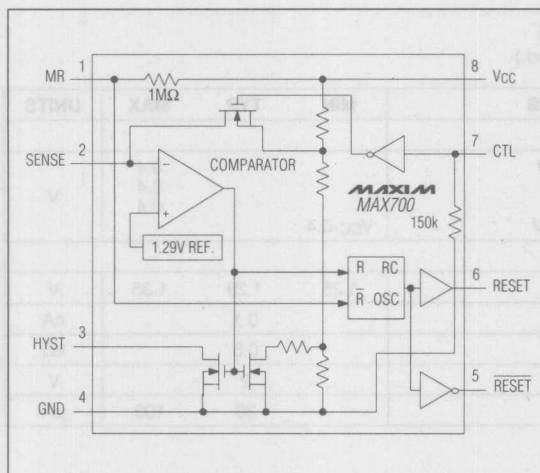


Figure 1. MAX700 Block Diagram

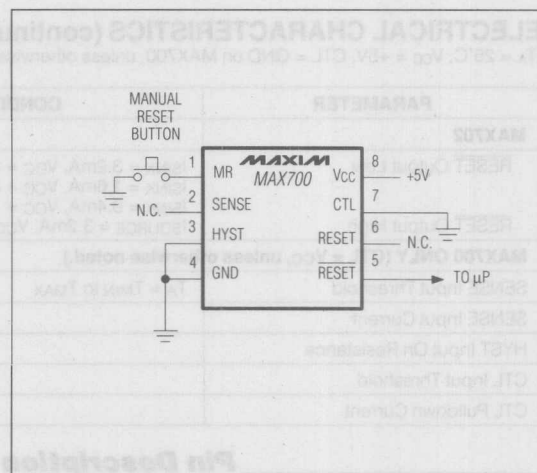


Figure 2. MAX700 Typical Connection Diagram

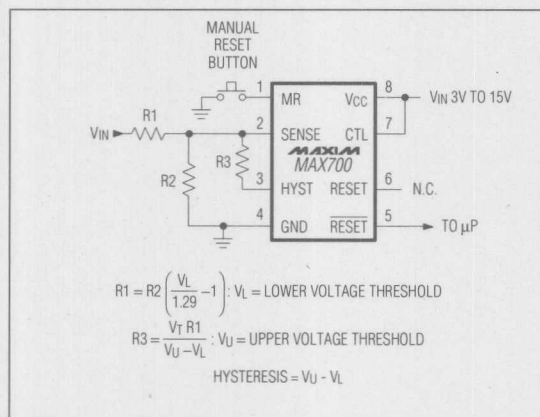


Figure 3. MAX700 Connected for External Sense and Hysteresis

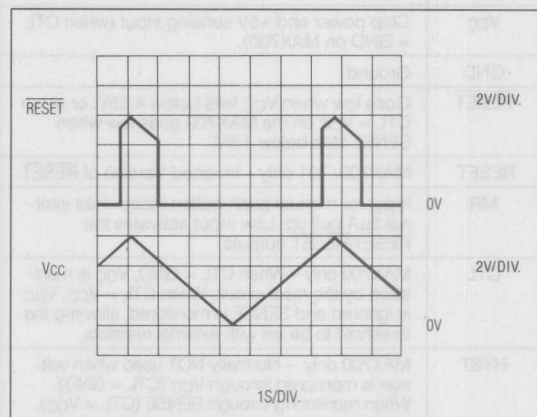


Figure 4. Typical MAX700/701/702 RESET Output vs. VCC

Figure 4 shows the RESET output of the MAX700/701/702 in the correct state for VCC voltages down to 0V. Note the effect of the built-in hysteresis on the trigger level of RESET.

Dual-Output, Switch-Mode Regulator (+5V to $\pm 12V$ or $\pm 15V$)

General Description

The MAX742 dual DC-DC converter IC creates dual-output power supplies in the 3W to 60W range. Relying on simple two-terminal inductors, the MAX742 regulates both outputs independently to within $\pm 4\%$ over line voltage and temperature.

The MAX742 provides high-efficiency conversion ($>75\%$) over a wide range of load currents. Two independent current-mode feedback loops provide tight regulation and operation free from subharmonic noise.

The MAX742 operates at a 200kHz frequency which is generated internally by a precise, laser-trimmed oscillator. This allows relatively small and lightweight external components in the end-use circuit and makes it easy to filter noise and ripple at the output.

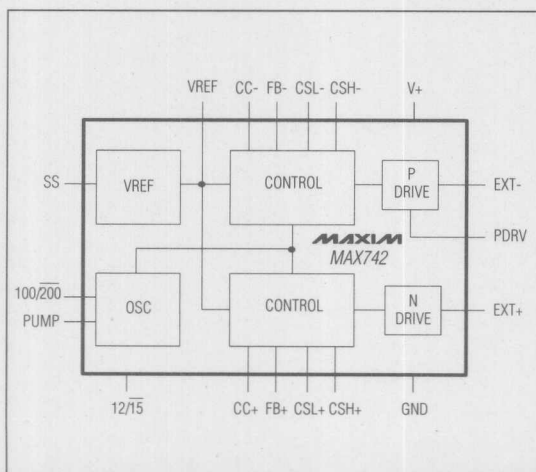
External power MOSFETs driven directly from the MAX742 are protected by cycle-by-cycle overcurrent sensing. The MAX742 also features undervoltage lock-out, thermal shutdown, and programmable soft-start.

If 3W of load power or less is needed, refer to the MAX743 data sheet for a device with internal power MOSFETs.

Applications

DC-DC Converter Module Replacement
Distributed Power Systems
Computer Peripherals

Block Diagram



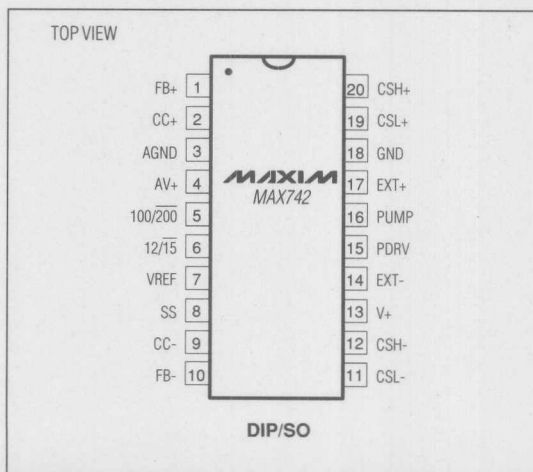
Features

- ◆ Specs Guaranteed for In-Circuit Performance
- ◆ $\pm 4\%$ Output Tolerance Max. Over Temp. and Line
- ◆ Switches from $\pm 15V$ to $\pm 12V$ Under Logic Control
- ◆ Load Currents to $\pm 2A$
- ◆ High Efficiency: 80% Typical
- ◆ Low-Noise, Current-Mode Feedback
- ◆ Cycle-by-Cycle Current Limiting
- ◆ Undervoltage Lock-out and Soft-Start

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX742CPP	0°C to +70°C	20 Plastic DIP
MAX742CWP	0°C to +70°C	20 Wide SO
MAX742EPP	-40°C to +85°C	20 Plastic DIP
MAX742EWP	-40°C to +85°C	20 Wide SO
MAX742MJP	-55°C to +125°C	20 CERDIP

Pin Configuration



Dual-Output, Switch-Mode Regulator (+5V to $\pm 15V$ or $\pm 12V$)

MAX743

General Description

The MAX743 DC-DC converter IC contains all the active circuitry needed to build small, dual-output power supplies. Relying on simple 2-terminal inductors rather than transformers, the MAX743 regulates both outputs independently to within $\pm 4\%$ over all conditions of line voltage, temperature, and load current.

The MAX743 typically provides 75% to 82% efficiency over most of the load range. It operates with current-mode feedback at 200kHz, so it can be used with rather small, lightweight external components. Also, ripple and noise are easy to filter.

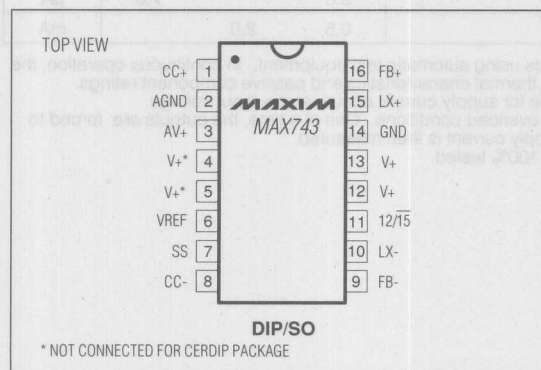
The MAX743 is inherently reliable due to its internal power transistors and monolithic construction. Thermal shutdown prevents overheating, and cycle-by-cycle current sensing protects the power-switch transistors. Other features include undervoltage lock-out and programmable soft-start.

Inductors, capacitors, and diodes to complement the MAX743 can be ordered directly from Maxim in production quantities. If higher load currents are needed, refer to the MAX742 data sheet for a device which drives external power MOSFETs.

Applications

- DC-DC Converter Module Replacement
- Distributed Power Systems
- Computer Peripherals
- Portable Instruments

Pin Configuration



Features

- Generates $\pm 100mA$ or $\pm 125mA$
- Specs Guaranteed for In-Circuit Performance
- $\pm 4\%$ Output Tolerance Max Over Temp, Line, and Load
- 82% Typ Efficiency
- Low-Noise, Current-Mode Feedback
- On-Board Current Limiting
- Thermal Shutdown Protection
- Undervoltage Lock-Out and Soft-Start
- Switches From $\pm 15V$ to $\pm 12V$ Under Logic Control
- Evaluation Kit Available
- Internal Power MOSFETs

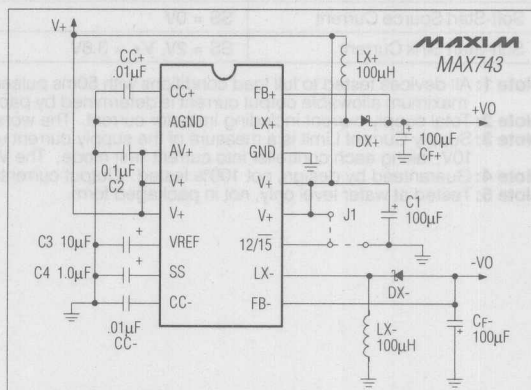
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX743CPE	0°C to +70°C	16 Plastic DIP
MAX743CWE	0°C to +70°C	16 Wide SO
MAX743C/D	0°C to +70°C	Dice
MAX 743EPE	-40°C to +85°C	16 Plastic DIP
MAX743EWE	-40°C to +85°C	16 Wide SO
MAX743MJE	-55°C to +125°C	16 CERDIP

Ordering information continued on page 3.

5

Typical Operating Circuit



Dual-Output, Switch-Mode Regulator (+5V to $\pm 15V$ or $\pm 12V$)

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $+4.5V < V+ < +5.5V$, Note 1.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage					
$\pm 15V$ Mode	$0mA < I_{LOAD} < 100mA$ $12/15 = 0V$	$T_A = +25^\circ C$		15.45	V
		$T_A = T_{MIN}$ to T_{MAX}		15.60	
$\pm 12V$ Mode	$0mA < I_{LOAD} < 125mA$ $12/15 = V+$	$T_A = +25^\circ C$		12.36	V
		$T_A = T_{MIN}$ to T_{MAX}		12.48	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V+ = +5.0V$, $12/15$ pin = $0V$, $I_{LOAD} = 0$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Efficiency	$I_{LOAD} = \pm 50mA$	$LX = MAXL001$	79		%
		$LX = MPP$ Toroid	82		
Supply Current (Note 2)			20	30	mA
Supply Current Limit (Note 3)	$+VO = +10V$			1.2	A
	$-VO = -10V$			1.2	
Standby Current	$V_{REF} = +5V$, includes V_{REF} current		2.2	4	mA
Line Regulation	$V+ = +4.5V$ to $+5.5V$.05	%/%
Load Regulation	$I_{LOAD} = 0$ to $100mA$			1	%
Reference Voltage	V_{REF}		2.0		V
Oscillator Frequency		180	200	220	kHz
Undervoltage Lock-out	Measured at $V+$	3.8		4.2	V
Thermal Shutdown Threshold			+190		$^\circ C$
$LX+$ On Resistance (Note 4)			1.2	3.0	Ω
$LX-$ On Resistance (Note 4)			1.0	2.2	Ω
$LX+$ Leakage Current (Note 5)	$LX+ = +17V$, $V+ = 6V$			100	μA
$LX-$ Leakage Current (Note 5)	$LX- = -17V$, $V+ = 6V$			-100	μA
Compensation Pin Impedance	$CC+$, $CC-$		10		k Ω
Soft-Start Source Current	$SS = 0V$	3.0		7.0	μA
Soft-Start Sink Current	$SS = 2V$, $V+ = 3.8V$	0.5	2.0		mA

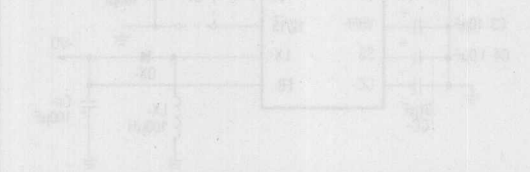
Note 1: All devices tested to full load conditions with 50ms pulsed loads using automatic test equipment. In continuous operation, the maximum allowable output current is determined by package thermal characteristics and passive component ratings.

Note 2: Total supply current including inductor current. The worst case for supply current occurs at low input voltage.

Note 3: Supply Current Limit is a measure of the supply current under overload conditions. One at a time, the outputs are forced to 10V, taking each controller into current limit mode. The $V+$ supply current is then measured.

Note 4: Guaranteed by design, not 100% tested. Output currents are 100% tested.

Note 5: Tested at wafer level only, not in packaged form.



Dual-Output, Switch-Mode Regulator (+5V to $\pm 15V$ or $\pm 12V$)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ or AV+ to GND)	+7V, -0.3V ($\pm 12V$ Mode) +6V, -0.3V ($\pm 15V$ Mode)
Output Switch Voltages (LX+ to GND) (LX- to V+)	+17V, -0.3V -23V, +0.3V
Output Switch Currents (LX+ Sink Current, Peak) (LX- Source Current, Peak)	2.0A -2.0A

Operating Temperature Range

MAX743C	0°C to +70°C
MAX743E	-40°C to +85°C
MAX743MJE	-55°C to +125°C
Junction Temperature	
MAX743E/C	+150°C
MAX743MJE	+175°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION - OBSERVE PROTOTYPING PRECAUTIONS BELOW

- DO NOT INSERT DEVICE INTO SOCKET WITH POWER APPLIED.
- BE CERTAIN THAT OUTPUT FILTER CAPACITORS ARE CONNECTED.
- DO NOT SOLDER OR WORK ON CIRCUIT WHILE POWER IS APPLIED.
- OBSERVE SUPPLY VOLTAGE RATINGS CAREFULLY.

Production Kit Ordering Information

Each kit contains a MAX743 IC and key external components. MAXL001 and MAXC001 can also be ordered individually.

PART	TEMP. RANGE	IC PACKAGE
MAX743CPEKIT	0°C to +70°C	Plastic DIP
MAX743EPEKIT	-25°C to +85°C	Plastic DIP

PRODUCTION KIT CONTENTS

PART	DESCRIPTION	QTY/KIT
MAX743	Integrated Circuit	1
1N5817	Schottky Rectifier	2
MAXC001	150 μ F Low ESR Capacitors	3
MAXL001	100 μ H Toroid Inductors	2

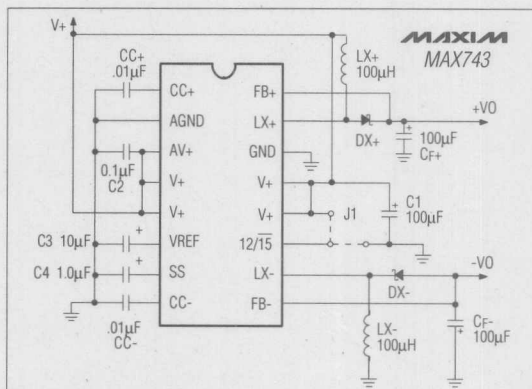


Figure 1. Basic Application Circuit

- Notes:** LX Inductors: MAXL001 or equivalent.
CF Filter Capacitors: MAXC001 or 100 μ F low-ESR equivalent.
C1 Bypass Capacitor: MAXC001 or 22 μ F 16V Tantalum or equivalent.
C4 Soft-Start Capacitor is optional.
DX Schottky Diodes: 1N5817 or equivalent.

MAX743

5

ADVANCE INFORMATION

FIRST PAGE OF DATA SHEET IN PREPARATION

MAXIM

High-Performance Supervisory Circuits

MAX790/MAX791

General Description

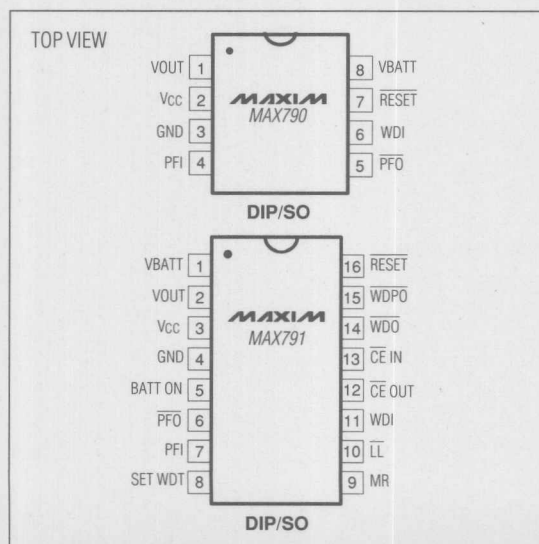
The MAX790/MAX791 supervisory circuits reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (μ P) systems. These include μ P reset, backup-battery switchover, watchdog timer, CMOS RAM write protection, and power-failure warning. The RESET output of the ICs is guaranteed to be in the correct state for VCC voltages down to 1V.

The MAX790/MAX791 offer several improvements over Maxim's MAX690 Series of supervisory circuits, including 70 μ A supply current, 10ns CE propagation delay, 250mA output current (VCC mode), and 25mA output current (VBATT mode). The MAX790 is pin compatible with the MAX690.

Applications

Computers
Controllers
Intelligent Systems
Automotive Systems
Critical μ P Power Monitoring

Pin Configurations



Features

- ◆ Precision 4.72V Monitor
- ◆ 250ms RESET VCC Assertion Time
- ◆ 1.6sec or Adjustable Watchdog Timeout Period
- ◆ Min Component Count
- ◆ 1 μ A Standby Current
- ◆ Monitors Backup Battery
- ◆ Battery-Backup Power Switching
- ◆ On-board Gating of Chip-Enable Signals

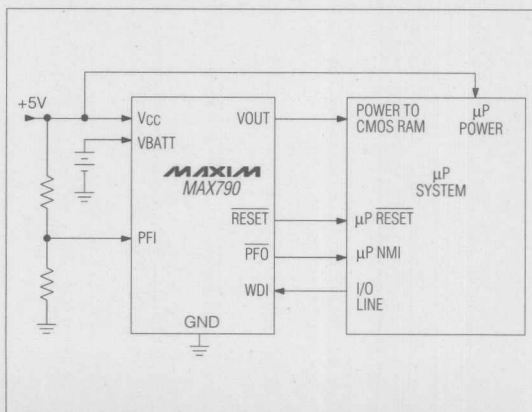
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX790CPA	0°C to +70°C	8 Plastic DIP
MAX790C/D	0°C to +70°C	Dice*
MAX790EPA	-40°C to +85°C	8 Plastic DIP
MAX790MJA	-55°C to +125°C	8 CERDIP
MAX791CPE	0°C to +70°C	16 Plastic DIP
MAX791CWE	-0°C to +70°C	16 Wide SO
MAX791C/D	0°C to +70°C	Dice*
MAX791EPE	-40°C to +85°C	16 Plastic DIP
MAX791EWE	-40°C to +85°C	16 Wide SO
MAX791MJE	-55°C to +125°C	16 CERDIP

*Consult factory for dice specifications.

5

Typical Operating Circuit



MAXIM

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Maxim Integrated Products 5-103



Interface

MAX230	+5V Powered, Five RS-232 Transmitters with Power Shutdown	6-1
MAX231	+5V and +12V Powered, Dual RS-232 Transmitters and Receivers	6-1
MAX232	+5V Powered, Dual RS-232 Transmitters and Receivers	6-1
MAX233	No External Component +5V Powered, Dual RS-232 Transmitters and Receivers	6-1
MAX234	+5V Powered, Quad RS-232 Transmitters	6-1
MAX235	No External Component +5V Powered, Five RS-232 Transmitters and Receivers with Power Shutdown and Receiver Three-State Enable	6-1
MAX236	+5V Powered, Four RS-232 Transmitters and Three RS-232 Receivers with Power Shutdown and Receiver Three-State Enable	6-1
MAX237	+5V Powered, Five RS-232 Transmitters and Three RS-232 Receivers	6-1
MAX238	+5V Powered, Quad RS-232 Transmitters and Receivers	6-1
MAX239	+5V and +12V Powered, Three RS-232 Transmitters and Five RS-232 Receivers with Three-State Receiver Enable	6-1
MAX240	+5V Powered, Five RS-232 Transmitters and Receivers with Power Shutdown and Receiver Three-State Enable in Plastic Flatpak	6-1
MAX241	+5V Powered, Four RS-232 Transmitters, Five Receivers with Power Shutdown and Receiver Three-State Enable in 28 Pin Small Outline	6-1
MAX250	+5V Powered Isolated RS-232 Driver/Receiver	6-17
MAX251	+5V Powered Isolated RS-232 Driver/Receiver	6-17
MAX252	Complete +5V- Powered Isolated Dual RS-232 Transceiver Module	6-29
RR-3A	Module Product Reliability Report	6-37

MAXIM

+5V Powered RS-232 Drivers/Receivers

MAX230-241*

General Description

Maxim's family of line drivers/receivers are intended for all RS-232 and V.28/V.24 communications interfaces, and in particular, for those applications where $\pm 12V$ is not available. The MAX230, MAX236, MAX240 and MAX241 are particularly useful in battery powered systems since their low power shutdown mode reduces power dissipation to less than $5\mu W$. The MAX233 and MAX235 use no external components and are recommended for applications where printed circuit board space is critical.

All members of the family except the MAX231 and MAX239 need only a single +5V supply for operation. The RS-232 drivers/receivers have on-board charge pump voltage converters which convert the +5V input power to the $\pm 10V$ needed to generate the RS-232 output levels. The MAX231 and MAX239, designed to operate from +5V and +12V, contain a +12V to -12V charge pump voltage converter.

Since nearly all RS-232 applications need both line drivers and receivers, the family includes both receivers and drivers in one package. The wide variety of RS-232 applications require differing numbers of drivers and receivers. Maxim offers a wide selection of RS-232 driver/receiver combinations in order to minimize the package count (see table below).

Both the receivers and the line drivers (transmitters) meet all EIA RS-232C and CCITT V.28 specifications.

Features

- ◆ Operates from Single 5V Power Supply (+5V and +12V — MAX231 and MAX239)
- ◆ Meets All RS-232C and V.28 Specifications
- ◆ Multiple Drivers and Receivers
- ◆ Onboard DC-DC Converters
- ◆ $\pm 9V$ Output Swing with +5V Supply
- ◆ Low Power Shutdown — $<1\mu A$ (typ)
- ◆ 3-State TTL/CMOS Receiver Outputs
- ◆ $\pm 30V$ Receiver Input Levels

Applications

Computers
Peripherals
Modems
Printers
Instruments

Selection Table

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Components	Low Power Shutdown /TTL 3-State	No. of Pins
MAX230	+5V	5	0	4 capacitors	Yes/No	20
MAX231	+5V and +7.5V to 13.2V	2	2	2 capacitors	No/No	14
MAX232	+5V	2	2	4 capacitors	No/No	16
MAX233	+5V	2	2	None	No/No	20
MAX234	+5V	4	0	4 capacitors	No/No	16
MAX235	+5V	5	5	None	Yes/Yes	24
MAX236	+5V	4	3	4 capacitors	Yes/Yes	24
MAX237	+5V	5	3	4 capacitors	No/No	24
MAX238	+5V	4	4	4 capacitors	No/No	24
MAX239	+5V and +7.5V to 13.2V	3	5	2 capacitors	No/Yes	24
MAX240	+5V	5	5	4 capacitors	Yes/Yes	44
MAX241	+5V	4	5	4 capacitors	Yes/Yes	28 (Flatpak) (Small Outline)

* Patent Pending

MAXIM

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Maxim Integrated Products 6-1

+5V Powered RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC}	-0.3V to +6V
V^+	($V_{CC} - 0.3V$) to +14V
V^-	+0.3V to -14V
Input Voltages	
T_{IN}	-0.3 to ($V_{CC} + 0.3V$)
R_{IN}	$\pm 30V$
Output Voltages	
T_{OUT}	($V^+ + 0.3V$) to ($V^- - 0.3V$)
R_{OUT}	-0.3V to ($V_{CC} + 0.3V$)

Short Circuit Duration

T_{OUT}	continuous
Power Dissipation	
CERDIP	675mW (derate 9.5mW/°C above +70°C)
Plastic DIP	375mW (derate 7mW/°C above +70°C)
Small Outline (SO)	375mW (derate 7mW/°C above +70°C)
Lead Temperature (soldering 10 seconds)	+300°C
Storage Temperature	-65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX232, 234, 236, 237, 238, 240, 241 $V_{CC} = 5V \pm 10\%$; MAX233, 235 $V_{CC} = 5V \pm 5\%$; MAX231, 239 $V_{CC} = 5V \pm 10\%$, $V^+ = 7.5V$ to 13.2V; T_A = Operating Temperature Range, Figures 3-14, unless otherwise noted.)

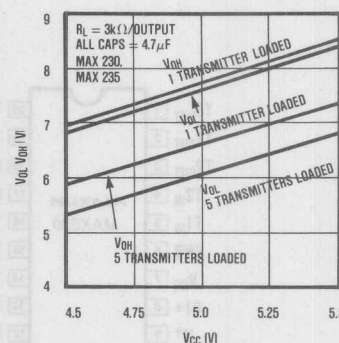
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage Swing	All Transmitter Outputs loaded with 3k Ω to Ground	± 5	± 9		V
V_{CC} Power Supply Current	No load, $T_A = +25^\circ C$		5	10	mA
	MAX231, MAX239		0.4	1	
V^+ Power Supply Current	No load, MAX231 and MAX239 only	MAX231	1.8	5	mA
		MAX239	5	15	
Shutdown Supply Current	Figure 1, $T_A = +25^\circ C$		1	10	μA
Input Logic Threshold Low	T_{IN} , \overline{EN} , Shutdown			0.8	V
Input Logic Threshold High	T_{IN}	2.0			V
	\overline{EN} , Shutdown	2.4			
Logic Pullup Current	$T_{IN} = 0V$		15	200	μA
RS-232 Input Voltage Operating Range		-30		+30	V
RS-232 Input Threshold Low	$V_{CC} = 5V$, $T_A = +25^\circ C$ (MAX231, 239 $V^+ = 0V$)	0.8	1.2		V
RS-232 Input Threshold High	$V_{CC} = 5V$, $T_A = +25^\circ C$ (MAX231, 239 $V^+ = 12V$)		1.7	2.4	V
RS-232 Input Hysteresis	$V_{CC} = 5V$	0.2	0.5	1.0	V
RS-232 Input Resistance	$T_A = +25^\circ C$, $V_{CC} = 5V$	3	5	7	k Ω
TTL/CMOS Output Voltage Low	$I_{OUT} = 1.6mA$ (MAX231-233, $I_{OUT} = 3.2mA$)			0.4	V
TTL/CMOS Output Voltage High	$I_{OUT} = -1.0mA$	3.5			V
TTL/CMOS Output Leakage Current	$\overline{EN} = V_{CC}$, $0V \leq R_{OUT} \leq V_{CC}$		0.05	± 10	μA
Output Enable Time (Figure 2)	MAX235, MAX236, MAX239, MAX240, 241		400		ns
Output Disable Time (Figure 2)	MAX235, MAX236, MAX239, MAX240, 241		250		ns
Propagation Delay	RS-232 to TTL		0.5		μs
Instantaneous Slew Rate	$C_L = 10pF$, $R_L = 3-7k\Omega$ $T_A = +25^\circ C$ (Note 1)			30	V/ μs
Transition Region Slew Rate	$R_L = 3k\Omega$, $C_L = 2500pF$ Measured from +3V to -3V or -3V to +3V		3		V/ μs
Output Resistance	$V_{CC} = V^+ = V^- = 0V$, $V_{OUT} = \pm 2V$	300			Ω
RS-232 Output Short Circuit Current			± 10		mA

Note 1: Sample tested.

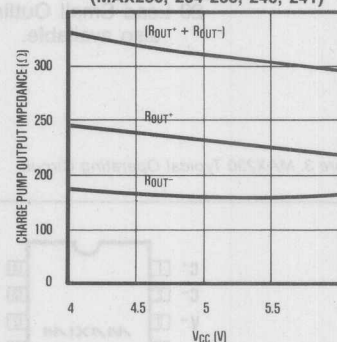
Typical Operating Characteristics

MAX230-241*

TRANSMITTER OUTPUT VOLTAGE vs: V_{CC} VOLTAGE



CHARGE PUMP OUTPUT IMPEDANCE
vs. V_{CC}
(MAX230, 234-238, 240, 241)



e

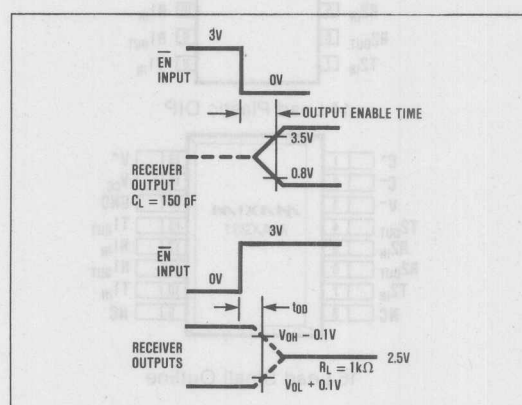
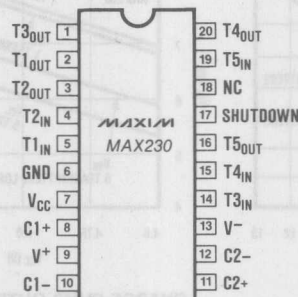


Figure 2. Receiver Output Enable and Disable Timing

+5V Powered RS-232 Drivers/Receivers



20 Lead Small Outline
also available.

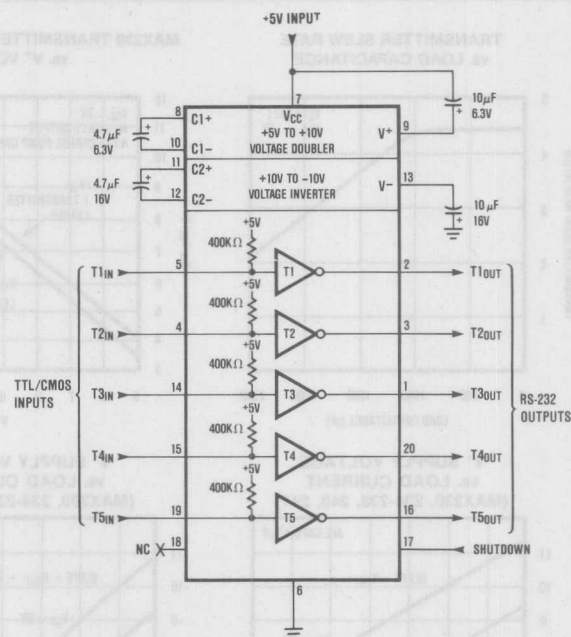
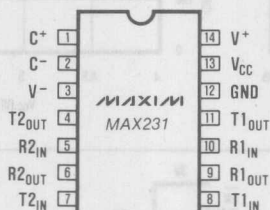
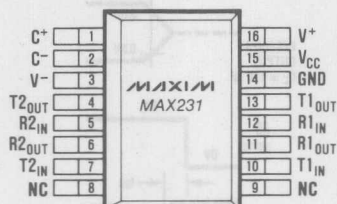


Figure 3. MAX230 Typical Operating Circuit



14 Lead Plastic DIP



16 Lead Small Outline

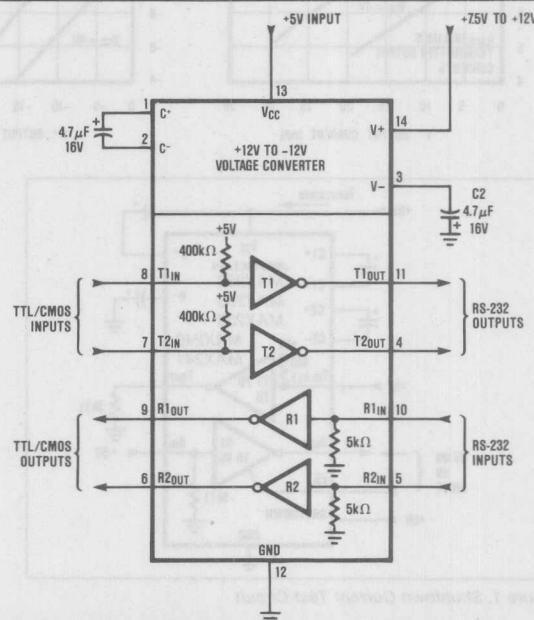
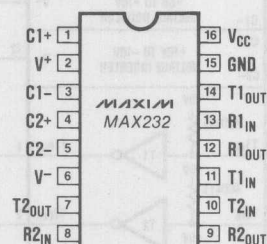


Figure 4. MAX231 Typical Operating Circuit

+5V Powered RS-232 Drivers/Receivers

MAX230-241*



16 Lead Small Outline
also available.

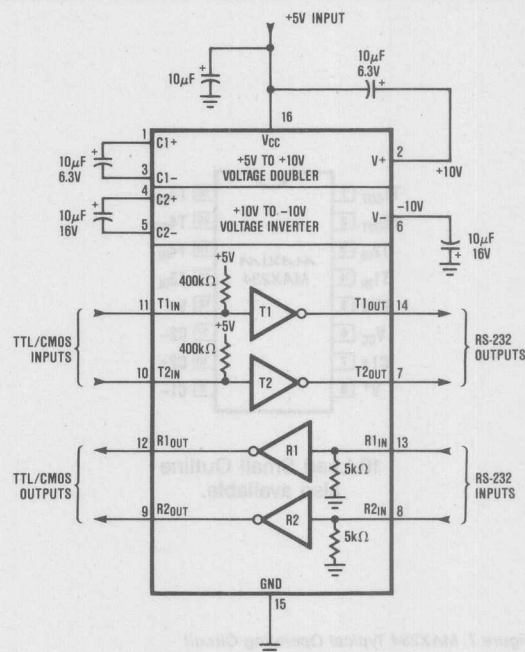
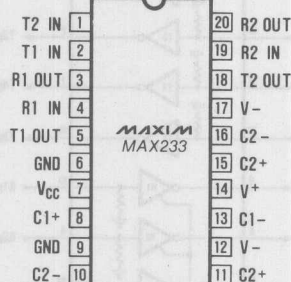


Figure 5. MAX232 Typical Operating Circuit



Small Outline Not Available

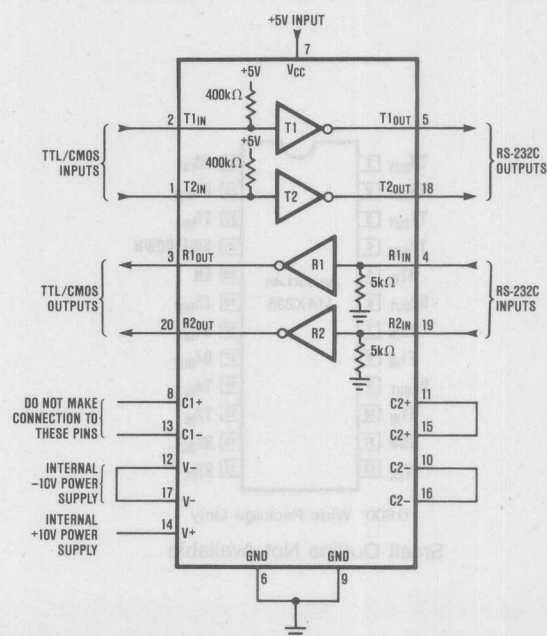
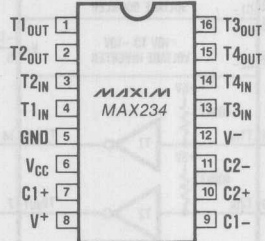


Figure 6. MAX233 Typical Operating Circuit

+5V Powered RS-232 Drivers/Receivers



16 Lead Small Outline
also available.

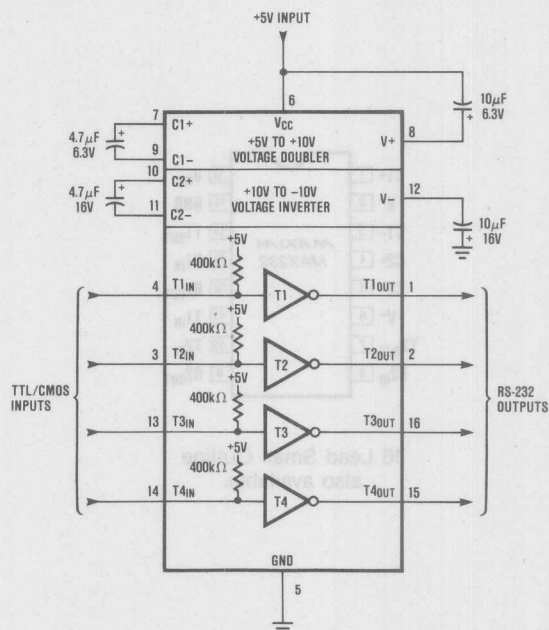
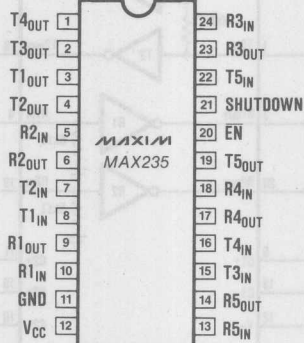


Figure 7. MAX234 Typical Operating Circuit



0.600" Wide Package Only
Small Outline Not Available

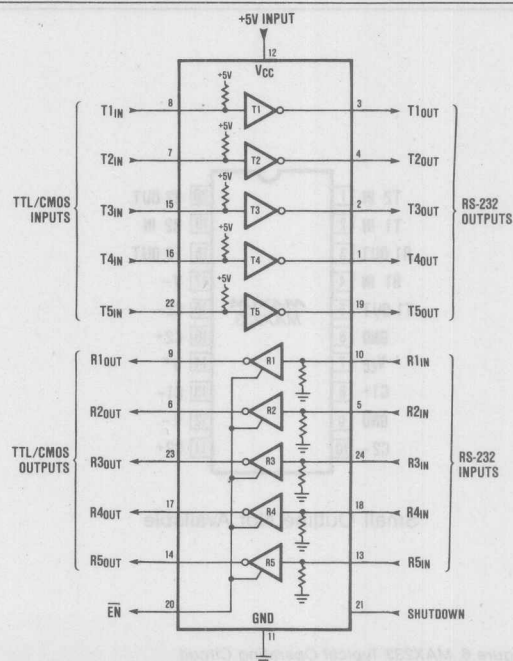
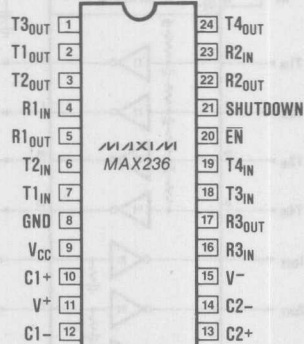


Figure 8. MAX235 Typical Operating Circuit

+5V Powered RS-232 Drivers/Receivers

MAX230-241*



24 Lead Small Outline
also available.

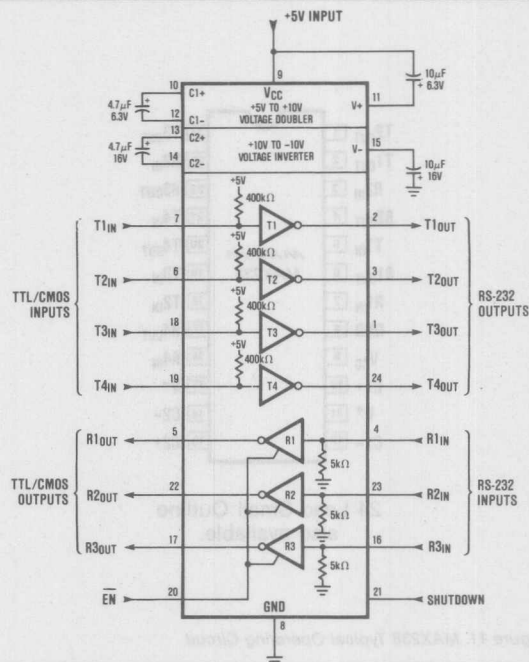
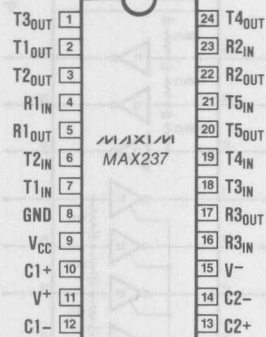


Figure 9. MAX236 Typical Operating Circuit



24 Lead Small Outline
also available.

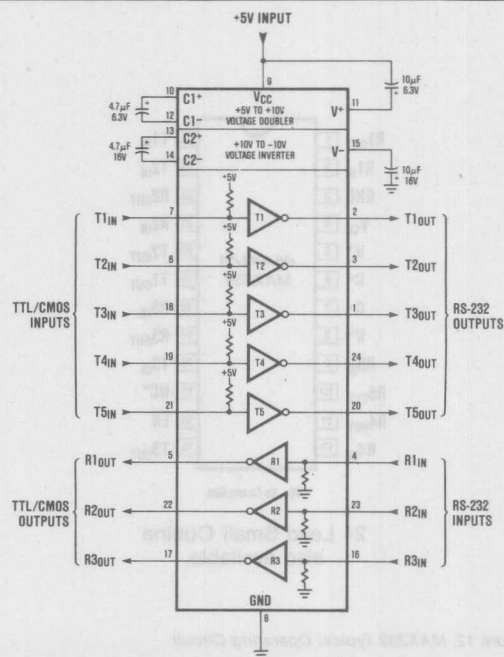
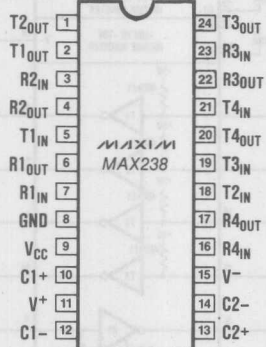


Figure 10. MAX237 Typical Operating Circuit

MAXIM

+5V Powered RS-232 Drivers/Receivers



24 Lead Small Outline
also available.

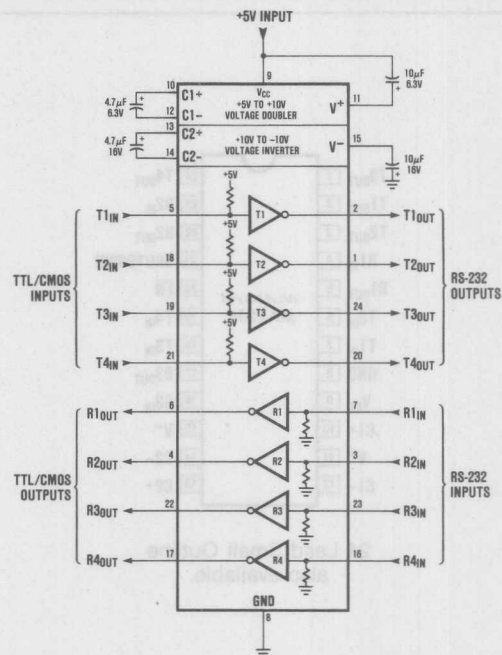
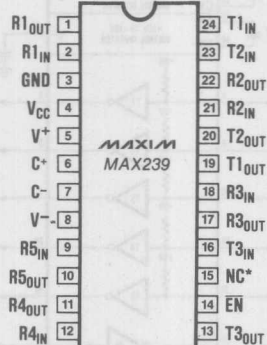


Figure 11. MAX238 Typical Operating Circuit



* NC - No Connection

24 Lead Small Outline
also available.

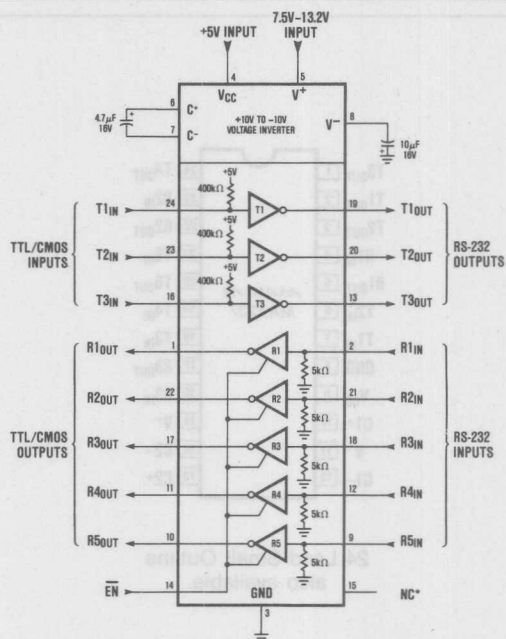
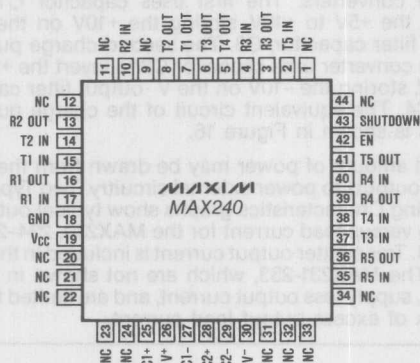


Figure 12. MAX239 Typical Operating Circuit

MAX230-241*



44 Lead Plastic Flatpak Only

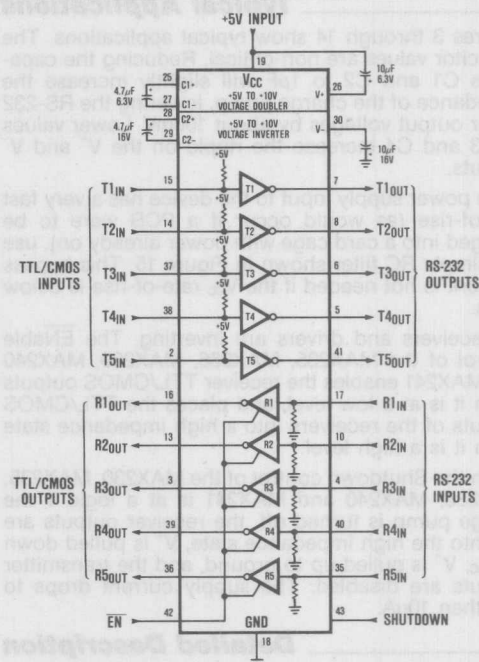
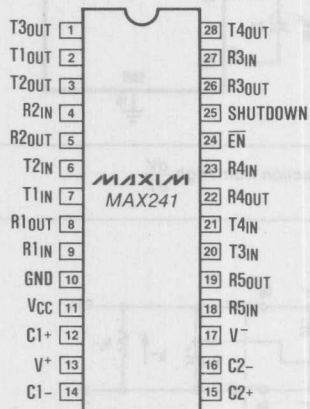
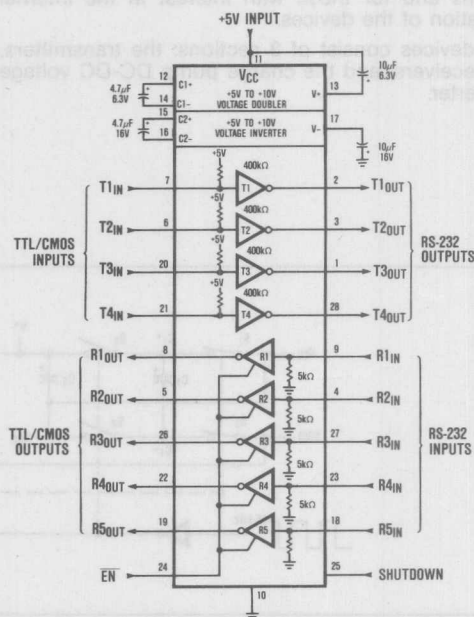


Figure 13. MAX240 Typical Operating Circuit.



28 Lead Wide Small Outline Only



+5V Powered RS-232 Drivers/Receivers

Typical Applications

Figures 3 through 14 show typical applications. The capacitor values are non-critical. Reducing the capacitors C1 and C2 to $1\mu\text{F}$ will slightly increase the impedance of the charge pump, lowering the RS-232 driver output voltages by about 100mV. Lower values of C3 and C4 increase the ripple on the V^+ and V^- outputs.

If the power supply input to the device has a very fast rate-of-rise (as would occur if a PCB were to be plugged into a card cage with power already on), use the simple RC filter shown in Figure 15. This bypass network is not needed if the V_{CC} rate-of-rise is below $1\text{V}/\mu\text{s}$.

All receivers and drivers are inverting. The $\overline{\text{ENable}}$ control of the MAX235, MAX236, MAX239, MAX240 and MAX241 enables the receiver TTL/CMOS outputs when it is at a low level, and places the TTL/CMOS outputs of the receivers into a high impedance state when it is at a high level.

When the Shutdown control of the MAX230, MAX235, MAX236, MAX240 and MAX241 is at a logic 1 the charge pump is turned off, the receiver outputs are put into the high impedance state, V^+ is pulled down to V_{CC} , V^- is pulled up to ground, and the transmitter outputs are disabled. The supply current drops to less than $10\mu\text{A}$.

Detailed Description

The following sections provide supplementary information for those designers with non-standard applications and for those with interest in the internal operation of the devices.

The devices consist of 3 sections: the transmitters, the receivers, and the charge pump DC-DC voltage converter.

+5V to $\pm 10\text{V}$

Dual Charge Pump Voltage Converter

All but the MAX231 and MAX239 convert +5V to $\pm 10\text{V}$. This conversion is performed by two charge pump voltage converters. The first uses capacitor C1 to double the +5V to +10V, storing the +10V on the V^+ output filter capacitor, C3. The second charge pump voltage converter uses capacitor C2 to invert the +10V to -10V, storing the -10V on the V^- output filter capacitor, C4. The equivalent circuit of the charge pump section is shown in Figure 16.

A small amount of power may be drawn from the V^+ and V^- outputs to power external circuitry. Two Typical Operating Characteristics graphs show typical output voltage versus load current for the MAX230, 234-238, and 241. Transmitter output current is included in these plots. The MAX231-233, which are not shown in the graphs, supply less output current, and are limited to 1 or 2mA of excess output load current.

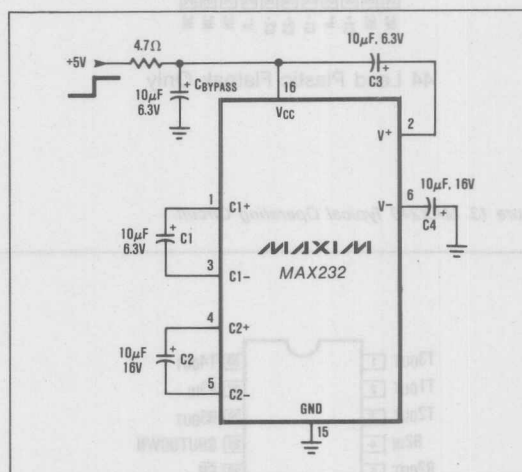


Figure 15. Protection from High $\frac{dV}{dT}$

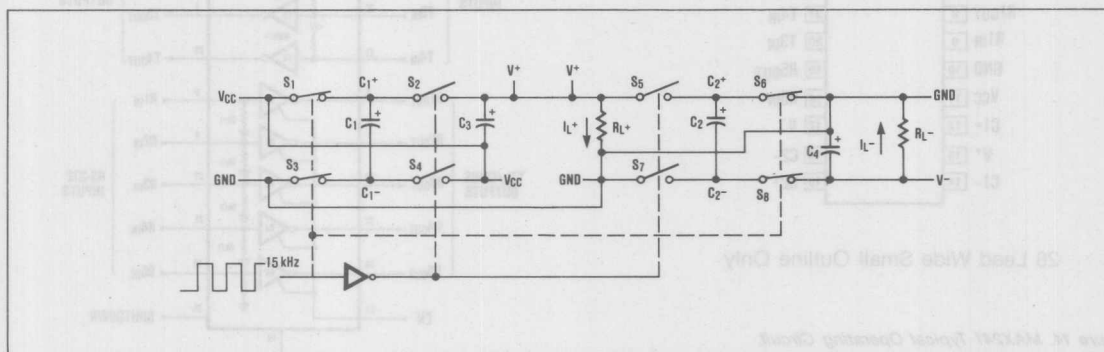


Figure 16. Charge Pump Diagram.

+5V Powered RS-232 Drivers/Receivers

MAX230-241*

For applications needing only the +5V to ± 10 V charge pump voltage converter, the MAX680 is available.

The capacitor values for C1 through C4 are non-critical. At the 15kHz typical switching frequency of the voltage converter, a $1\mu\text{F}$ capacitor has approximately 10Ω impedance, and replacing the $4.7\mu\text{F}$ and $10\mu\text{F}$ capacitors shown in the typical applications with $1\mu\text{F}$ for C1 and C2 will increase the output impedance of the V^+ output by about 10Ω and the output impedance of V^- by about 20Ω . Lowering the value of C3 and C4 increases the ripple on the V^+ and V^- outputs. Where operation to the upper temperature limit is not required, or V_{CC} will not go below 4.75V, C1 and C2 can be $1\mu\text{F}$, and C3 and C4 can be $1\mu\text{F}$ per output channel ($1\mu\text{F}$ if one transmitter is used, $5\mu\text{F}$ if five transmitters are used).

There are parasitic diodes which become forward biased if V^+ goes below V_{CC} or V^- goes above ground. When in the shutdown mode (MAX230, MAX235, MAX236, MAX240 and MAX241 only), V^+ is internally connected to V_{CC} by a $1\text{k}\Omega$ pulldown, and V^- is internally connected to ground via a $1\text{k}\Omega$ pullup.

The MAX233 and MAX235 contain all charge pump components, including the capacitors, and operate with NO external components.

The MAX231 and MAX239 include only the V^+ to V^- charge pump, and are intended for applications which have a +5V supply and either a $+12\text{V} \pm 10\%$ supply or a 7.5V to 13.2V battery voltage. When operating with V^+ greater than 8.0V, both capacitors can be $1\mu\text{F}$.

Driver (Transmitter) Section

The transmitters or line drivers are inverting level translators which convert the CMOS or TTL input levels to RS-232 or V.28 voltage levels. With +5V V_{CC} , the typical output voltage swing is $\pm 9\text{V}$ when loaded with the nominal $5\text{k}\Omega$ input resistance of an RS-232 receiver. The output swing is guaranteed to meet the RS-232/V.28 specification of $\pm 5\text{V}$ minimum output swing under the worst case conditions of all transmitters driving the $3\text{k}\Omega$ minimum allowable load impedance, $V_{CC} = 4.5\text{V}$, and maximum operating ambient temperature. The open circuit output voltage swing is from ($V^+ - 0.6\text{V}$) to V^- .

The input thresholds are both CMOS and TTL compatible, with a logic threshold of about 25% of V_{CC} . The inputs of unused drivers sections can be left unconnected; an internal $400\text{k}\Omega$ input pullup resistor to V_{CC} will pull the inputs high, forcing the unused transmitter outputs low. The input pullup resistors source about $12\mu\text{A}$, and the driver inputs should be driven high or open circuited to minimize power supply current in the shutdown mode.

When in the low power shutdown mode, the driver outputs are turned off and their leakage current is less than $1\mu\text{A}$ with the driver output pulled to ground. The driver output leakage remains less than $1\mu\text{A}$, even if the transmitter output is backdriven between 0V and ($V_{CC} + 6\text{V}$). Below -0.5V the transmitter is diode clamped to ground with $1\text{k}\Omega$ series impedance. The transmitter is also zener clamped to approximately $V_{CC} + 6\text{V}$, with a series impedance of $1\text{k}\Omega$. As required by the RS232 and V.28, the slew rate is limited to less than $30\text{V}/\mu\text{s}$. This limits the maximum usable baud rate to 19,200 baud.

Receiver Section

All but the MAX230 and MAX234 contain RS-232/V.28 receivers. These receivers convert the $\pm 5\text{V}$ to $\pm 15\text{V}$ RS-232 signals to 5V TTL/CMOS outputs. Since the RS-232C/V.28 specifications define a voltage level greater than +3V as a 0, the receivers are inverting. Maxim has set the guaranteed input thresholds of the receivers to 0.8V minimum and 2.4V maximum, which are significantly tighter than the -3.0V minimum and $+3.0\text{V}$ maximum required by the RS-232 and V.28 specifications. This allows the receivers to respond both to RS-232/V.28 levels and TTL level inputs. The receivers are protected against input overvoltage up to $\pm 30\text{V}$.

The 0.8V guaranteed lower threshold is important to ensure that the receivers will have a logic 1 output if the receiver is not being driven because the equipment containing the line driver is turned off or disconnected, or if the connecting cable has an open circuit or short circuit. In other words, the receiver implements Type 1 interpretation of fault conditions (§7 of V.28, §2.5 of RS-232C). While a 0V or even a -3V receiver threshold would be acceptable for the data lines, these lower thresholds would not give proper indication on the control lines such as DTR and DSR. The receivers, on the other hand, have a full 0.8V noise margin for detecting the power-down or cable-disconnected states.

The receivers have a hysteresis of approximately 0.5V, with a minimum guaranteed hysteresis of 200mV. This aids in obtaining clean output transitions, even with slow rise and fall time input signals with moderate amounts of noise and ringing. The propagation delays of the receivers are 350ns for negative-going input signals, and 650ns for positive-going input signals (see Typical Characteristics graphs).

The MAX239 has a receiver 3-state control line, and the MAX235, MAX236, MAX240 and MAX241 have both a receiver 3-state control line and a low power shutdown control. The receiver TTL/CMOS outputs are in a high impedance 3-state mode whenever the 3-state $\overline{\text{ENable}}$ line is high, and are also high impedance whenever the Shutdown control line is high.

+5V Powered RS-232 Drivers/Receivers

Review of EIA Standard RS-232-C and CCITT Recommendations V.28 and V.24

The most common serial interface between electronic equipment is the "RS232" interface. This serial interface has been found to be particularly useful for the interface between units made by different manufacturers since the voltage levels are defined by the EIA Standard RS-232-C and CCITT Recommendation V.28. The RS-232 specification also contains signal circuit definitions and connector pin assignments, while CCITT circuit definitions are contained in a separate document, Recommendation V.24. Originally intended to interface modems to computers and terminals, these standards have many signals which are not used for computer-to-computer or computer-to-peripheral communication.

Serial interfaces can be used with a variety of transmission formats. The most popular by far is the asynchronous format, generally at one of the standard baud rates of 300, 600, 1200, etc. The maximum recommended baud rate for RS-232 and V.28 is 20,000 baud, and the fastest commonly used baud rate is 19,200 baud. Asynchronous serial links use a variety of combinations of the number of data bits, what type (if any) of parity bit, and the number of stop bits. A typical combination is 7 data bits, even parity, and 1 stop bit.

RS232/V.28 physical links are also suitable for synchronous transmission protocols. These higher level protocols often use the standard RS-232C/V.28 voltage levels. Note that one type of physical link (such as RS-232/V.28 voltage levels) can be used for a variety of higher level protocols. Table 2 summarizes the voltage levels and other requirements of V.28 and RS-232.

Comparison of RS-232C/V.28 with other Standards

The other two most common serial interface specifications are the EIA RS423 and RS422/RS485 (CCITT recommendations V.10 and V.11). While the RS-232 or V.28/V.24 interface is the most common interface for communication between equipment made by different manufacturers, the RS423/V.10 interface and RS422/V.11 interfaces can operate at higher baud rates. In addition, the RS485 interface can be used for low cost local area networks.

The RS423 and V.10 interfaces are unbalanced or "single-ended" interfaces which use a differential receiver. This standard is intended for data signaling rates up to 100 kbit/s (100 kilobaud). It achieves this higher baud rate through more precise requirements

on the waveshape of the transmitters and through the use of differential receivers to compensate for ground potential variations between the transmitting and receiving equipment. With certain limitations, this interface is compatible with RS-232 and V.28. The limitations are:

- 1) less than 20,000 baud rate,
- 2) maximum cable lengths determined by RS-232 performance,
- 3) RS423/V.10 DTE and DCE signal return paths must be connected to the RS232/V.28 signal ground,
- 4) the RS-232 transmitter output voltages must be limited to $\pm 12V$, or additional protection must be provided for the RS423/V.10 receivers, and
- 5) not all RS232/V.28 receivers will show proper power-off detection of V.10 transmitter outputs.

Maxim's MAX230 and MAX232-MAX238, MAX240 and MAX241 meet restrictions 4 and 5 over the entire range of recommended operating conditions. The MAX231 and MAX239 meet restrictions 4 and 5 provided that the V^+ voltage is 12.5V or less.

The RS422, RS485, and V.11 interfaces are balanced double-current interchanges suitable for baud rates up to 10 Mbit/s. These interfaces are not compatible with RS-232 or V.28 voltage levels.

Application Hints

Operation at High Baud Rates

V.28 states that "the time required for the signal to pass through the transition region during a change in state shall not exceed 1 millisecond or 3 percent of the nominal element period on the interchange circuit, whichever is less." RS-232C allows the transition time to be 4 percent of the duration of a signal element. At 19,200 baud, the "nominal element period" is approximately $50\mu s$, of which 3 percent is $1.5\mu s$. Since the transition region is from $-3V$ to $+3V$, this means the V.28 slew rate would ideally be faster than $6V/1.5\mu s = 4V/\mu s$ at 19.2 kbaud and $2V/\mu s$ at 9600 baud. The RS-232 requirement is equivalent to $3V/\mu s$ at 19.2 kbaud, $1.5V/\mu s$ at 9600 baud, etc. The slew rate of the MAX230 series devices is about $3V/\mu s$ with the maximum recommended load of 2500pF. In practice, the effect of less than optimum slew rate is a distortion of the recovered data, where the 1's and 0's no longer have equal width. This distortion generally has negligible effect and the devices can be reliably used for 19.2 kbaud serial links when the cable capacitance is kept below 2500pF. With very low capacitance loading, the MAX230 and MAX234-239, MAX240 and MAX241 may even be used at 38.4 kbaud, since the typical slew rate is $5V/\mu s$ when loaded with 500pF in parallel with $5k\Omega$. Under no circumstance will the

+5V Powered RS-232 Drivers/Receivers

Non-Inverting Drivers and Receivers

Occasionally a non-inverting driver or receiver is needed instead of the inverting drivers and receivers of the family. Simply use one of the receivers as a TTL/CMOS inverter to get the desired operation (Figure 17). If the logic output driving the receiver input has less than 1mA of output source capability, then add the 2.2k Ω pullup resistor.

The receiver TTL outputs can directly drive the input of another receiver to form a non-inverting RS-232 receiver.

Protection for Shorts to $\pm 15V$ Supplies

All driver outputs except on the MAX231, MAX232 and MAX233 are protected against short circuits to $\pm 15V$, which is the maximum allowable loaded output voltage of an RS-232/V.28 transmitter. The MAX231, MAX232, and MAX233 can be protected against short circuits to $\pm 15V$ power supplies by the addition of a series 220 Ω resistor in each output. This protection is not needed to protect against short circuits to most RS-232 transmitters such as the 1488, since they have an internal short circuit current limit of 12mA.

The power dissipation of the MAX230 and MAX234-MAX239, MAX240 and MAX241 is about 200mW with all transmitters shorted to $\pm 15V$.

Isolated RS-232 Interfaces

RS-232 and V.28 specifications require a common ground connection between the two units communicating via the RS-232/V.28 interface. In some cases, there may be large differences in ground potential between the two units, and in other cases it may be desired to avoid ground loop currents by isolating the two grounds. In other cases, a computer or control system must be protected against accidental connection of the RS-232/V.28 signal lines to 110/220VAC power lines. Figure 18 shows a circuit with this isolation. The power for the MAX233 is generated by a MAX635 DC-DC converter. When the MAX635 regulates point "A" to -5V, the isolated output at point "B" will be semi-regulated to +5V. The two optocouplers maintain isolation between the system ground and the RS-232 ground while transferring the data across the isolation barrier. While this circuit will not withstand 110VAC between the RS-232 ground and either the receiver or transmitter lines, the voltage difference between the two grounds is only limited by the optocoupler and DC-DC converter transformer breakdown ratings.

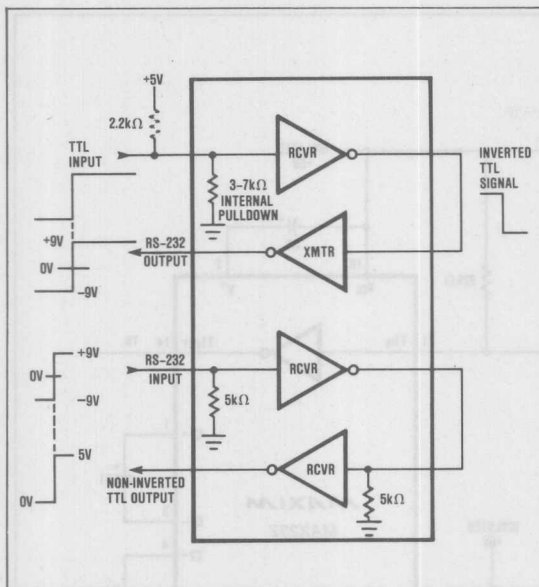


Figure 17. Non-inverting RS-232 Transmitters and Receivers.

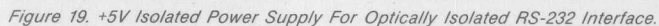
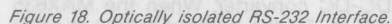
slew rate exceed the RS-232/V.28 maximum spec of 30V/ μ s and, unlike the 1488 driver, no external compensation capacitors are needed under any load condition.

Driving Long Cables

The RS-232 standard states that "The use of short cables (each less than approximately 50 feet or 15 meters) is recommended; however, longer cables are permissible, provided that the load capacitance . . . does not exceed 2500pF."

Baud rate and cable length can be traded off: use lower baud rates for long cables, use short cables if high baud rates are desired. For both long cables and high baud rates, use RS422/V.11. The maximum cable length for a given baud rate is determined by several factors, including the capacitance per meter of cable, the slew rate of the driver under high capacitive loading, the receiver threshold and hysteresis, and the acceptable bit error rate. The receivers have 0.5V of hysteresis, and the drivers are designed such that the slew rate reduction caused by capacitive loading is minimized (see Typical Characteristics).

MAX230-241*



+5V Powered RS-232 Drivers/Receivers

Ordering Information

MAX230-241*

PART	TEMP. RANGE	PACKAGE
MAX230		0.3" Wide
MAX230CPP	0°C to +70°C	20 Lead Plastic DIP
MAX230CWP	0°C to +70°C	20 Lead Wide S.O.
MAX230C/D	0°C to +70°C	Dice
MAX230EPP	-40°C to +85°C	20 Lead Plastic DIP
MAX230EWP	-40°C to +85°C	20 Lead Wide S.O.
MAX230EJP	-40°C to +85°C	20 Lead CERDIP
MAX230MJP	-55°C to +125°C	20 Lead CERDIP
MAX231		0.3" Wide
MAX231CPD	0°C to +70°C	14 Lead Plastic DIP
MAX231CWE	0°C to +70°C	16 Lead Wide S.O.
MAX231C/D	0°C to +70°C	Dice
MAX231EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX231EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX231EJD	-40°C to +85°C	14 Lead CERDIP
MAX231MJD	-55°C to +125°C	14 Lead CERDIP
MAX232		0.3" Wide
MAX232CPE	0°C to +70°C	16 Lead Plastic DIP
MAX232CWE	0°C to +70°C	16 Lead Wide S.O.
MAX232C/D	0°C to +70°C	Dice
MAX232EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX232EJE	-40°C to +85°C	16 Lead CERDIP
MAX232EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX232MJE	-55°C to +125°C	16 Lead CERDIP
MAX233		0.3" Wide
MAX233CPP	0°C to +70°C	20 Lead Plastic DIP
MAX233EPP	-40°C to +85°C	20 Lead Plastic DIP
MAX234		0.3" Wide
MAX234CPE	0°C to +70°C	16 Lead Plastic DIP
MAX234CWE	0°C to +70°C	16 Lead Wide S.O.
MAX234C/D	0°C to +70°C	Dice
MAX234EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX234EWE	-40°C to +85°C	16 Lead Wide S.O.
MAX234EJE	-40°C to +85°C	16 Lead CERDIP
MAX234MJE	-55°C to +125°C	16 Lead CERDIP
MAX235		0.6" Wide
MAX235CPG	0°C to +70°C	24 Lead Plastic DIP*
MAX235EPG	-40°C to +85°C	24 Lead Plastic DIP*
MAX235EDG	-40°C to +85°C	24 Lead Ceramic*
MAX235MDG	-55°C to +125°C	24 Lead Ceramic*

* = 0.600" package

PART	TEMP. RANGE	PACKAGE
MAX236		0.3" Wide
MAX236CNG	0°C to +70°C	24 Lead Plastic DIP
MAX236CWG	0°C to +70°C	24 Lead Wide S.O.
MAX236C/D	0°C to +70°C	Dice
MAX236ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX236EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX236ERG	-40°C to +85°C	24 Lead CERDIP
MAX236MRG	-55°C to +125°C	24 Lead CERDIP
MAX237		0.3" Wide
MAX237CNG	0°C to +70°C	24 Lead Plastic DIP
MAX237CWG	0°C to +70°C	24 Lead Wide S.O.
MAX237C/D	0°C to +70°C	Dice
MAX237ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX237EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX237ERG	-40°C to +85°C	24 Lead CERDIP
MAX237MRG	-55°C to +125°C	24 Lead CERDIP
MAX238		0.3" Wide
MAX238CNG	0°C to +70°C	24 Lead Plastic DIP
MAX238CWG	0°C to +70°C	24 Lead Wide S.O.
MAX238C/D	0°C to +70°C	Dice
MAX238ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX238EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX238ERG	-40°C to +85°C	24 Lead CERDIP
MAX238MRG	-55°C to +125°C	24 Lead CERDIP
MAX239		0.3" Wide
MAX239CNG	0°C to +70°C	24 Lead Plastic DIP
MAX239CWG	0°C to +70°C	24 Lead Wide S.O.
MAX239C/D	0°C to +70°C	Dice
MAX239ENG	-40°C to +85°C	24 Lead Plastic DIP
MAX239EWG	-40°C to +85°C	24 Lead Wide S.O.
MAX239ERG	-40°C to +85°C	24 Lead CERDIP
MAX239MRG	-55°C to +125°C	24 Lead CERDIP
MAX240		Flatpak
MAX240CMH	0°C to +70°C	44 Lead Flatpak
MAX240EMH	-40°C to +85°C	44 Lead Flatpak
MAX241		0.3" Wide
MAX241CWI	0°C to +70°C	28 Lead Wide S.O.
MAX241EWI	-40°C to +85°C	28 Lead Wide S.O.

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+5V Powered RS-232 Drivers/Receivers

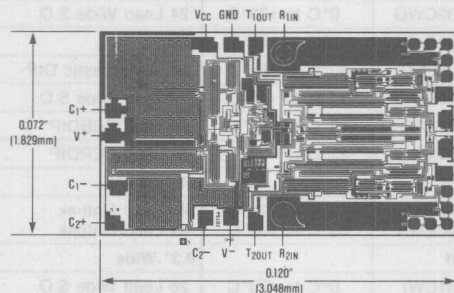
Table 1. Circuits Commonly Used for RS-232C and V.24 Asynchronous Interfaces

PIN	CIRCUIT	
1	Protective Ground	Connect to Earth Ground
2	Transmit Data (TD)	Data from DTE
3	Receive Data (RD)	Data from DCE
4	Request To Send (RTS)	Handshake from DTE
5	Clear to Send (CTS)	Handshake from DCE
6	Data Set ready (DSR)	Handshake from DCE
7	Signal Ground	Reference Point for Signals
8	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
11	Printer Busy Signal	Handshake from Printer
20	Data Terminal Ready	Handshake from DTE
22	Ring Indicator	Handshake from DCE

Table 2. Summary of RS-232C and V.28 Electrical Specifications

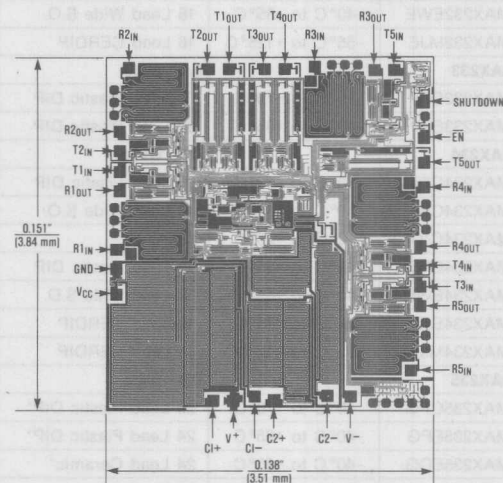
PARAMETER	SPECIFICATION	COMMENTS
Driver Output Voltage		
0 level	+5V to +15V	With 3-7k Ω load
1 level	-5V to -15V	With 3-7k Ω load
Max. output	$\pm 25V$ Max.	No Load
Receiver Input Thresholds (data and clock signals)		
0 level	+3V to +25V	
1 level	-3V to -25V	
Receiver Thresholds RTS, DSR, DTR		
On level	+3V to +25V	
Off level	Open Circuit or -3V to -25V	Detects Power Off Condition at Driver
Receiver Input Resistance	3k Ω to 7k Ω	
Driver Output Resistance, power off condition	300 Ω Min.	$V_{OUT} < \pm 2V$
Driver Slew Rate	30V/ μs Max.	3k $\Omega < R_L < 7k\Omega$; 0pF $< C_L < 2500pF$
Signalling Rate	Up to 20kbits/sec.	
Cable Length	50'/15 m. Recommended Max. Length	Longer cables permissible, if $C_{LOAD} \leq 2500pF$

Chip Topography



MAX231, MAX232 and MAX233

Note: Connect substrate to V⁺.



MAX230 and MAX234-239, MAX240, MAX241

Notes:

1. Shutdown pin of MAX234, MAX237, MAX238, MAX239, MAX240 and MAX241 are internally connected to ground.
2. Connect substrate to V⁺.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

+5V Powered Isolated RS-232 Drivers/Receivers

General Description

The MAX250 and MAX251 chip set form the heart of a complete, electrically isolated, RS-232 dual transmitter/receiver. By combining many functions on two chips, the cost and complexity required for an isolated digital interface is greatly reduced. Four low cost optocouplers, four capacitors, a diode and a small pot-core type transformer are all that are required to complete a 19.2k baud transceiver. Faster data rates are possible by using high speed optocouplers. In addition to the driving and receiving circuitry for the optocouplers, the chip set includes a push-pull transformer driver to supply power to the interface's isolated side.

Other convenient features include single +5V operation, a low power shutdown mode, and output enable control for three-state operation. The MAX250 and MAX251 are supplied in 14 lead DIP, 14 lead small outline and 20 leadless chip carrier packages.

The MAX252 has all the required components for RS-232 communication in a single package.

Applications

High Noise Data Communications
Industrial Communications
Data Links To Analog Circuits
Bridge Ground Differentials

Features

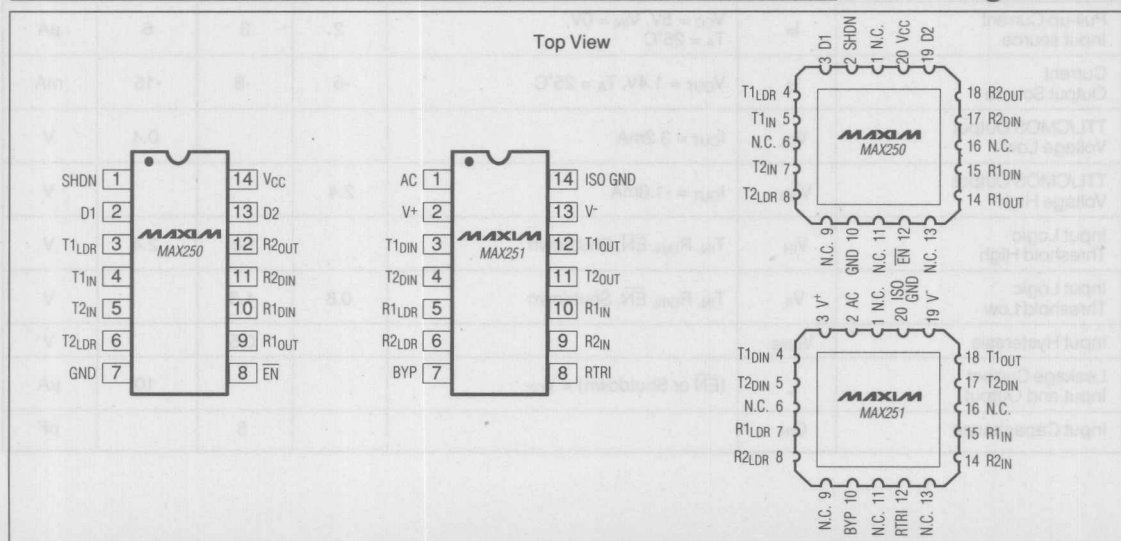
- ◆ Isolated Data Interface
- ◆ Single +5V Supply
- ◆ Uses Low Cost Optocouplers
- ◆ 5μW Low Power Shutdown
- ◆ 2 Transmitters and 2 Receivers

Ordering Information

PART	TEMP. RANGE	PACKAGE*
MAX250CPD	0°C to +70°C	14 Lead Plastic DIP
MAX250CSD	0°C to +70°C	14 Lead SO
MAX250C/D	0°C to +70°C	Dice
MAX250EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX250ESD	-40°C to +85°C	14 Lead SO
MAX250EJD	-40°C to +85°C	14 Lead Cerdip
MAX250MJD	-55°C to +125°C	14 Lead Cerdip
MAX250MLP	-55°C to +125°C	20 Lead LCC
MAX251CPD	0°C to +70°C	14 Lead Plastic DIP
MAX251CSD	0°C to +70°C	14 Lead SO
MAX251C/D	0°C to +70°C	Dice
MAX251EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX251ESD	-40°C to +85°C	14 Lead SO
MAX251EJD	-40°C to +85°C	14 Lead Cerdip
MAX251MJD	-55°C to +125°C	14 Lead Cerdip
MAX251MLP	-55°C to +125°C	20 Lead LCC

* Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.

Pin Configurations



MAXIM

Maxim Integrated Products 6-17

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+5V Powered Isolated RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS: MAX250

Supply Voltage, V_{CC} 6V
 Input Voltages -0.3V to ($V_{CC} + 0.3V$)
 Output Drive Current, D1, D2 240mA
 Output Drive Voltage, D1, D2 $V_{CC} + 6V$
 Opto Driver pins T1_{DR}, T2_{DR}, R1_{OUT} and R2_{OUT} may be
 shorted one at a time indefinitely to V_{CC} or GND

Power Dissipation
 Plastic DIP (derate 7mW/°C above 70°C) 375mW
 CERDIP (derate 9.5mW/°C above 70°C) 675mW
 Small Outline (derate 7mW/°C above 70°C) 375mW
 LCC (derate 7mW/°C above 70°C) 375mW
 Lead Temperature (Soldering, 10 seconds) +300°C
 Storage Temperature -65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX250

($V_{CC} = 5V \pm 10\%$, T_A = Full Temperature Range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Over Temp.	4.5		5.5	V
Operating Supply Current	I_{CC}	D1, D2 Open		0.1	0.5	mA
Shutdown Supply Current	I_{CS}	Shutdown $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		1	10 100	μA
Input Currents	I_{EN} , I_{SHDN}	Input = GND to V_{CC}		0.001	1	μA
POWER DRIVER D1, D2						
Switch Frequency	$f_{D1, D2}$	$V_{CC} = 5V$, $T_A = 25^\circ\text{C}$	100	200	275	kHz
ON Resistance Power Driver	$r_{DS(ON)}$	At 25 mA		25	50	Ω
Leakage Current					10	μA
Zener Clamp Voltage	V_{CL}	w. r. t. V_{CC}	6	8	10	V
DRIVER SECTION						
Pull-up Current Input source	I_P	$V_{CC} = 5V$, $V_{IN} = 0V$, $T_A = 25^\circ\text{C}$	2	3	6	μA
Current Output Source	I_S	$V_{OUT} = 1.4V$, $T_A = 25^\circ\text{C}$	-5	-8	-15	mA
TTL/CMOS Output Voltage Low	V_{OL}	$I_{OUT} = 3.2mA$			0.4	V
TTL/CMOS Output Voltage High	V_{OH}	$I_{OUT} = -1.0mA$	2.4			V
Input Logic Threshold High	V_{IH}	T_{IN} , R_{DIN} , \overline{EN} , Shutdown		1.8	2.4	V
Input Logic Threshold Low	V_{IL}	T_{IN} , R_{DIN} , \overline{EN} , Shutdown	0.8	1.3		V
Input Hysteresis	V_{IHYS}			0.5		V
Leakage Current Input and Output	I_L	(\overline{EN} or Shutdown) = V_{CC}			10	μA
Input Capacitance	C_{IN}			5		pF

+5V Powered Isolated RS-232 Drivers/Receivers

MAX250/MAX251

ABSOLUTE MAXIMUM RATINGS: MAX251

Positive Input Voltage, AC terminal	15V	Diode Forward Current (AC to V ⁺)	250mA
Positive Input Voltage, V ⁺ terminal	14V	Reverse Diode Voltage	-28V
Negative Input Voltage, V ⁻ terminal	-14V	Power Dissipation	
RS-232 Input Voltage	-30V to 30V	Plastic DIP (derate 7mW/°C above 70°C)	375mW
RS-232 Applied Output Voltage	-15V to 15V	CERDIP (derate 9.5mW/°C above 70°C)	675mW
Tristate Input Voltage, V _{TRI}	-0.3V to (V ⁺ + 0.3V)	Small Outline (derate 7mW/°C above 70°C)	375mW
RS-232 Transmitters may be indefinitely shorted to GND		LCC (derate 7mW/°C above 70°C)	375mW
Opto Driver pins R1 _{LDR} , R2 _{LDR} may be shorted one at a time indefinitely to GND		Lead Temperature (Soldering, 10 seconds)	+300°C
		Storage Temperature	-65°C to +160°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX251

(Test Circuit 1, See Figure 3, T_A = Full Temperature Range unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current	I ⁺	R _L = ∞		0.7	2.5	mA
Negative Supply Current	I ⁻	R _L = ∞		0.45	1.0	mA
RS-232 CHARACTERISTICS						
RS-232 Output Voltage Swing	T _{VS}	All Transmitter Outputs loaded with 3kΩ to Ground	±5	±7.2		V
RS-232 Output Leakage Current	T _{OL}	V ⁺ = V ⁻ = 0V T _{OUT} = ±15V	-10		+10	μA
RS-232 Input Threshold High	V _{IH}			1.8	3.0	V
RS-232 Input Threshold Low	V _{IL}		0.6	1.2		V
RS-232 Input Hysteresis	V _{IHYS}			0.6		V
RS-232 Input Resistance		T _A = 25°C	3		7	kΩ
3-State Enable	t _{EN}			3.5		μs
3-State Disable	t _{DS}			1.0		μs
Transmitter Slew Rate		R _L = 3kΩ, C _L = 2500pF	3			V/μs
OPTOINTERFACE CHARACTERISTICS						
Input Pull-up Current	I _P	T _A = 25°C	2.5	4	6	μA
Input Pull-up Voltage Clamp	V _{PCL}	w. r. t. ISO GND		3		V
Input Threshold Voltage High	V _{IH}			1.5	2	V
Input Threshold Voltage Low	V _{IL}		0.8	1.2		V
Input Hysteresis Voltage	V _{IHYS}			0.3		V

+5V Powered Isolated RS-232 Drivers/Receivers

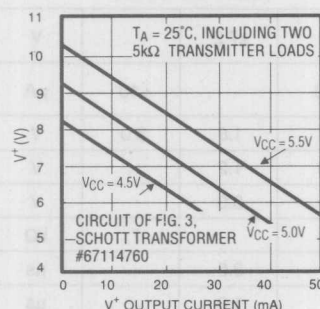
ELECTRICAL CHARACTERISTICS: MAX251 (continued)

(Test Circuit 1, See Figure 3, T_A = Full Temperature Range unless otherwise noted.)

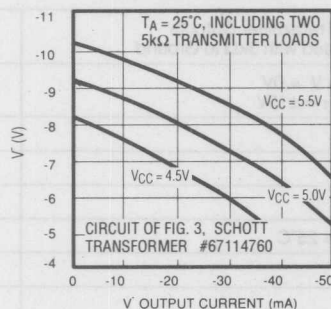
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Source Current	I_{PH}	$V_{OUT} = 1.4V$, $T_A = 25^\circ C$	-12	-7	-5	mA
Output Voltage Low	V_{OL}	$I_{OUT} = 3.2mA$			0.4	V
Output Leakage Current, $R1_{LDR}$, $R2_{LDR}$	I_L	(RTRI or Shutdown) = +5V			10	μA
3-STATE CONTROL						
Pulldown Current	I_{TPD}	$V = GND$	10	4	1	μA
Threshold Voltage	V_T		0.6	1.4	2	V

Typical Operating Characteristics

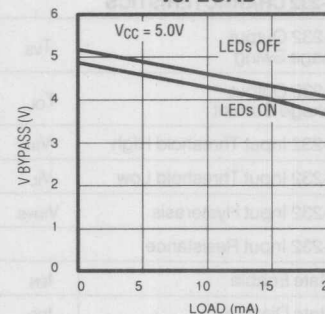
**MAX251 V^+ SUPPLY
VOLTAGE vs.
LOAD CURRENT**



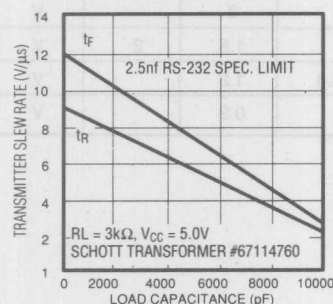
**MAX251 V^- SUPPLY
VOLTAGE vs.
LOAD CURRENT**



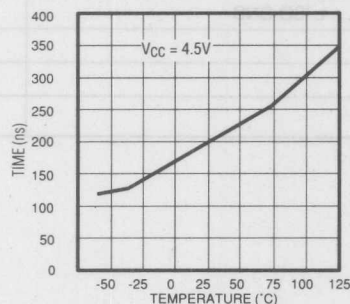
**MAX251 V^- BYPASS
VOLTAGE vs. LOAD**



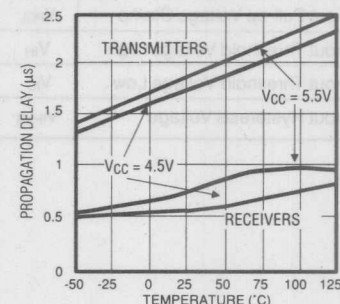
**MAX251 TRANSMITTER
SLEW RATE
vs. LOAD CAPACITANCE**



**MAX250 PROPAGATION
DELAY vs. TEMPERATURE**



**MAX251 PROPAGATION
DELAY vs. TEMPERATURE**

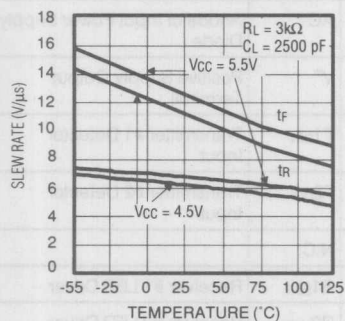


+5V Powered Isolated RS-232 Drivers/Receivers

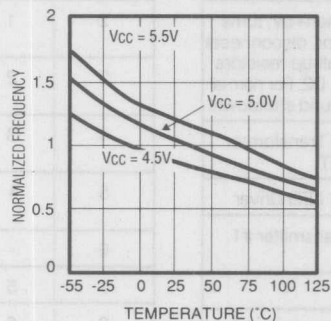
Typical Operating Characteristics (continued)

MAX250/MAX251

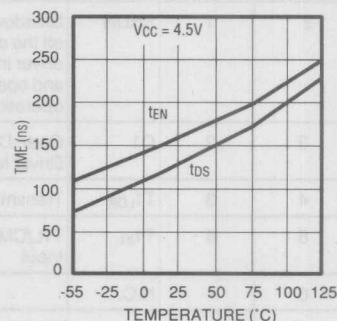
MAX251 TRANSMITTER
SLEW RATE
vs. TEMPERATURE



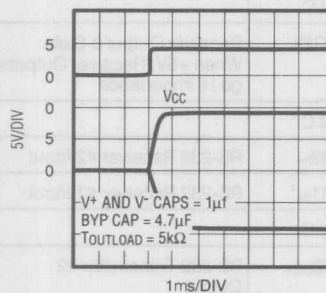
MAX250 D1, D2
SWITCH FREQUENCY
vs. TEMPERATURE



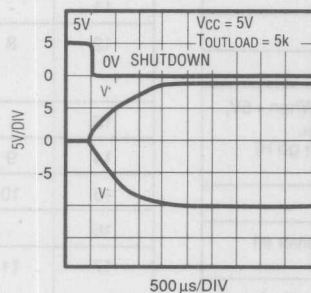
MAX250 ENABLE,
DISABLE TIME
vs. TEMPERATURE



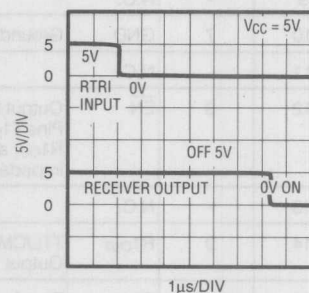
POWER UP DELAY FROM
MAX250 V_{CC} TO MAX251
TRANSMITTER OUTPUTS



TIME FROM SHUTDOWN
TO POWER UP



RTRI DELAY TIME
TO RECEIVER
OUTPUT ACTIVE



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+5V Powered Isolated RS-232 Drivers/Receivers

Pin Description

MAX250 LCC PIN#	MAX250 DIP & SO PIN#	SYMBOL	DESCRIPTION
1	-	N.C.	
2	1	SHDN	Shutdown: When +5V, turns off the oscillator, disconnects driver input pull-up resistors and opens D1, D2. For normal operation, ground shutdown.
3	2	D1	Open Drain of Transformer Driver MOSFET
4	3	T1 _{LDR}	Transmitter #1 LED Driver
5	4	T1 _{IN}	TTL/CMOS Transmitter #1 Input
6	-	N.C.	
7	5	T2 _{IN}	TTL/CMOS Transmitter #2 Input
8	6	T2 _{LDR}	Transmitter #2 LED Driver
9	-	N.C.	
10	7	GND	Ground
11	-	N.C.	
12	8	$\overline{\text{EN}}$	Output Enable: When +5V, Pins T1 _{LDR} , T2 _{LDR} , R1 _{OUT} and R2 _{OUT} go Hi impedance
13	-	N.C.	
14	9	R1 _{OUT}	TTL/CMOS Receiver #1 Output
15	10	R1 _{DIN}	Receiver #1 Detector Input
16	-	N.C.	
17	11	R2 _{DIN}	Receiver #2 Detector Input
18	12	R2 _{OUT}	TTL/CMOS Receiver #2 Output
19	13	D2	Open Drain of Transformer Driver MOSFET
20	14	V _{CC}	+5V Positive Supply Voltage

MAX251 LCC PIN#	MAX251 DIP & SO PIN#	SYMBOL	DESCRIPTION
1	-	N.C.	
2	1	AC	Anode of Input Power Supply Diode
3	2	V ⁺	Positive Supply Output Terminal
4	3	T1 _{DIN}	Transmitter #1 Detector Input
5	4	T2 _{DIN}	Transmitter #2 Detector Input
6	-	N.C.	
7	5	R1 _{LDR}	Receiver #1 LED Driver
8	6	R2 _{LDR}	Receiver #2 LED Driver
9	-	N.C.	
10	7	BYP	Internal V _{CC} Bypass Point
11	-	N.C.	
12	8	RTRI	Receiver Output 3-State: When +5V, Receiver Outputs go Hi impedance
13	-	N.C.	
14	9	R2 _{IN}	RS-232 Receiver #2 Input
15	10	R1 _{IN}	RS-232 Receiver #1 Input
16	-	N.C.	
17	11	T2 _{OUT}	RS-232 Transmitter #2 Output
18	12	T1 _{OUT}	RS-232 Transmitter #1 Output
19	13	V ⁻	Negative Supply Output Voltage
20	14	ISO GND	Isolated Ground

+5V Powered Isolated RS-232 Drivers/Receivers

MAX250/MAX251

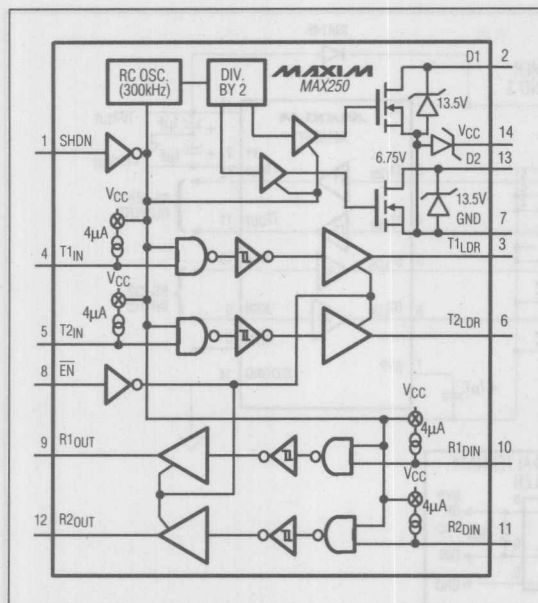


Figure 1. MAX250 Block Diagram

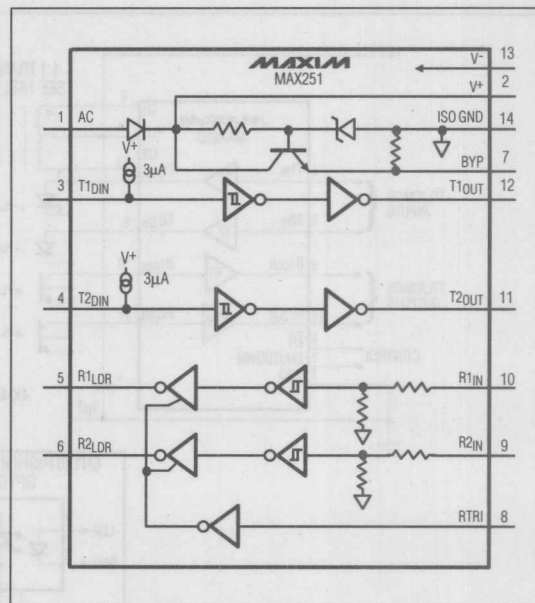


Figure 2. MAX251 Block Diagram

Typical Applications

Figure 3 shows the typical connection for a complete 19.2k baud isolated RS-232 circuit. Figure 3 also shows how 4N26 optocouplers can be replaced by 6N136 devices to achieve 90k baud rates.

A recommended printed circuit board layout is shown in Figure 4. This may be modified for individual designs but two important factors should be considered. 1.) To maximize isolation, the "isolation line" through the center of Figure 4 should not be breached. Connections and components from one side should not be located near those of the other side. 2.) Since the optocoupler outputs are relatively high impedance nodes, they should be located as close as possible to the MAX250 and MAX251. This minimizes stray capacitance and maximizes data rate.

When the MAX250's shutdown input (SHDN) is taken high, power is removed from the MAX251, and the RS-232 transmitter outputs (T1OUT, T2OUT) go to high impedance states. Timing plots in the Typical Operating Characteristics section show the turn-on and enable delays for various control functions.

The circuit in Figure 4 has been laid out so that it can be used for either a one or two sided PC board. The lines that are thick from one IC pad to the next IC pad are on the bottom side. Lines that are broken by a thin line can

either go on the top side of the board or on the bottom side with jumpers where the thin lines appear. At no time should any lines cross the middle of the board at the isolation barrier.

The MAX250 and MAX251 have a logic inversion in the optocoupler when using the standard configuration. For applications where no inversion is required, or more LED drive current is needed, Figure 5 shows the output structure of the LDR output. The LDR output can typically source 7mA and sink 25mA. Because of the higher sinking capability, a current limiting resistor is required.

Detailed Description

The MAX250 and MAX251, together with four optocouplers and a transformer, form an isolated dual RS-232 transmitter and receiver (See Figure 3). The MAX250 connects to the non-isolated or "logic" side of the interface, translating logic signals to and from the optocouplers, while the MAX251 resides on the isolated or "cable" side, translating data between the optocouplers and RS-232 line drivers and receivers. In addition to the optocoupler drivers and receivers, the MAX250 also contains isolation transformer drive circuitry which supplies power to the isolated side of the interface, and the MAX251.

+5V Powered Isolated RS-232 Drivers/Receivers

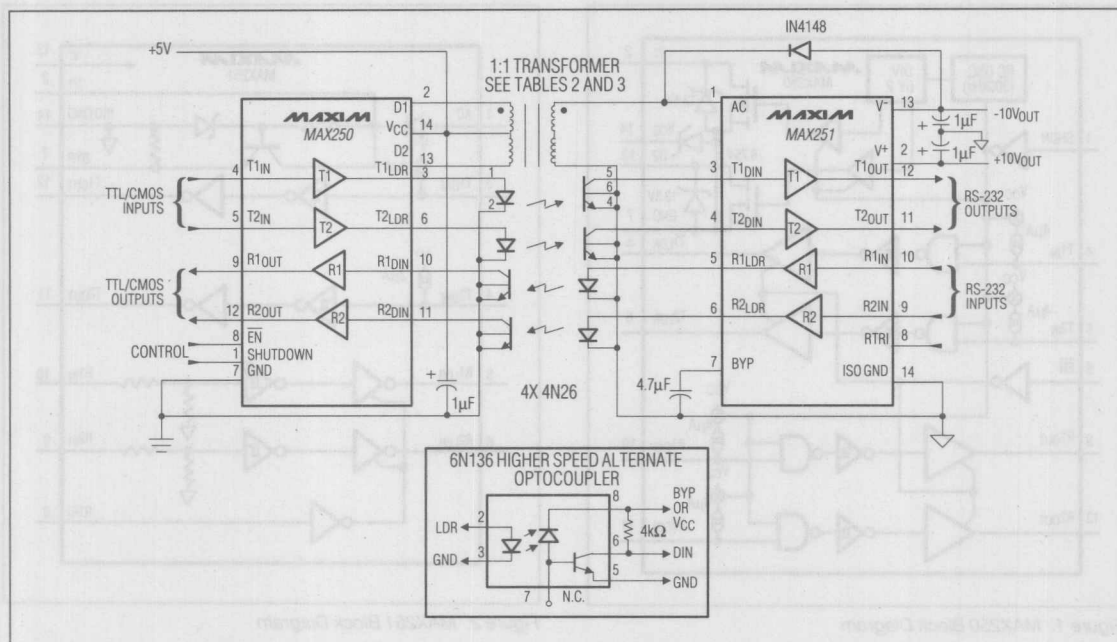


Figure 3. Isolated RS-232 Interface

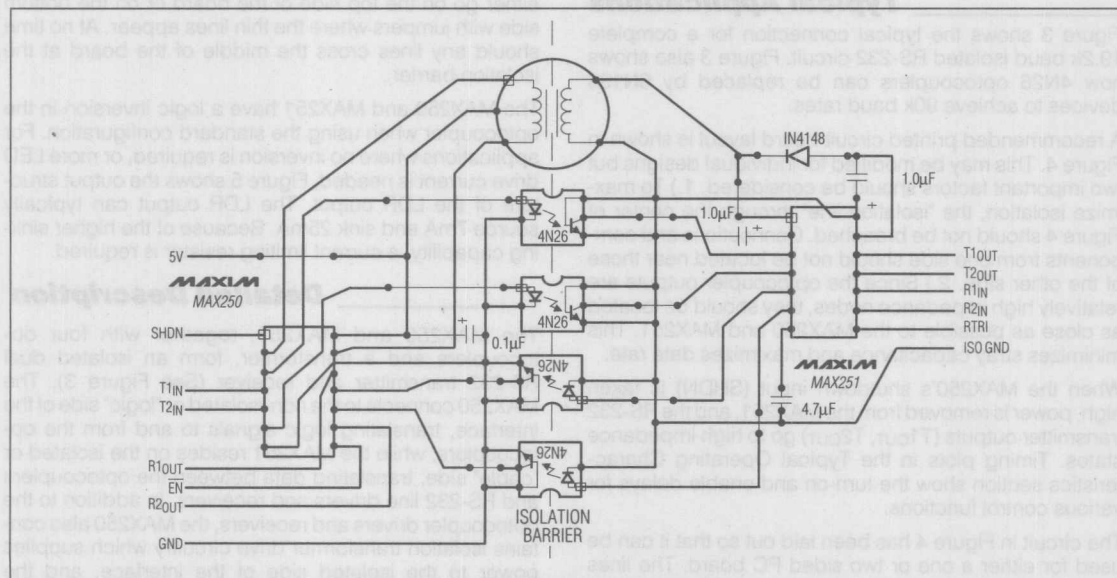


Figure 4. Recommended PC Board Layout for Dual Channel, Optoisolated, Self-Powered RS-232

+5V Powered Isolated RS-232 Drivers/Receivers

MAX250/MAX251

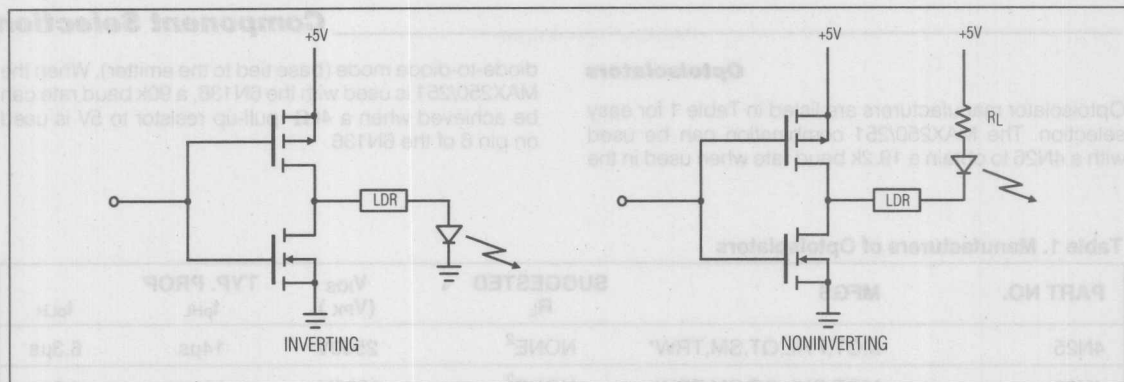


Figure 5. LDR Output Structure

MAX250

The MAX250 contains four identical noninverting drivers whose outputs may be used either as optocoupler LED drivers or as TTL/CMOS logic outputs. Each driver input (T1_{IN}, T2_{IN}, R1_{DIN}, R2_{DIN}) has a "weak" 4 μ A internal pull-up current source, and 0.5V of hysteresis to improve noise rejection. The input logic thresholds conform to standard TTL/CMOS specifications.

In normal operation, the MAX250 driver outputs (T1_{LDR}, T2_{LDR}, R1_{OUT}, R2_{OUT}) source 7mA via internal current sources and do not require limiting resistors when driving grounded optocoupler LEDs or CMOS/TTL logic inputs. The outputs can also sink up to 25mA when the current is limited by external resistors.

D1 and D2 are open-drain N-Channel MOSFETs which drive an external isolation transformer in push-pull fashion at 150kHz with a 50% duty cycle. A 1:1 transformer turns ratio provides a 10V peak-to-peak output at the secondary. Specifications and suitable manufacturer's part numbers for this transformer are listed in Tables 2 and 3. No transformer snubbers are required because D1 and D2 are protected against switching transients by internal 13.5V zener clamp diodes as shown in Figure 1.

The MAX250 functions also include an output enable control (EN) and a SHUTDOWN pin (SHDN). EN puts all driver outputs into a high impedance state when driven high. SHDN, when pulled high, disables the following MAX250 functions:

- 1.) Disables D1 and D2;
- 2.) Turns off the oscillator;
- 3.) Shuts off 4 μ A pull-up currents at driver inputs;
- 4.) Resets driver outputs to a low state;
- 5.) Lowers power consumption to 5 μ W.

MAX251

The MAX251 connects to the "cable" side of the RS-232 interface and includes two line drivers and receivers along with circuitry to translate these levels to optocoupler signals. The RS-232 inputs (R1_{IN}, R2_{IN}) and outputs (T1_{OUT}, T2_{OUT}) completely conform to all EIA RS-232C and CCITT V.28 specifications. The receiver outputs (R1_{LDR}, R2_{LDR}) source 7mA and can drive optocoupler inputs without external current limiting resistors. The MAX251 transmitter inputs (T1_{DIN}, T2_{DIN}) contain 4 μ A internal pull-ups which allow direct connection to optocoupler output transistors, again without external resistors.

When the MAX251's RTRI input is pulled high, the receiver outputs (R1_{LDR}, R2_{LDR}) are disabled and go to a high impedance state. In normal operation, this pin is left open or grounded.

Optocoupler Limitations

In Figure 3, the 4N26 optocouplers are connected in "diode mode" to optimize cost and data rate. While Current Transfer Ratio (CTR) is generally unspecified for this configuration, optocouplers from several manufacturers have been successfully tested in this circuit. The MAX250/MAX251 require a minimum optocoupler current transfer ratio of 0.12%, but may exhibit data rate limitations from the combined effect of higher MAX250/MAX251 drive and high optocoupler CTR.

The 6N136 optocouplers, shown in the inset in Figure 3 and listed in Table 1, operate in phototransistor mode, with limiting values of CTR specified by the manufacturers.

If further information is required, please contact Maxim Applications.

+5V Powered Isolated RS-232 Drivers/Receivers

Component Selection

Optoisolators

Optoisolator manufacturers are listed in Table 1 for easy selection. The MAX250/251 combination can be used with a 4N26 to obtain a 19.2k baud rate when used in the

diode-to-diode mode (base tied to the emitter). When the MAX250/251 is used with the 6N136, a 90k baud rate can be achieved when a 4k Ω pull-up resistor to 5V is used on pin 6 of the 6N136.

Table 1. Manufacturers of Optoisolators

PART NO.	MFGS	SUGGESTED R _L	V _{IOS} (V _{PK})	TYP. PROP t _{pHL}	t _{pLH}
4N25	MOT,PHL,QT,SM,TRW*	NONE ²	2500V	14 μ s	6.3 μ s
4N26	MOT,PHL,QT,SM,TRW	NONE ²	1500V	14 μ s	4.3 μ s
6N136	HP,QT,TRW	4K	2500V	1.8 μ s	1.5 μ s

* MOT= Motorola Inc. (303) 337-3434

PHL= Phillips (401) 232-0500

QT = Quality Technologies (General Instrument) (415) 493-0400

SM = Siemens Components (408) 257-7910

TRW= TRW Electronic Components Group (214) 323-2200

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Note 2: When used with a MAX250/251.

Transformers

Table 2 is a list of transformer characteristics that should be used to customize your own transformer. Table 3 is a list of transformers that are compatible with the

MAX250/251 chip set. The list includes both transformers that are small and more expensive and transformers that are larger and less expensive.

Table 2. Transformer Characteristics

Pri. Inductance	1mH to 2.5mH
Pri. Leakage Inductance	30 μ H
Turns Ratio	1:1 Pri. center tapped
ET	50V- μ s
Switching Frequency	150kHz
Interwinding Capacitance	< 100pF
DC Resistance	< 2 Ω
I _{pk}	300mA
Dielectric Strength	> 1500 VAC/1sec.

+5V Powered Isolated RS-232 Drivers/Receivers

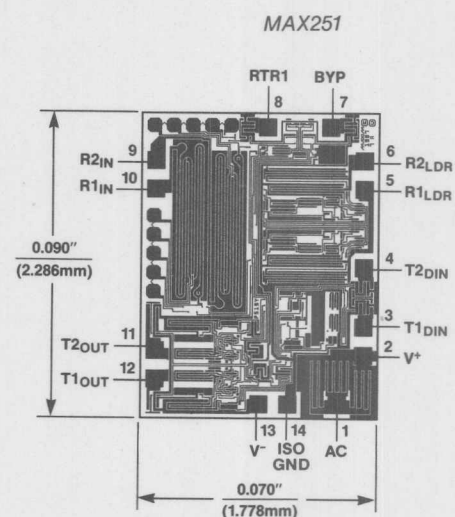
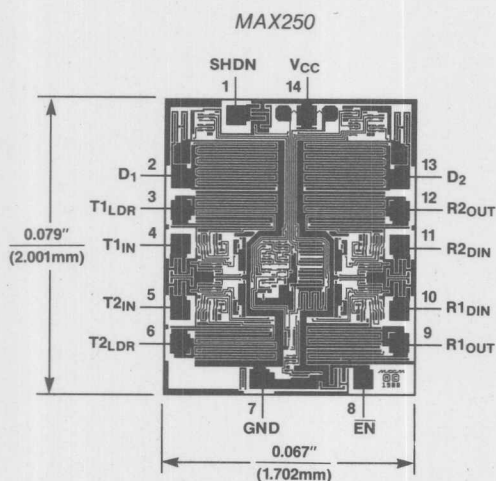
MAX250/MAX251

Table 3. Transformers Selection for Common Designs

MANUFACTURERS	LESS EXPENSIVE	SMALL
BH ELECTRONICS 604 Michigan Rd. Marshall, MN 56258 (507) 532-3211	Q6471-1	Q6471-2
MINI-MAGNETICS 1100 Fulton Place Fremont, CA 94539-7077 (415) 490-7500	MM2757	MM2758
SCHOTT Corporation 1000 Parkers Lake Rd. Minneapolis, MN 55391 (612) 475-1173	67114760	67117970

Note 1: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

Chip Topographies



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Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

Complete +5V-Powered Isolated Dual RS-232 Transceiver Module

General Description

The MAX252 complete, electrically isolated dual RS-232 transmitter/receiver systems require no external components. By combining many functions in one package, the cost and complexity of an isolated digital interface are greatly reduced.

A single +5V supply powers both sides of the interface. Transceivers, optocouplers, and a transformer in one low-cost package provide a complete interface up to 9600 bits/sec. Additional pins provide low-power shutdown and a high impedance state for both transmitter outputs.

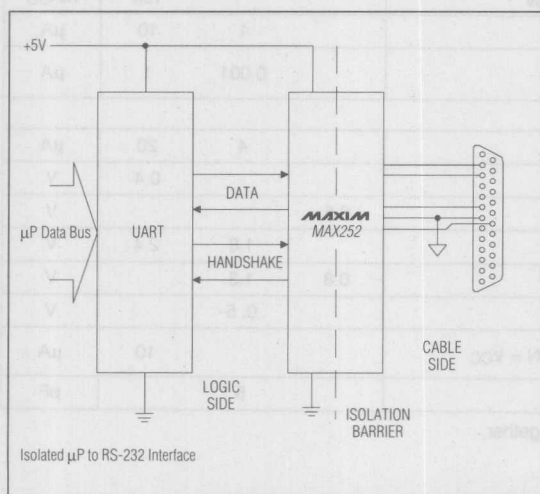
The MAX252A withstands 130V_{RMS} (continuous), 1260V_{RMS} (1 minute) or 1520V_{RMS} (1 sec) and is intended for applications where very high transient voltages, differential ground potentials or noise may be encountered. UL recognition is pending. The MAX252B is intended for less stringent applications and is rated for 500V_{RMS} (1 minute) or 600V_{RMS} (1 sec).

Receivers and line drivers (transmitters) meet EIA RS-232D and CCITT V.28 specifications. The MAX252 are supplied in 40-pin plastic DIP packages in commercial (0°C to +70°C) and extended (-40°C to +85°C) temperature ranges.

Applications

High Noise Environments
Industrial Controls
Differential Ground Potentials

Typical Application



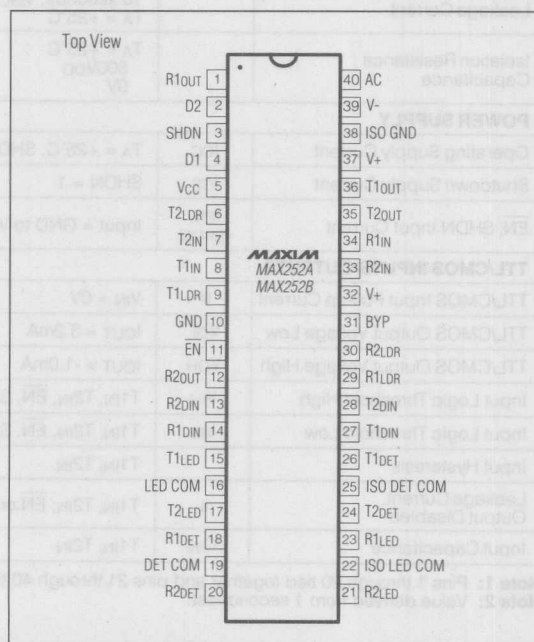
Features

- ◆ Isolated Data Interface
- ◆ No External Components
- ◆ Single +5V Supply
- ◆ 50µW Low-Power Shutdown
- ◆ Two Transmitters and Two Receivers
- ◆ UL Recognition Pending (MAX252A)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX252AÇHL	0°C to +70°C	40 Plastic Module
MAX252BCHL	0°C to +70°C	40 Plastic Module
MAX252AEHL	-40°C to +85°C	40 Plastic Module
MAX252BEHL	-40°C to +85°C	40 Plastic Module

Pin Configuration



MAX252

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MAXIM

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Maxim Integrated Products 6-29

Complete +5V-Powered Isolated Dual RS-232 Transceiver Module

ABSOLUTE MAXIMUM RATINGS

Voltages with respect to GND (pin 10)
 Supply Voltage, V_{CC} -0.3V to +6V
 Input Voltage
 Pins 3, 7, 8, 11, 13, 14, 18, 20 -0.3V to ($V_{CC} + 0.3V$)
 Voltages with respect to ISO GND (pin 38)
 RS-232 Input Voltage (pins 33, 34) -30V to +30V
 RS-232 Applied Output Voltage (pins 35, 36) -15V to +15V
 Pins 32, 37 (V^+) +15V
 Pins 24, 26, 31 V^+
 RS-232 Transmitter outputs may be shorted individually and indefinitely to ISO GND.

LED Forward Continuous Current (Pins 15, 17, 21, 23) ... 30mA
 Power Dissipation
 Plastic DIP (Derate 10mW/°C above +70°C) 650mW
 Storage Temperature +150°C
 Lead Temperature (Soldering, 10 sec.) -65°C to +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V \pm 10\%$, $T_A = \text{Full Temperature Range}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION (Note 1)						
Test Voltage	VISO	$T_A = +25^\circ\text{C}$ MAX252A 1 sec. 1 minute (Note 2) Continuous (Note 2) MAX252B 1 sec. 1 minute (Note 2)	1520 1260 130 600 500			V _{RMS}
Leakage Current		10 seconds, VISO = 500V _{RMS} , 60Hz $T_A = +25^\circ\text{C}$		10	50	μA_{RMS}
Isolation Resistance Capacitance		$T_A = +25^\circ\text{C}$ 500VDC 0V		10 ¹⁰ 10		Ω pF
POWER SUPPLY						
Operating Supply Current	I _{CC}	$T_A = +25^\circ\text{C}$, SHDN = 0V			130	mADC
Shutdown Supply Current	I _{CS}	SHDN = 1		1	10	μA
$\overline{\text{EN}}$, SHDN Input Current	I _{EN} , I _{SHDN}	Input = GND to V_{CC}		0.001	1	μA
TTL/CMOS INPUTS/OUTPUTS						
TTL/CMOS Input Pull-up Current	I _P	$V_{IN} = 0V$		4	20	μA
TTL/CMOS Output Voltage Low	V _{OL}	I _{OUT} = 3.2mA			0.4	V
TTL/CMOS Output Voltage High	V _{OH}	I _{OUT} = -1.0mA	3.5			V
Input Logic Threshold High	V _{IH}	T _{1IN} , T _{2IN} , $\overline{\text{EN}}$, SHDN		1.8	2.4	V
Input Logic Threshold Low	V _{IL}	T _{1IN} , T _{2IN} , $\overline{\text{EN}}$, SHDN	0.8	1.3		V
Input Hysteresis		T _{1IN} , T _{2IN}		0.5		V
Leakage Current, Output Disabled	I _L	T _{1IN} , T _{2IN} ; $\overline{\text{EN}}$ or SHDN = V_{CC}			10	μA
Input Capacitance	C _{IN}	T _{1IN} , T _{2IN}		5		pF

Note 1: Pins 1 through 20 tied together and pins 21 through 40 tied together.

Note 2: Value derived from 1 second test.

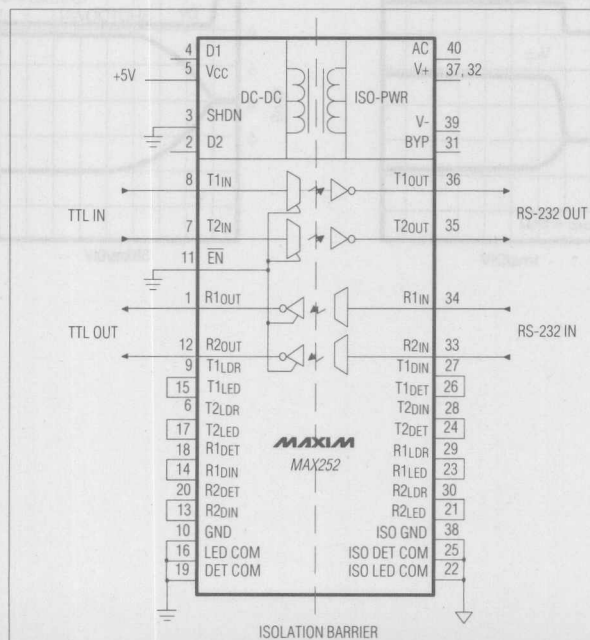
Complete +5V-Powered Isolated Dual RS-232 Transceiver Module

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, T_A = Full Temperature Range, unless otherwise noted.)

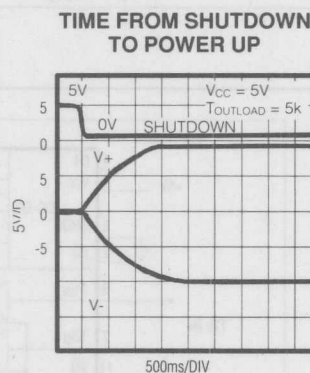
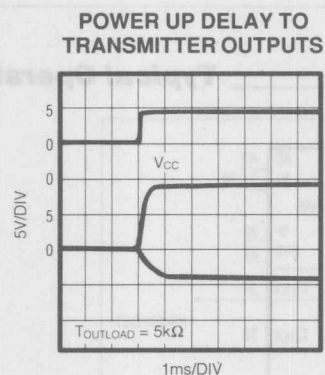
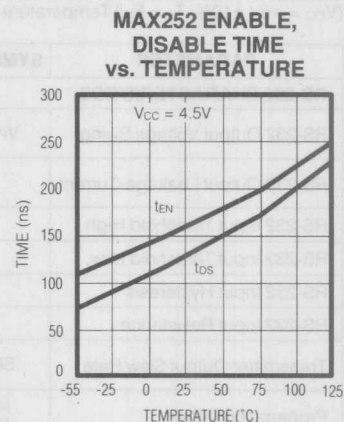
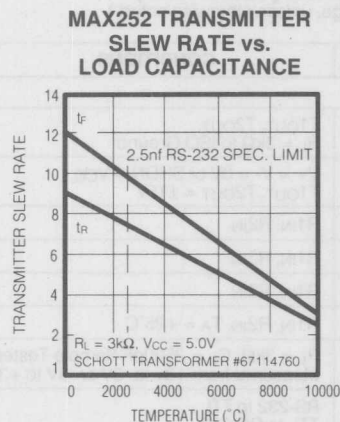
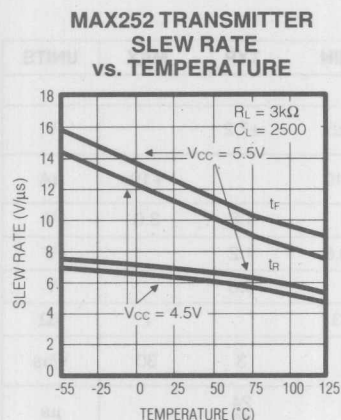
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RS-232 CHARACTERISTICS						
RS-232 Output Voltage Swing	V _{PP}	T1 _{OUT} , T2 _{OUT} , R _L = 3kΩ to ISO Ground	±5	±7.2		V
RS-232 Output Leakage Current		V ₊ = V ₋ = 0V or SHDN = V _{CC} , T1 _{OUT} , T2 _{OUT} = ±15V	-10		+10	μA
RS-232 Input Threshold High		R1 _{IN} , R2 _{IN}		1.8	3.0	V
RS-232 Input Threshold Low		R1 _{IN} , R2 _{IN}	0.6	1.2		V
RS-232 Input Hysteresis		R1 _{IN} , R2 _{IN}		0.6		V
RS-232 Input Resistance		R1 _{IN} , R2 _{IN} , T _A = +25°C	3		7	kΩ
Transmitter Output Slew Rate	SR	R _L = 3kΩ, C _L = 2500pF Sample Tested Measured from +3v to -3v or -3V to +3V		3	30	V/μs
Propagation Delay	t _R t _T	RS-232 to TTL TTL to RS-232		24 20		μs
Transmission Rate		Sample Tested R _L = 3kΩ C _L = 2500pF	9600			Bits/s

Typical Operating Circuit



Complete +5V-Powered Isolated Dual RS-232 Transceiver Module

Typical Operating Characteristics



Complete +5V-Powered Isolated Dual RS-232 Transceiver Module

Pin Description

PIN #	NAME	FUNCTION
1	R1OUT	Receiver #1 Output; TTL/CMOS logic levels
2	D2	Internal Connection. Leave this pin unconnected. Do not ground.
3	SHDN	Shutdown. When high, turns off the oscillator and disconnects driver inputs. Ground for normal operation.
4	D1	Internal Connection. Leave this pin unconnected. Do not ground.
5	VCC	+5V Supply Voltage
6	T2LDR	Transmitter #2 LED Driver
7	T2IN	Transmitter #2 Input; TTL/CMOS logic levels
8	T1IN	Transmitter #1 Input; TTL/CMOS logic levels
9	T1LDR	Transmitter #1 LED Driver
10	GND	Ground
11	$\overline{\text{EN}}$	Output Enable. If High, T1LDR, T2LDR, R1OUT, and R2OUT go to high impedance state. Ground for normal operation.
12	R2OUT	Receiver #2 Output; TTL/CMOS logic levels
13	R2DIN	Receiver #2 Detector Input
14	R1DIN	Receiver #1 Detector Input
15	T1LED	T1 LED Anode Input
16	LED COM	Common T1LED, T2LED Cathode. Tie to Ground.
17	T2LED	T2 LED Anode Input
18	R1DET	R1 Photodiode Cathode Output
19	DET COM	Common R1DET, R2DET Anode. Tie to Ground.
20	R2DET	R2 Photodiode Cathode Output

PIN #	NAME	FUNCTION
21	R2LED	R2 LED Cathode Input
22	ISO LED COM	Common R1LED, R2LED Cathode. Tie to Isolated Ground.
23	R1LED	R1 LED Cathode Input
24	T2DET	T2 Photodiode Anode Output
25	ISO DET COM	Common T1DET, T2DET LED Anode. Tie to Isolated Ground.
26	T1DET	T1 Photodiode Anode Output
27	T1DIN	Transmitter #1 Detector Input
28	T2DIN	Transmitter #2 Detector Input
29	R1LDR	Receiver #1 LED Driver
30	R2LDR	Receiver #2 LED Driver
31	BYP	Internal Connection. Leave this pin unconnected. Do not ground.
32	V+	Isolated Positive Supply
33	R2IN	RS-232 Receiver #2 Input
34	R1IN	RS-232 Receiver #1 Input
35	T2OUT	RS-232 Transmitter #2 Output
36	T1OUT	RS-232 Transmitter #1 Output
37	V+	Isolated Positive Supply
38	ISO GND	Isolated Ground
39	V-	Isolated Negative Supply Voltage
40	AC	Internal Connection. Leave this pin unconnected. Do not ground.

MAX252

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Complete +5V-Powered Isolated Dual RS-232 Transceiver Module

Isolation Applications

The MAX252 is intended for industrial communications and control applications where voltage transients, differential ground potentials or high noise may be encountered. The MAX252A withstands 130V_{RMS} (continuous), 1260V_{RMS} (1 minute) or 1520V_{RMS} (1 second). For less stringent applications, the MAX252B is rated at 500V_{RMS} (1 minute) or 600V_{RMS} (1 second). For applications requiring higher isolation ratings or transmission rates, Maxim recommends the MAX250 and MAX251 device set, which uses external optocouplers and transformer.

Figure 1 shows the typical interconnection for a complete 9600 bits/s transceiver. Important layout considerations include:

* for maximum isolation, the "isolation line" through the center of Figure 1 should not be breached; connections from each side should be kept separate.

* optocoupler outputs (pins 18, 20, 24, and 26) are high impedance nodes, so connecting traces should be

as short as possible to minimize stray capacitance and maximize data transfer rate; shunt capacitance seen by each pin should not exceed 10pF.

The MAX252 pinout enables optimal printed circuit board layout by minimizing interconnect lengths and cross-overs. Figure 2 shows the preferred layout, which is strongly recommended for 9600 bits/s applications. Note the position of the ground traces, particularly the protection of pin 20 by the wraparound from pin 19.

Isolation Example

Figure 3 illustrates how to isolate an existing RS-232 interface by inserting a MAX252 and MAX233 in series. Both devices invert while translating RS-232 to TTL and TTL to RS-232 levels. Since there is no net inversion, the circuit functions like two "plain pieces of wire", but with 1520V_{RMS} (at 1 sec) isolation between the ports.

Detailed Description

The MAX252 contains two integrated circuits, four optocouplers, four capacitors, two diodes, and a small transformer. Together, these provide a complete, isolated, dual RS-232 transmitter and receiver. The non-isolated or "logic" side of the interface transfers logic signals to and from the optocouplers, while the isolated or "cable" side transfers data between the optocouplers and RS-232

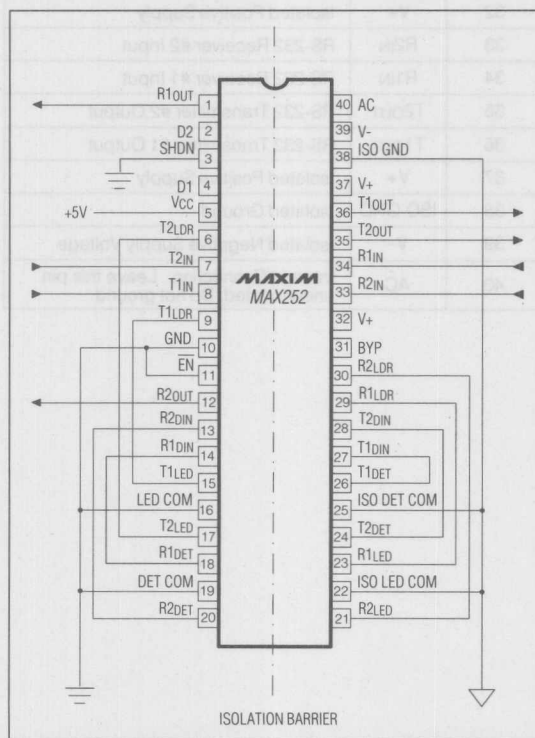


Figure 1. Typical Interconnections

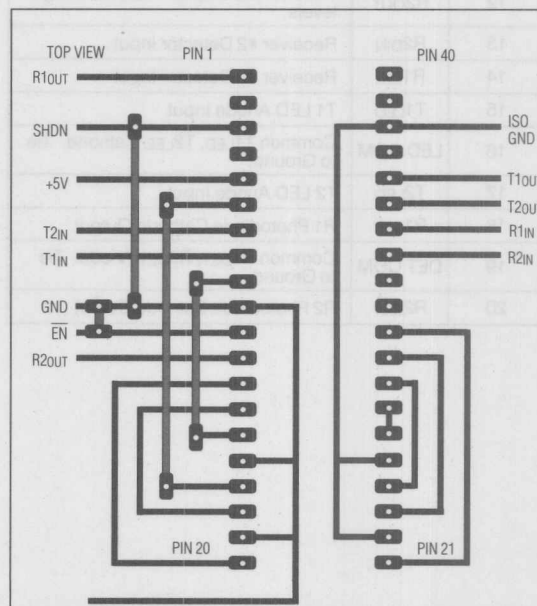


Figure 2. Preferred Layout

Complete +5V-Powered Isolated Dual RS-232 Transceiver Module

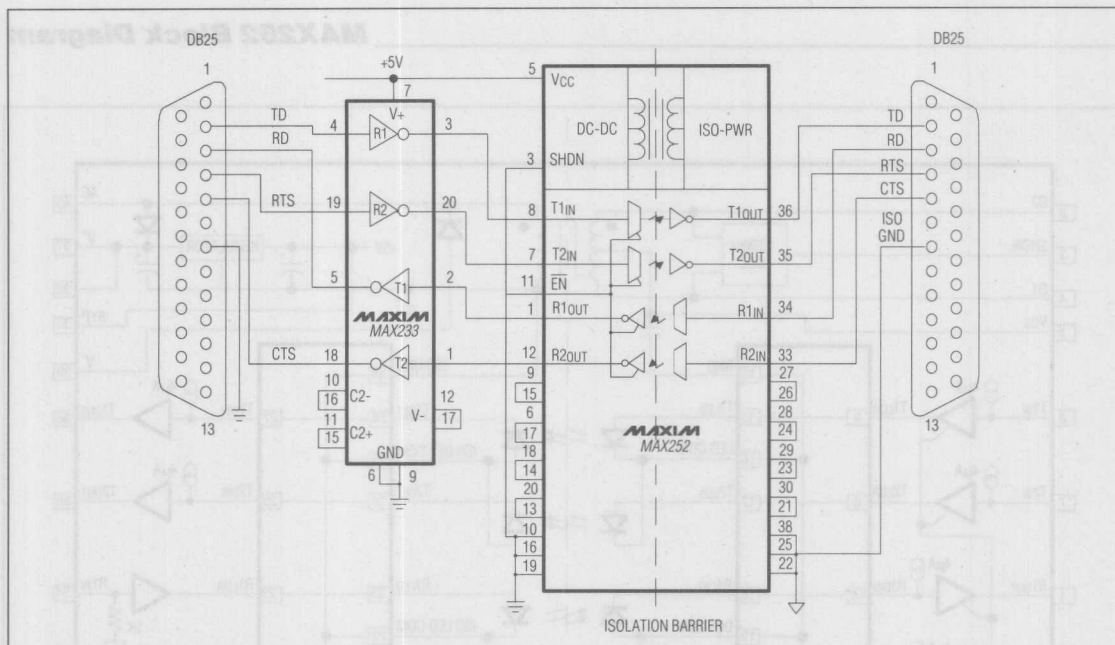


Figure 3. RS-232 Isolation Adapter from a Single 5V Supply

transmitters (line drivers) and receivers. The MAX252 also contains an isolation transformer and drive circuitry to supply power to the isolated side of the interface.

On the logic side of the MAX252 are four identical non-inverting drivers whose outputs may be used either as optocoupler LED drivers or as TTL/CMOS logic outputs. Each driver input (T1_{IN}, T2_{IN}, R1_{DIN}, R2_{DIN}) has a "weak" 4μA internal pull-up current source, and 0.5V hysteresis to improve noise rejection; logic thresholds for the driver inputs conform to standard TTL/CMOS specifications.

The RS-232 side of the interface includes two line drivers and receivers along with circuitry to translate these levels to optocoupler signals. The RS-232 inputs (R1_{IN}, R2_{IN}) and outputs (T1_{OUT}, T2_{OUT}) conform to EIA RS-232D and CCITT V.28 specifications. The inputs to the RS-232 line drivers (T1_{DIN}, T2_{DIN}), which are normally strapped to the internal optoisolators, are TTL/CMOS compatible.

Also included are an OUTPUT ENABLE control ($\overline{\text{EN}}$) and a SHUTDOWN pin (SHDN). $\overline{\text{EN}}$ places all driver outputs in a high impedance state when driven high. SHDN, when pulled high, performs the following functions:

- 1) turns off the 130kHz oscillator, removing power from the RS-232 side of the interface;
- 2) places T1_{OUT} and T2_{OUT} in a high impedance state;
- 3) disables the 4μA pull-up currents at the logic-side driver inputs (T1_{IN}, T2_{IN}, R1_{DIN}, R2_{DIN});
- 4) resets logic-side driver outputs (T1_{LDR}, T2_{LDR}, R1_{OUT}, R2_{OUT}) to LOW;
- 5) reduces power consumption to 50μW.

Module Product Reliability

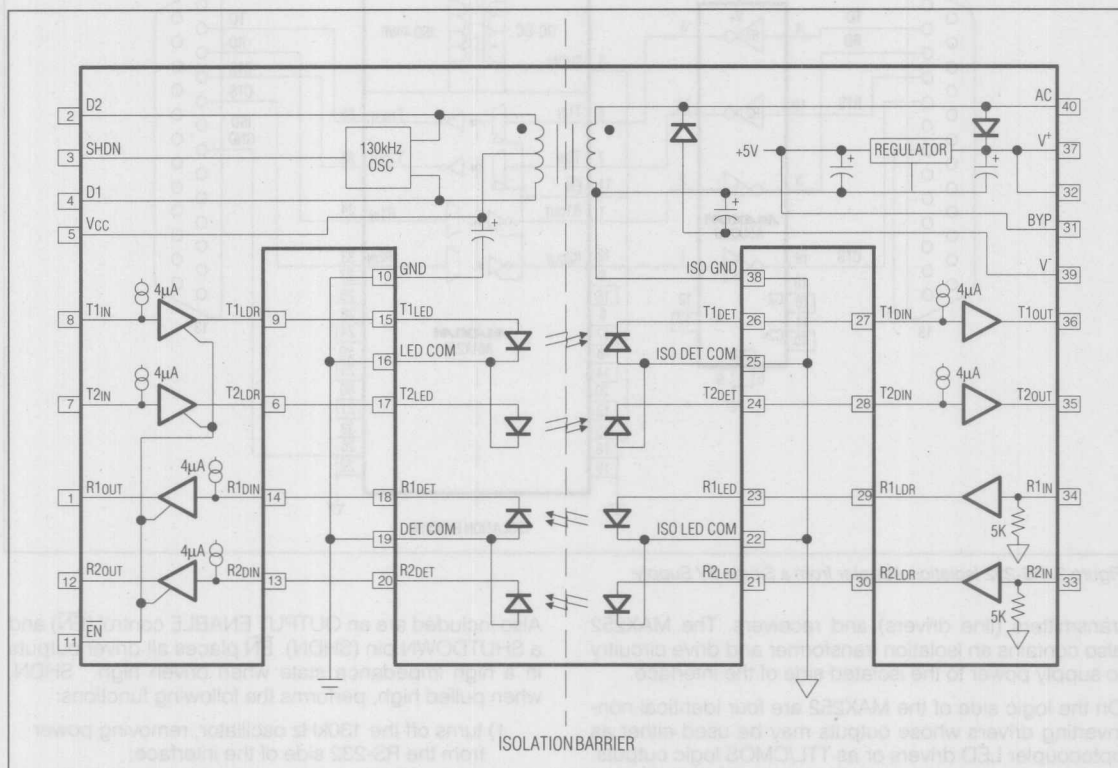
For reliability data on Maxim's Module Product Line, see Reliability Report RR-3A following this data sheet.

MAX252

6

Complete +5V-Powered Isolated Dual RS-232 Transceiver Module

MAX252 Block Diagram



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Module Product Reliability Report

Quality and Reliability Considerations

Extensive reliability testing is performed on all Maxim products to ensure prolonged operational life. Quality and reliability tests are performed under conditions which equal or exceed normal operation. These tests are designed to accelerate any possible failure modes that could occur during normal product life.

Although packaged in standard outline plastic molded DIP packages, Maxim isolated RS232 transceiver modules exhibit certain differences compared to monolithic ICs. For example, multiple components such as optocouplers and miniature transformers are included within the package. For this reason, Maxim issues separate reliability reports for module products.

Maxim's goal is to build opto-isolated module products which are more reliable than encapsulated opto-isolators from leading suppliers. Although our reliability program is based on an industry-wide survey of opto-isolator manufacturers, Maxim's testing is more stringent in several areas.

The data in Table 1 were recorded for pre-production units of MAX252ACHL. Note that Life Test failures were due to assembly-related defects: the cause has been identified and corrective action taken. Updates will be issued as more data becomes available.

For reliability data on Maxim's standard monolithic products, see Reliability Report RR-1. For reliability data on surface mount products, see Reliability Report RR-2.

RR-3A

Table 1: Reliability Data For MAX252

TEST NAME	TEST CONDITIONS	# OF UNITS TESTED	FAILURES
Life Test	125°C, 1000 hours, biased	80	2*
Temperature Cycle	-65°C to +150°C, 100 cycles, Dwell = 15 minutes	62	0
Thermal Shock	0°C to +100°C, 100 cycles, Dwell = 10 minutes	15	0
Solderability	Sn63/Pb37 solder, T = 245°C, Dwell = 5 seconds	25	0
Resistance to Solvents	One minute immersion, then brushing; repeat 3 times	25	0
Physical Dimension	Per package drawing	5	0
Lead Fatigue	Bend a lead 90° three times	5	0

* Both Life Test failures were due to assembly-related defects: corrective action has been taken.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.



Analog Filters

MAX270	Digitally Programmed, Dual 2nd-Order Continuous Lowpass Filter	7-1
MAX271	Digitally Programmed, Dual 2nd-Order Continuous Lowpass Filter	7-1
MAX281	5th-Order, Zero-Error, Bessel Switched-Capacitor Lowpass Filter	7-3

Digitally Programmed, Dual 2nd-Order Continuous Lowpass Filters

General Description

The MAX270/MAX271 are digitally programmed, dual 2nd-order continuous-time lowpass filters. Typical dynamic range of the filters is 96dB, surpassing most switched capacitor filters which require additional filtering for removal of clock noise. The MAX270/MAX271 are ideal for anti-aliasing and DAC smoothing applications and can be cascaded for faster rolloff.

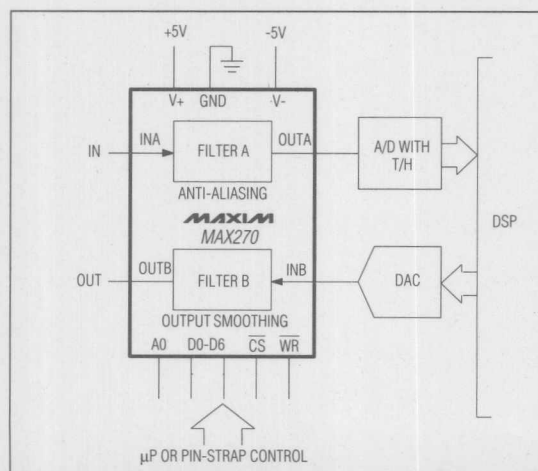
The two filter sections are independently programmable either by microprocessor (μ P) control or pin strapping. Cutoff frequencies in the range of 1kHz to 25kHz can be programmed.

The MAX270/MAX271 differ in two respects. The MAX270 has an on-board uncommitted op amp, while the MAX271 has an internal Track-and-Hold (T/H). Also, the MAX270/MAX271 differ slightly in their control programming.

Applications

Anti-Aliasing Filters
DAC Output Smoothing Applications
Low-Noise Applications

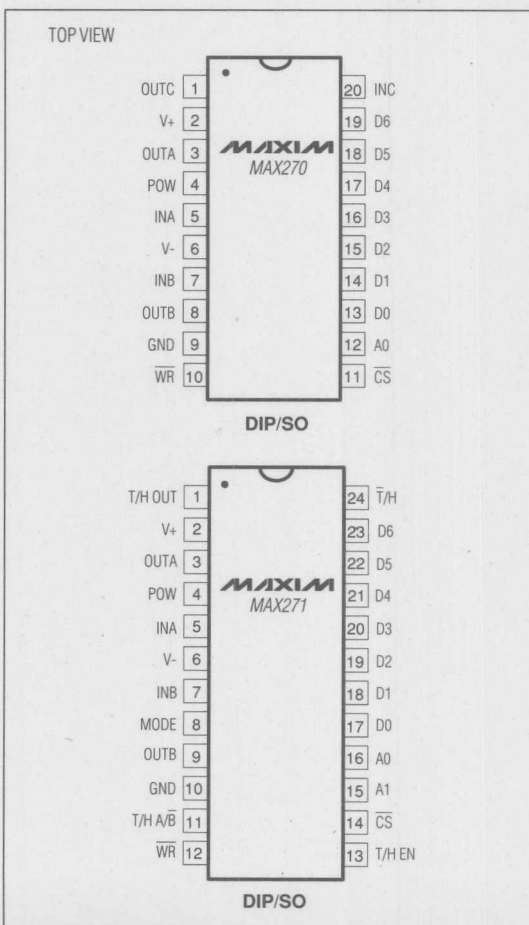
Typical Operating Circuit



Features

- ◆ Dual 2nd-Order Continuous Lowpass Filters
- ◆ No External Components
- ◆ Sections Independently Programmable: 1kHz to 25kHz
- ◆ Continuous-Time Filters - No Clock Required
- ◆ 96dB Dynamic Range
- ◆ Cascadable for Higher Order

Pin Configurations



MAX270/MAX271

7

5th-Order, Zero-Error, Bessel Lowpass Filter

General Description

The MAX281 is a 5th-order all-pole instrumentation lowpass filter with no DC error. The filter uses an external resistor and capacitor to isolate the integrated circuit from the DC signal path, thus providing DC accuracy.

The external resistor and capacitor together with the on-chip 4th order switched capacitor filter form a 5th-order Bessel lowpass filter. Bessel lowpass filters provide linear phase (constant group delay) response from DC to beyond the filter cutoff frequency, with some reduction in stopband attenuation.

The filter cutoff frequency is set by a clock which can be either internally generated or externally provided. The clock to cutoff frequency ratio of 101 allows easy removal of clock ripple.

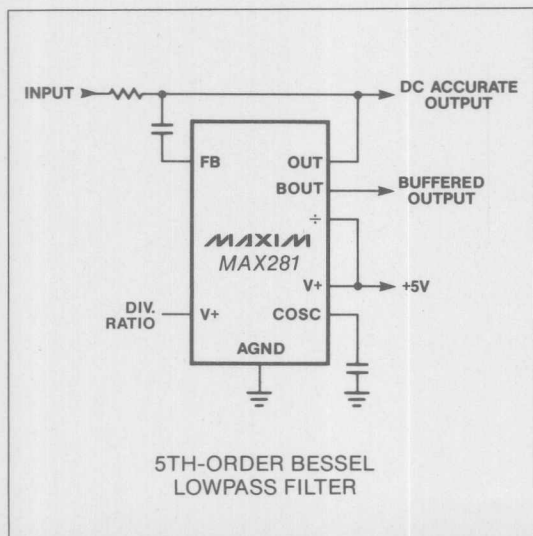
MAX281A provides tighter specifications than the MAX281B for internal clock oscillator frequency and buffer amplifier offset voltage.

MAX280 is available for applications requiring a maximally flat (Butterworth) amplitude response.

Applications

Anti-Aliasing Filters
Data Loggers
Digital Voltmeters
Weigh Scales
Strain Gauges

Typical Operating Circuit



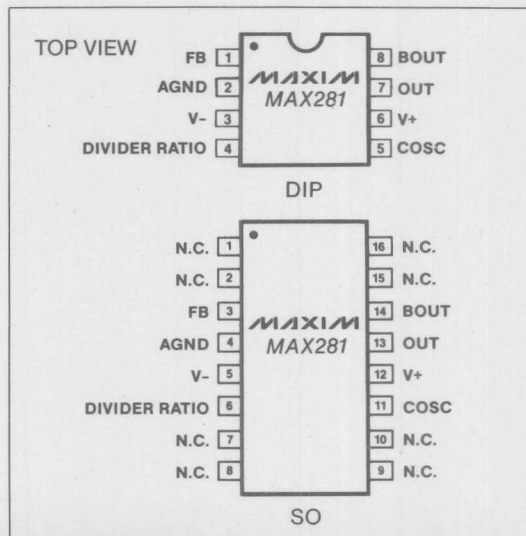
Features

- ◆ Bessel Lowpass Filter with No DC Error
- ◆ Low Passband Noise
- ◆ DC to 20kHz Cutoff Frequency
- ◆ 5th-Order All-Pole Bessel Response
- ◆ Internal or External Clock
- ◆ Cascadable for Higher Order Rolloff
- ◆ Buffered Output Available
- ◆ 8-Pin DIP or 16-Pin Wide SO Packages

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX281ACPA	0°C to +70°C	8 Plastic DIP
MAX281BCPA	0°C to +70°C	8 Plastic DIP
MAX281ACWE	0°C to +70°C	16 Wide SO
MAX281BCWE	0°C to +70°C	16 Wide SO
MAX281C/D	0°C to +70°C	DICE
MAX281AEPA	-40°C to +85°C	8 Plastic DIP
MAX281BEPA	-40°C to +85°C	8 Plastic DIP
MAX281AEWE	-40°C to +85°C	16 Wide SO
MAX281BEWE	-40°C to +85°C	16 Wide SO
MAX281AMJA	-55°C to +125°C	8 CERDIP
MAX281BMJA	-55°C to +125°C	8 CERDIP

Pin Configurations



MAX281

7



Analog Multiplexers

MAX328	Ultra-Low Leakage Monolithic CMOS Analog Multiplexer	8-1
MAX329	Ultra-Low Leakage Monolithic CMOS Analog Multiplexer	8-1
MAX368	Fault Protected 8 Channel Latched Multiplexer	8-3
MAX369	Fault Protected 8 Channel Latched Multiplexer	8-3
MAX378	High Voltage, Fault-Protected Analog Multiplexer	8-15
MAX379	High Voltage, Fault-Protected Analog Multiplexer	8-15
MAX453	2 Channel 50MHz Video Multiplexer/Amplifier	4-41
MAX454	4 Channel 50MHz Video Multiplexer/Amplifier	4-41
MAX455	8 Channel 50MHz Video Multiplexer/Amplifier	4-41



Ultra-Low Leakage Monolithic CMOS Analog Multiplexers

MAX328/MAX329

General Description

The MAX328/MAX329 are monolithic CMOS analog multiplexers. The MAX328 is a single-ended, 1-of-8 device, and the MAX329 is a differential, 2-of-8 device.

Designed to provide the lowest possible "on" and "off" leakages, these multiplexers are effective in switching signals from high source impedance, provided the mux operates into a high input impedance op amp or A/D converter. The MAX328 and MAX329 are pin-for-pin replacements for the popular DG508/DG509 in these applications.

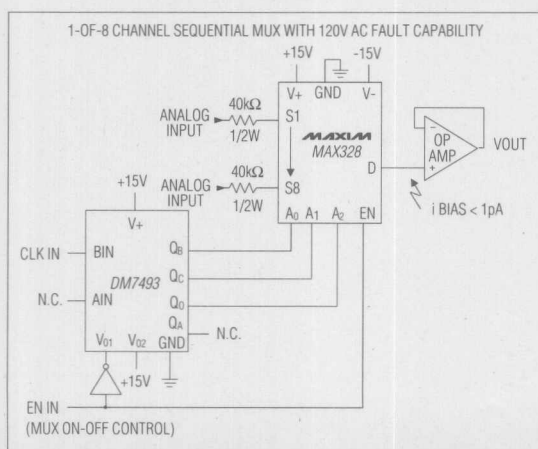
Adding an external 40k Ω resistor to each input of a MAX328/MAX329 makes an excellent fault-tolerant multiplexer. Low leakage (less than 1pA at 25°C) and 2.5k Ω on resistance allow the circuit to sustain 110V AC faults indefinitely while maintaining an error of less than 43nV for normal signals (i.e., 1pA times 43k Ω).

The MAX328/MAX329 work equally well with a single supply of 10V to 30V or dual supplies of $\pm 5V$ to $\pm 18V$. They also perform well with unbalanced combinations of supply voltage such as +12V and -5V or +5V and -15V. Low power dissipation (1.9mW with $\pm 15V$ supplies) enables use of the multiplexers in portable applications.

Applications

Control Systems
Data Logging Systems
Aircraft Heads-Up Displays
Data Acquisition Systems
Signal Routing

Typical Operating Circuit



Features

- ◆ Ultra-Low "Off" and "On" Leakage: 1pA Typ
- ◆ Bi-Directional Operation (Use as Mux or Demux)
- ◆ TTL and CMOS Logic Compatibility
- ◆ Analog Signal Range Includes Power-Supply Rails
- ◆ Switching Speeds Less Than 1.5 μ s
- ◆ Pin Compatible With DG508/DG509 and MAX358/MAX359
- ◆ Latch-Up Proof Construction

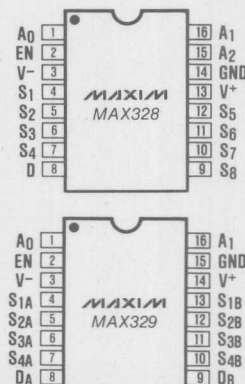
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX328CPE	0°C to +70°C	16 Plastic DIP
MAX328CWE	0°C to +70°C	16 Wide SO
MAX328CJE	0°C to +70°C	16 CERDIP
MAX328C/D*	0°C to +70°C	Dice
MAX328EPE	-40°C to +85°C	16 Plastic DIP
MAX328EWE	-40°C to +85°C	16 Wide SO
MAX328EJE	-40°C to +85°C	16 CERDIP
MAX328MJE	-55°C to +125°C	16 CERDIP

* Contact factory for availability.
** Substrate may be allowed to float or be tied to V+. Ordering information for MAX328 only.

Pin Configurations

Top View



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8-1

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

Fault-Protected Analog Multiplexer with Latch

General Description

Maxim's MAX368/369 are 8 channel single-ended (1 of 8) and 4 channel differential (2 of 8) fault-protected multiplexers with on-chip data latches. Using a series N-channel, P-channel, N-channel structure, these multiplexers provide significantly improved fault protection over previous devices. If power to the multiplexers is removed while input voltages are still applied, all channels turn off, allowing only a few nanoamperes of leakage current to flow in the inputs. This not only protects the multiplexer and the circuitry connected to the output, but also protects the sensors or signal sources which drive the multiplexer inputs.

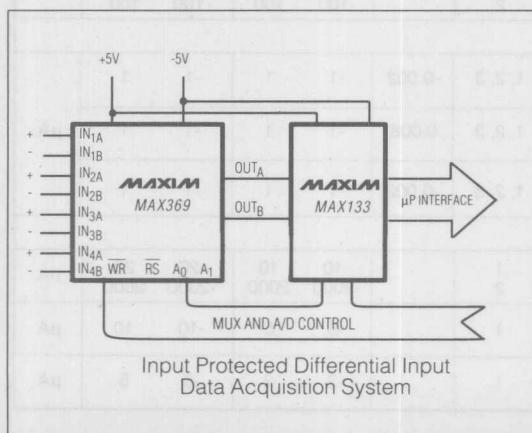
When an overvoltage signal of up to $\pm 35V$ is applied to an analog input of a Maxim fault-protected multiplexer, that input channel turns off. If the overvoltage is applied to an on channel, the multiplexer output is clamped to less than its power supply voltage, thereby protecting sensitive circuitry that may be connected to the multiplexer output.

All channel selection and control inputs are fully compatible with both TTL and CMOS logic levels. In addition, break-before-make switch operation is guaranteed and typical power dissipation is less than 7 milliwatts, which makes the MAX 368/369 ideally suited for portable equipment usage.

Applications

- Data Acquisition Systems
- Industrial Process Control Systems
- Avionics Test Equipment
- Signal Routing Between Systems
- Computer Controlled Analog Data Logging

Typical Operating Circuit



Features

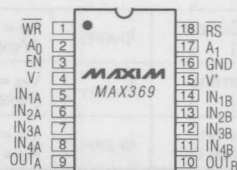
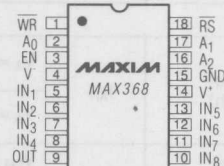
- ◆ All Switches Off with Power Supplies Off
- ◆ Overvoltage Protection up to $\pm 35V$
- ◆ Only Nanoamperes of Input Current under All Fault Conditions
- ◆ Latch-Up Proof Construction
- ◆ Operates from ± 4.5 to $\pm 18V$ Supplies
- ◆ All Digital Inputs are TTL and CMOS Compatible
- ◆ Internal Data Latches for Channel Selection

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX368C/D	0°C to +70°C	Dice
MAX368CPN	0°C to +70°C	18 Lead Plastic DIP
MAX368CJN	0°C to +70°C	18 Lead Cerdip
MAX368CWN	0°C to +70°C	18 Lead Wide SO
MAX368EPN	-40°C to +85°C	18 Lead Plastic DIP
MAX368EJN	-40°C to +85°C	18 Lead Cerdip
MAX368EWN	-40°C to +85°C	18 Lead Wide SO
MAX368MJN	-55°C to +125°C	18 Lead Cerdip
MAX369C/D	0°C to +70°C	Dice
MAX369CPN	0°C to +70°C	18 Lead Plastic DIP
MAX369CJN	0°C to +70°C	18 Lead Cerdip
MAX369CWN	0°C to +70°C	18 Lead Wide SO
MAX369EPN	-40°C to +85°C	18 Lead Plastic DIP
MAX369EJN	-40°C to +85°C	18 Lead Cerdip
MAX369EWN	-40°C to +85°C	18 Lead Wide SO
MAX369MJN	-55°C to +125°C	18 Lead Cerdip

Pin Configurations

Top View



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MAXIM

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Maxim Integrated Products 8-3

MAX368/369

Fault-Protected Analog Multiplexer with Latch

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins	+44V
V^+	+22V
V^-	-22V
Digital Input Overvoltage:	
V_{EN}, V_A $\begin{cases} V_{Supply(+)} \\ V_{Supply(-)} \end{cases}$	$\begin{cases} +4V \\ -4V \end{cases}$
Analog Input Overvoltage with Multiplexer Power On:	
V_S $\begin{cases} V_{Supply(+)} \\ V_{Supply(-)} \end{cases}$	$\begin{cases} +20V \\ -20V \end{cases}$
Analog Input Overvoltage with Multiplexer Power Off:	
V_S $\begin{cases} V_{Supply(+)} \\ V_{Supply(-)} \end{cases}$	$\begin{cases} +35V \\ -35V \end{cases}$

Continuous Current, S or D	20mA
Peak Current, S or D	
(Pulsed at 1ms, 10% duty cycle max)	40mA
Power Dissipation (Note 1) (CERDIP)	1.28W
Operating Temperature Range:	
MAX368/369C	0°C to +70°C
MAX368/369E	-40°C to +85°C
MAX368/369M	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

Note 1: Derate 12.8mW/°C above $T_A = +70^\circ\text{C}$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V^- = -15V$; GND = 0, WR = 0, RS = 2.4V unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	TEMP *	TYP	M SUFFIX		E, C SUFFIX		UNITS
						MIN	MAX	MIN	MAX	
ANALOG SWITCH										
Analog Signal Range		V _{ANALOG}	(Note 2)	1		-15	15	-15	15	V
Drain-Source ON Resistance		r _{DS (ON)}	V _D = ±10V, V _{AL} = 0.8V I _S = 100µA, V _{AH} = 2.4V	1, 3 2			1500 1800		1800 2000	Ω
Greatest Change in r _{DS(ON)} Between Channels		Δ r _{DS (ON)}	-10V < V _S < 10V	1	10					%
Source OFF Leakage Current		I _{S (OFF)}	V _{EN} = 0.8V	V _S = ±10V V _D = ∓10V	1 2	-0.005	-1 50	-5 50	-5 50	nA
Drain OFF Leakage Current	MAX368	I _{D (OFF)}		V _D = ±10V V _S = ∓10V	1 2	-0.015	-2 200	-5 200	5 200	
	MAX369			V _D = ±10V V _S = ∓10V	1 2	-0.008	-1 100	-5 100	5 100	
Drain ON Leakage Current	MAX368	I _{D (ON)}	V _S = V _D = ±10V V _{EN} = 2.4V V _{AL} = 0.8V V _{AH} = 2.4V	1 2	-0.03	-2 200	-5 200	5 200		
	MAX369			1 2	-0.015	-1 100	-5 100	5 100		
LOGIC INPUT										
Logic Input Current (Input Voltage High)		I _{AH}	V _A = 2.4V	1, 2, 3	-0.002	-1	1	-1	1	µA
			V _A = 14V	1, 2, 3	0.006	-1	1	-1	1	
Logic Input Current (Input Voltage Low)		I _{AL}	V _{EN} = 0 or 2.4V, V _A = 0V RS = 0V, WR = 0V	1, 2, 3	-0.002	-1	1	-1	1	
FAULT										
Output Leakage Current (with Overvoltage)		I _{D (OFF)}	V _D = 0V (Note 3) Analog Overvoltage = ±33V	1 2		-10 -2000	10 2000	-20 -2000	20 2000	nA
Input Leakage Current (with Overvoltage)		I _{S (OFF)}	V _{IN} = ±25V, V _D = ±10V (Note 3)	1		-5	5	-10	10	µA
Input Leakage Current (with Power Supplies Off)		I _{D (OFF)}	V _{IN} = ±25V, V _{EN} = V _D = 0V A ₀ = A ₁ = A ₂ = 0V or 5V	1		-2	2	-5	5	µA

*1 = 25°C, 2 = 125°C, 85°C, 70°C, 3 = -55°C, -40°C, 0°C

Fault-Protected Analog Multiplexer with Latch

ELECTRICAL CHARACTERISTICS (continued)

(V⁺ = +15V, V⁻ = -15V; GND = 0, WR = 0, RS = 2.4V unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		TEMP *	TYP	M SUFFIX		E,C SUFFIX		UNITS
							MIN	MAX	MIN	MAX	
DYNAMIC											
Switching Time of Multiplexer		t _{TRANS}	See Figure 2		1	0.6	1		1		μs
Break-Before-Make Interval		t _{OPEN}	See Figure 4		1	0.2					
Enable and Write Turn ON Time		t _{ON} (EN, \overline{WR})	See Figures 3 and 5		1	1	1.5		1.5		
Enable and Reset Turn OFF Time		t _{OFF} (EN, \overline{RS})	See Figures 3 and 6		1	0.4	1		1		
Charge Injection		Q	See Figure 7 and Tables 1A and 1B		1	55					pC
OFF Isolation		OIRR	V _{EN} = 0, R _L = 1k Ω C _L = 15pF, V _{IN} = 7V _{RMS} f = 100kHz		1	68					dB
Logic Input Capacitance with Switch OFF		C _{IN}	f = 1MHz		1	5					pF
Input Capacitance with Switch OFF		C _{S(OFF)}	V _{EN} = 0 f = 140kHz	V _{IN} = 0	1	5					pF
Output Capacitance with Switch OFF	MAX368	C _{D(OFF)}		V _{OUT} = 0	1	25					
	MAX369				1	12					
\overline{WR} Pulse Width		t _{WW}	See Figure 1		1, 2, 3		300		300		ns
A _X , EN Data Valid to \overline{WR}		t _{DW}	Set-up Time See Figure 1		1, 2, 3		180		180		
A _X , EN Data Valid after \overline{WR}		t _{WD}	Hold Time See Figure 1		1, 2, 3	0	10		30		
\overline{RS} Pulse Width		t _{RS}	V _{IN} = 5V See Figure 1		1, 2, 3		300		500		
SUPPLY											
Positive Supply Current		I ⁺	V _{EN} = 2.4V, V _A = 0V/5V		1, 2, 3		1.25 1.5		1.5 2.0		mA
Negative Supply Current		I ⁻			1, 2, 3		-0.1 -0.2		-0.1 -0.2		

*1 = 25°C, 2 = 125°C, 85°C, 70°C, 3 = -55°C, -40°C, 0°C

Note 2: When the analog signal exceeds +13.5V or -12V, the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.

Note 3: The value shown is the steady state value. The transient leakage is typically 10μA. See detailed description.

Note 4: Electrical Characteristics, such as ON Resistance will change when power supplies other than ±15V are used.

Note 5: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

Fault-Protected Analog Multiplexer with Latch

TRUTH TABLE — MAX368

A ₂	A ₁	A ₀	EN	WR	RS	ON SWITCH
Latching						
X	X	X	X		1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

TRUTH TABLE — MAX369

A ₁	A ₀	EN	WR	RS	ON SWITCH
Latching					
X	X	X		1	Maintains previous switch condition
Reset					
X	X	X	X	0	NONE (latches cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

NOTE: Logic "1": $V_{AH} \geq 2.4V$, Logic "0": $V_{AL} \leq 0.8V$.

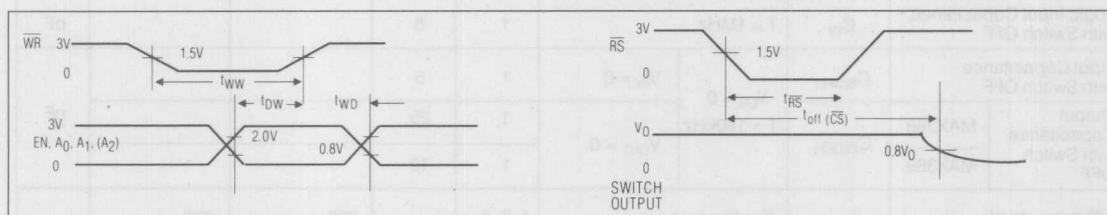


Figure 1. Typical Timing Diagrams for MAX368/369

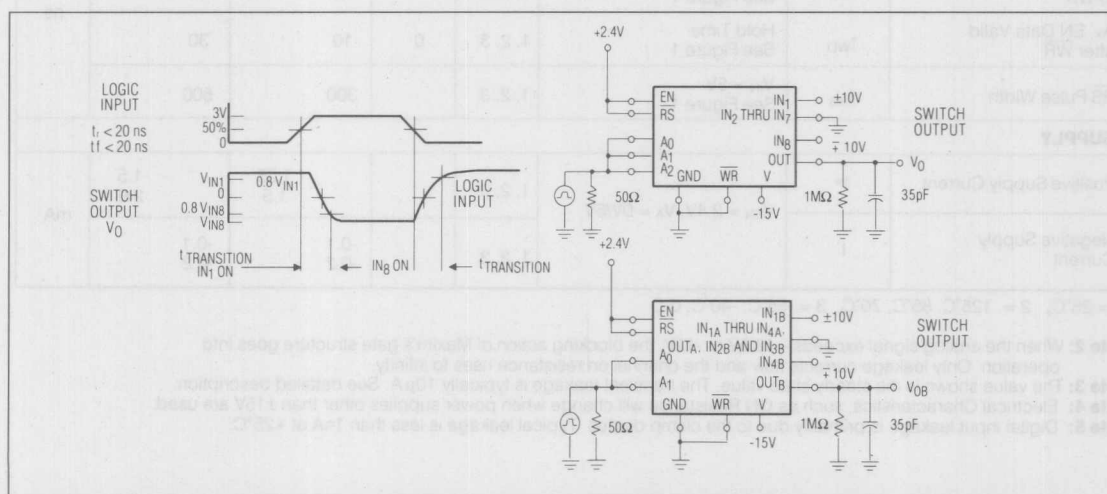


Figure 2. Transition Time Test Circuits

Fault-Protected Analog Multiplexer with Latch

MAX368/369

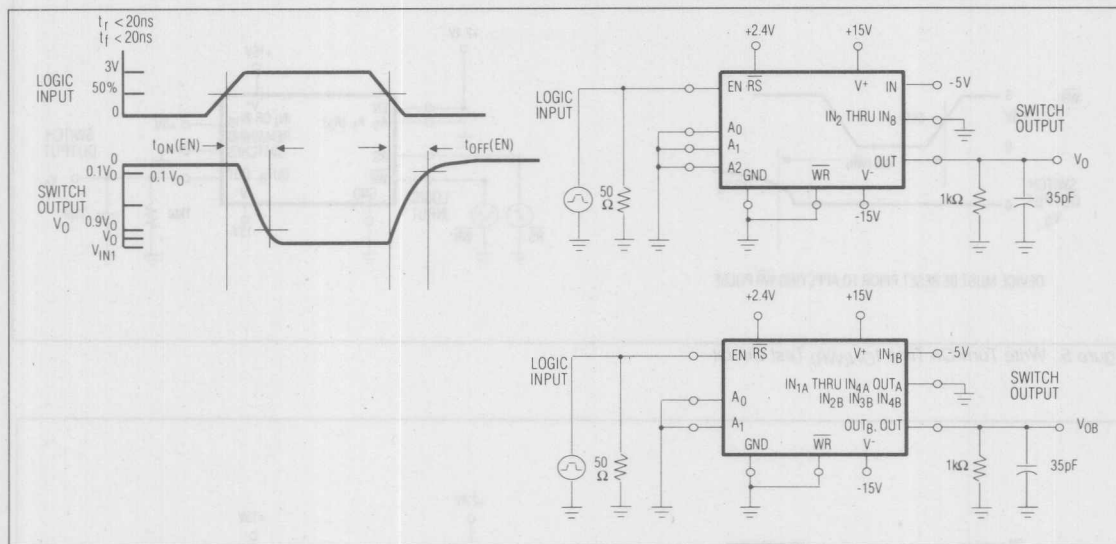


Figure 3. Enable t_{ON}/t_{OFF} Time Test Circuit

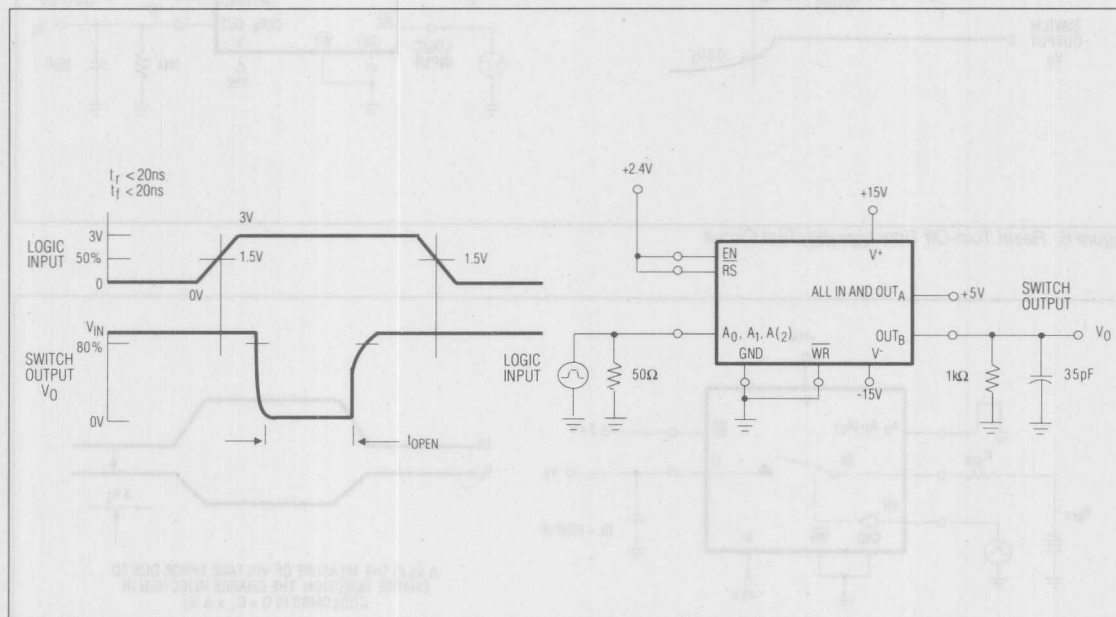


Figure 4. Open Time (B.B.M.) Interval Test Circuit

Fault-Protected Analog Multiplexer with Latch

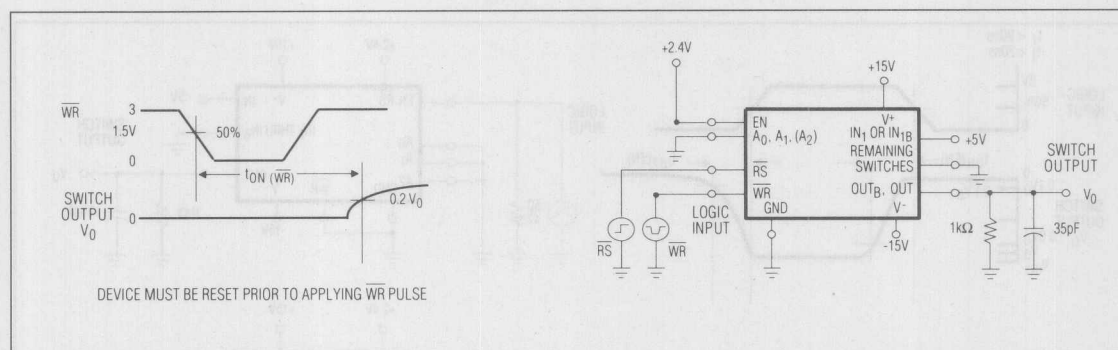


Figure 5. Write Turn-On Time $t_{ON}(WR)$ Test Circuit

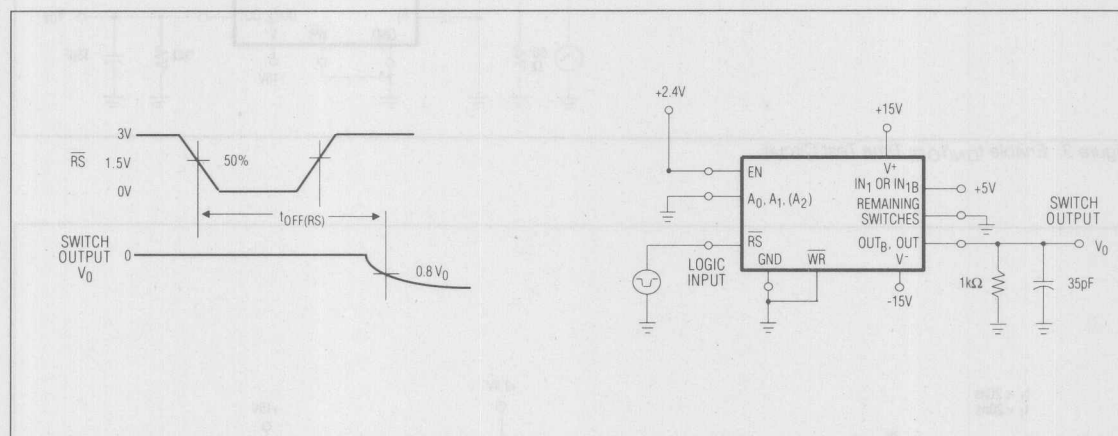


Figure 6. Reset Turn-Off Time $t_{OFF}(RS)$ Test Circuit

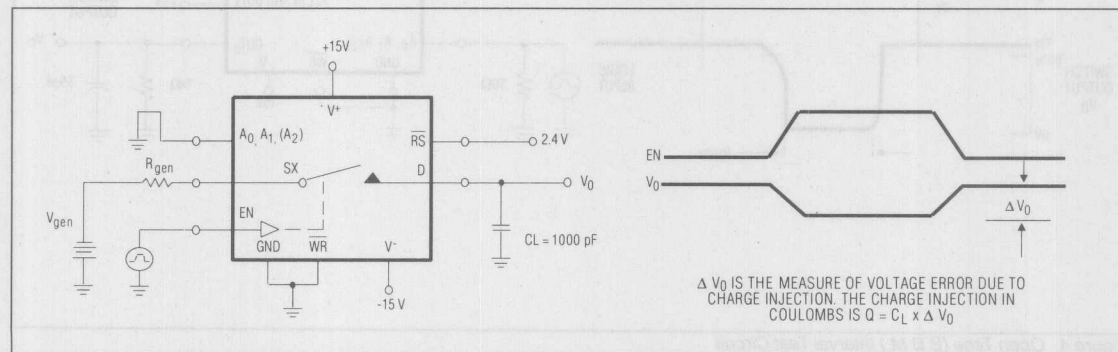


Figure 7. Charge Injection Test Circuit

Fault-Protected Analog Multiplexer with Latch

Detailed Description

Fault Protection Circuitry

Maxim's MAX368/369 are fully fault-protected for continuous input voltages up to $\pm 35V$, whether or not the $+V_{SUP}$ and $-V_{SUP}$ power supplies are present. These devices use a "series FET" protection scheme which not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels.

Figures 8 and 9 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all the FETs are at ground. With a $-25V$ input, N-channel FET Q1 is turned on by the $+25V$ gate-to-source voltage. The P-channel device (Q2), however, has $+25V$ V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is $+25V$, Q1 has a negative V_{GS} , which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any over voltage will turn off either Q1 or Q2.

Figure 10 shows the condition of an OFF channel with $+V_{SUP}$ and $-V_{SUP}$ present. As with Figures 8 and 9, either

an N-channel or a P-channel device will be off for any input voltage from $-35V$ to $+35V$. The leakage current with negative overvoltages will immediately drop to a few nanoamps at $25^\circ C$. For positive overvoltages the fault current will initially be 10 or $20\mu A$, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault protection scheme.

Figure 11 shows the condition of the ON channel with $+V_{SUP}$ and $-V_{SUP}$ present. With input voltages less than $\pm 10V$, all three FETs are on and the input signal appears at the output. If the input voltage exceeds $+V_{SUP}$ minus the N-channel threshold voltage (V_{TN}), then the N-channel FET will turn off. For voltages more negative than $-V_{SUP}$ minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically $1.5V$ and V_{TP} is typically $3V$, the multiplexer's output swing is limited to about $-12V$ to $+13.5V$ with $\pm 15V$ supplies

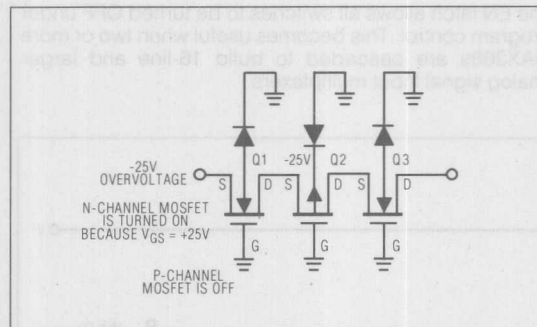


Figure 8. $-25V$ Overvoltage with Multiplexer Power OFF

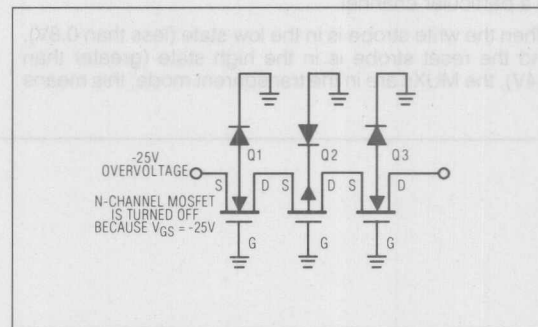


Figure 9. $+25V$ Overvoltage with Multiplexer Power OFF

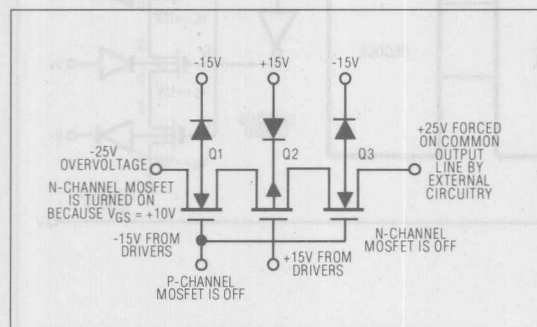


Figure 10. $-25V$ Overvoltage on an OFF Channel with Multiplexer Power Supply ON

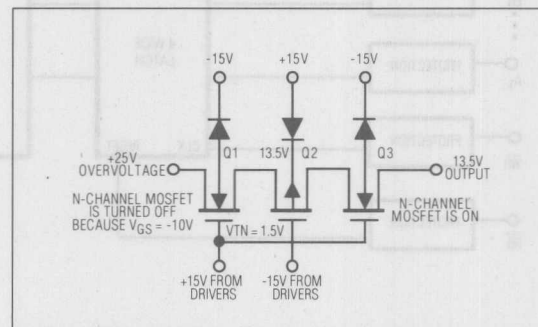


Figure 11. $+25V$ Overvoltage Input to the ON Channel

Fault-Protected Analog Multiplexer with Latch

The Typical Operating Characteristics graphs show typical leakage vs. input voltage curves. Although the maximum rated overvoltage of these devices is $\pm 35\text{V}$, the MAX368/369 typically has excellent performance up to $\pm 40\text{V}$, providing additional margin for the unknown transients that exist in the real world. In summary, the MAX368/369 provides superior protection from all fault conditions, while using a standard, readily produced junction isolated CMOS process.

Digital Control Circuitry

The internal structure of the MAX368/369 includes translators for the A₀, A₁, A₂, EN, RS, and WR digital inputs, latches, a decode section for channel selection (see Truth Tables on the fourth page of this data sheet). The gate structure consists of series N-channel/ P-channel/ N-channel MOSFETs (see Figure 12). This combination produces a very rugged, fault tolerant multiplexer with address latch capability, and does so with extremely low power dissipation.

Write ($\overline{\text{WR}}$), and Reset ($\overline{\text{RS}}$) strobes are provided for interfacing with microprocessor bus lines (Figure 13), alleviating the need for the microprocessor to provide constant address inputs to the MUX in order to hold on to a particular channel.

When the write strobe is in the low state (less than 0.8V), and the reset strobe is in the high state (greater than 2.4V), the MUXs are in the transparent mode; this means

that the MUXs act similar to non-latching MUXs such as the MAX358/359 or the HI-508A/509A.

When the write input goes to the high state (>2.4V), the previous BCD address input will be latched and held in that state indefinitely. To pull the MUX out of this state, either the write input (WR) must be taken low (0.8V), back to the transparent state, or the Reset (RS) input taken low, turning off all channels.

The function of the Reset input is to allow for turning off all channels when the RS input is low ($<0.8V$); this has the dual function of resetting channel selection back to the channel 1 mode.

The MAX368/369 is designed to work with single as well as dual supplies, and good performance can be expected in the 9V to 22V single supply range. For example, with a single +15V power supply, analog signals in the range of +3.3V to +12V can be switched normally, and overvoltages up to $\pm 35V$ can still be tolerated. If negative signals, around 0V are expected, a negative supply is needed. However, only -5V is needed to normally switch signals in the -2V to +12V range (-5V, +15V supplies). No current is drawn from the negative supply, so Maxim's MAX635 D/C to D/C converter does the job very nicely.

The EN latch allows all switches to be turned OFF under program control. This becomes useful when two or more MAX368s are cascaded to build 16-line and larger analog signal input multiplexers.

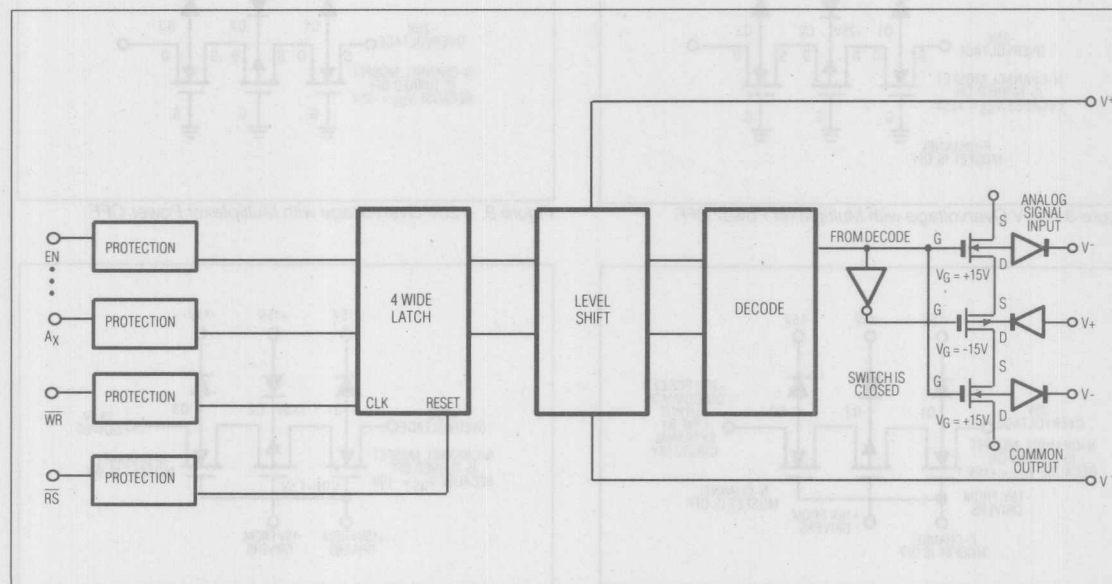
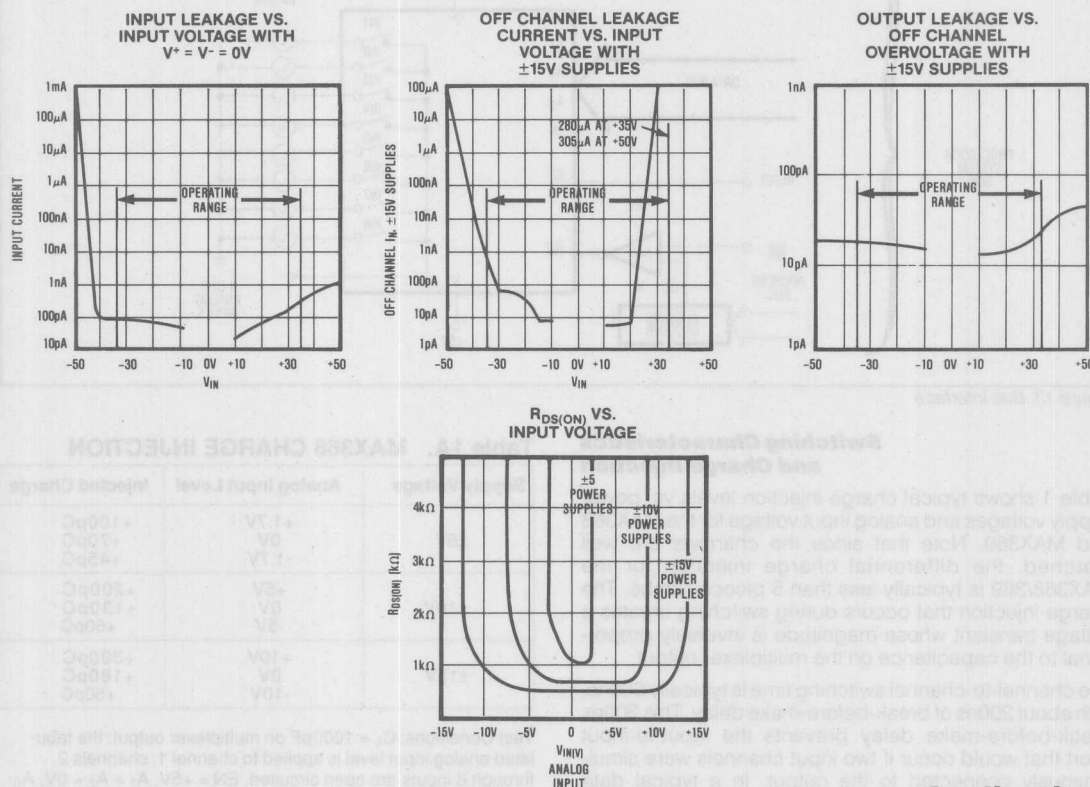


Figure 12. Simplified Internal Structure

Fault-Protected Analog Multiplexer with Latch

Typical Operating Characteristics



Operation with Supply Voltages Other than $\pm 15V$

The main effect of supply voltages other than $\pm 15V$ is the reduction in output signal range. The MAX368/369 limits the output voltage to about 1.5V below $+V_{SUP}$ and about 3V above $-V_{SUP}$. In other words, the output swing is limited to +3.5V to -2V when operating from $\pm 5V$. The Typical Operating Characteristics graphs show typical $R_{DS(ON)}$ for $\pm 15V$, $\pm 10V$, and $\pm 5V$ power supplies. Maxim guarantees the MAX368/369 for operation from $\pm 4.5V$ to $\pm 18V$ supplies. The switching delays increase by about a factor of 2 at $\pm 5V$, but break-before-make action is preserved.

The MAX368/369 can be operated with a single +9V to +22V supply, as well as asymmetrical power supplies such as +15V and -5V. The digital threshold will remain approximately 1.6V above the GROUND pin, and the analog characteristics such as $R_{DS(ON)}$ are determined

by the total voltage difference between $+V_{SUP}$ and $-V_{SUP}$. Connect $-V_{SUP}$ to 0V when operating with a +9V to +22V single supply.

The MAX368/369 digital threshold is relatively independent of the power supply voltages, going from a typical 1.6V when $+V_{SUP}$ is 15V to 1.5V typical with a 5V $+V_{SUP}$. This means that Maxim's MAX368/369 will operate with standard TTL logic levels, even with $\pm 5V$ power supplies. In all cases, the threshold of the Enable pin is the same as the other logic inputs.

Operation as a Demultiplexer

The MAX368/369 will function as a demultiplexer, where the input is applied to the Output pin, and the Input pins are used as outputs. The MAX368/369 provide both break-before-make action and full fault protection when operated as a demultiplexer, unlike earlier generations of fault protected multiplexers.

MAX368/369

8

Analog Multiplexer with Latch

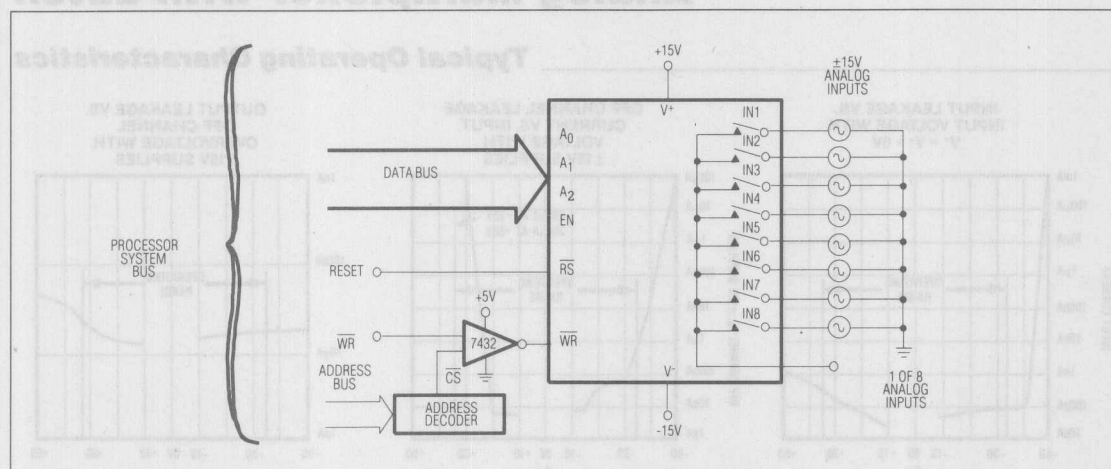


Figure 13. Bus Interface

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels vs. power supply voltages and analog input voltage for the MAX368 and MAX369. Note that since the channels are well matched, the differential charge injection for the MAX368/369 is typically less than 5 picocoulombs. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

The channel-to-channel switching time is typically 600ns, with about 200ns of break-before-make delay. This 200ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system such as that shown in Figure 13, the dominant delay is not the switching time of the MAX368/MAX369 multiplexer but is the settling time of the following amplifier and sample/hold. Another limiting factor is the RC time constant of the multiplexer $R_{DS(ON)}$ plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output approximately doubles the settling time for 0.01% accuracy settling.

Digital Interface Levels

The typical digital threshold of both the address lines and the enable pin is 1.6V, with a temperature coefficient of approximately $-3\text{mV}/^\circ\text{C}$. This ensures compatibility with 0.8V to 2.4V TTL logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from $\pm 15\text{V}$ to $\pm 5\text{V}$. In all cases, the digital threshold is referenced to the GROUND pin.

Table 1A. MAX368 CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge
$\pm 5\text{V}$	+1.7V 0V -1.7V	+100pC +70pC +45pC
$\pm 10\text{V}$	+5V 0V -5V	+200pC +130pC +60pC
$\pm 15\text{V}$	+10V 0V -10V	+300pC +180pC +50pC

Test Conditions: $C_L = 1000\text{pF}$ on multiplexer output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. $\text{EN} = +5\text{V}$, $A_1 = A_2 = 0\text{V}$, A_0 is toggled at 2kHz rate between 0V and 3V. +100 picocoulombs of charge creates a +100mV step when injected into a 1000pF load capacitance.

Table 1B. MAX369 CHARGE INJECTION

Supply Voltage	Analog Input Level	Injected Charge		
		Out A	Out B	Differential A - B
$\pm 5\text{V}$	+1.7V 0V -1.7V	+105pC +73pC +48pC	+107pC +48pC +50pC	-2pC -1pC -2pC
$\pm 10\text{V}$	+5V 0V -5V	+215pC +135pC +62pC	+220pC +139pC +63pC	-5pC -4pC -1pC
$\pm 15\text{V}$	+10V 0V -10V	+325pC +180pC +55pC	+330pC +185pC +55pC	-5pC -5pC 0pC

Test Conditions: $C_L = 1000\text{pF}$ on Out A and Out B; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. $\text{EN} = +5\text{V}$, $A_1 = 0\text{V}$, A_0 is toggled from 0V to 3V at a 2kHz rate.

Fault-Protected Analog Multiplexer with Latch

The digital inputs can also be driven with CMOS logic levels swinging from either +V_{SUP} to -V_{SUP} or from +V_{SUP} to Ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of 1μA. The digital inputs are protected from ESD by a 30V zener diode between the input and +V_{SUP}, and can be driven ±6V beyond the supplies without drawing excessive current.

Channel-to-Channel Crosstalk, Off Isolation and Digital Feedthrough

At DC and low frequencies, the channel-to-channel crosstalk is caused by variations in output leakage currents as the off channel input voltages are varied. The MAX368/369 output leakage varies only a few picoamps as all 7 off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX368/369 output, which is R_{DS(ON)} plus the input signal source resistance in most cases, since the load driven by the MAX368/369 is usually a high impedance. For a signal source impedance of 10kΩ or lower, the DC crosstalk exceeds 120dB.

Table 2 shows typical AC crosstalk and off isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled.

When the output is disabled, the digital feedthrough is virtually unmeasurable, since the digital pins are physically isolated from the analog section by the GROUND and -V_{SUP} pins. The groundplane formed by these lines is continued onto the MAX368/369 die to provide over 100dB isolation between the digital and analog sections.

**Table 2A. TYPICAL OFF ISOLATION
REJECTION RATIO**

Frequency	100kHz	500kHz	1MHz
One Channel Driven	74dB	72dB	66dB
All Channels Driven	64dB	48dB	44dB

Test Conditions: V_{IN} = 20V_{PK-PK} at the tabulated frequency, R_L = 1.5k between OUT and ground, EN = 0V.

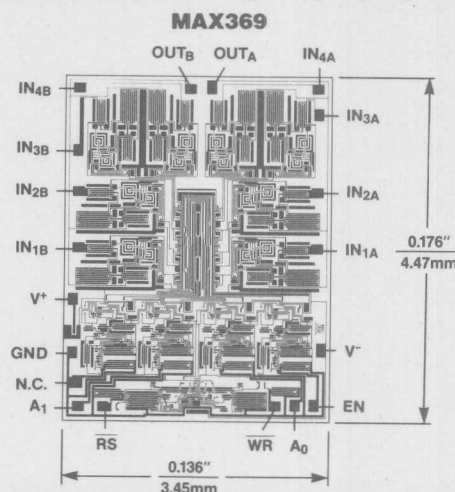
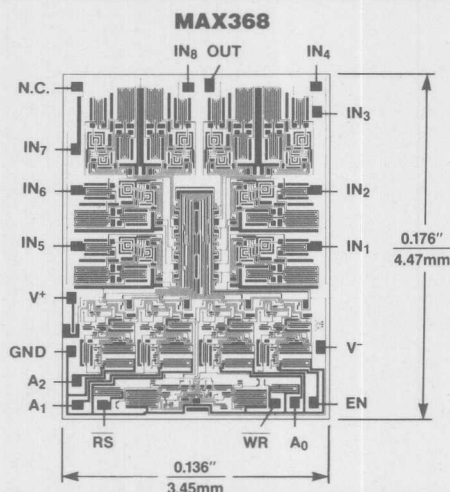
$$\text{OIRR} = 20 \text{ Log } \frac{20 \text{ V}_{\text{PK-PK}}}{V_{\text{OUT}} (\text{PK-PK})}$$

**Table 2B. TYPICAL CROSSTALK
REJECTION RATIO**

Frequency	100kHz	500kHz	1MHz
R _L = 1.5k	70dB	68dB	64dB
R _L = 10k	62dB	46dB	42dB

Test Conditions: Specified R_L connected from OUT to ground, EN = +5V, A₀ = A₁ = A₂ = 0V (Channel 1 selected). 20V_{PK-PK} at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

Chip Topographies



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM High Voltage, Fault-Protected Analog Multiplexers

General Description

Maxim's MAX378 is an 8 channel single-ended (1 of 8) multiplexer with fault protection, and the MAX379 is a 4 channel differential (2 of 8) multiplexer with fault protection. Using a series N-channel, P-channel, N-channel structure, these multiplexers provide significant fault protection. If the power supplies to the fault-protected multiplexers are inadvertently turned off while input voltages are still applied, all channels in the multiplexers are turned off, and only a few nanoamperes of leakage current will flow into the inputs. This protects not only the multiplexers and the circuitry driven by the multiplexers, but also protects the sensors or signal sources which drive the multiplexers.

The series N-channel, P-channel, N-channel protection structure has two significant advantages over the simple current limiting protection scheme of the industry's first generation fault-protected multiplexers. First, the Maxim protection scheme limits fault currents to nanoamp leakage values rather than many milliamperes. This prevents damage to sensors or other sensitive signal sources. Second, the MAX378/379 fault-protected multiplexers can withstand a continuous $\pm 60V$ input, unlike the first generation which had a continuous $\pm 35V$ input limitation imposed by power dissipation considerations.

All digital inputs have logic thresholds of 0.8V and 2.4V, ensuring both TTL and CMOS compatibility without requiring pullup resistors. Break-before-make operation is guaranteed. Power dissipation is less than 2 milliwatts.

Applications

Data Acquisition Systems
Industrial and Process Control Systems
Avionics Test Equipment
Signal routing between Systems

Features

- ◆ Fault Input Voltage $\pm 75V$ with Power Supplies Off
- ◆ Fault Input Voltage $\pm 60V$ with $\pm 15V$ Power Supplies
- ◆ All Switches Off with Power Supplies Off
- ◆ On Channel Turns OFF if Overvoltage Occurs on Input or Output
- ◆ Only Nanoamperes of Input Current Under All Fault Conditions
- ◆ No Increase in Supply Currents Due to Fault Conditions
- ◆ Latchup-proof Construction
- ◆ Operates From $\pm 4.5V$ to $\pm 18V$ Supplies
- ◆ All Digital Inputs are TTL and CMOS Compatible
- ◆ Low-Power Monolithic CMOS Design

Ordering Information

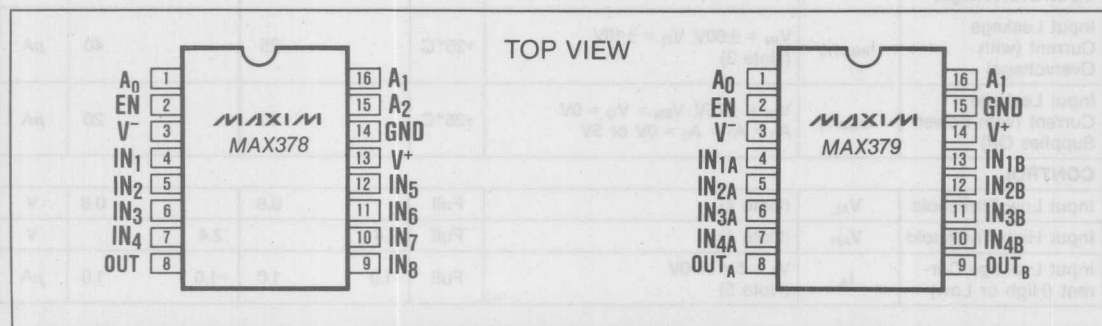
PART	TEMP. RANGE	PACKAGE
MAX378CPE	0°C to +70°C	16 Lead Plastic DIP
MAX378CWE	0°C to +70°C	16 Lead Wide SO
MAX378CJE	0°C to +70°C	16 Lead Cerdip
MAX378EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX378EWE	-40°C to +85°C	16 Lead Wide SO
MAX378EJE	-40°C to +85°C	16 Lead Cerdip
MAX378MJE	-55°C to +125°C	16 Lead Cerdip
MAX378MLP*	-55°C to +125°C	20 Lead LCC
MAX378C/D**	0°C to +70°C	Dice
MAX379CPE	0°C to +70°C	16 Lead Plastic DIP
MAX379CWE	0°C to +70°C	16 Lead Wide SO
MAX379CJE	0°C to +70°C	16 Lead Cerdip

Ordering Information continued on page 10.

* Contact Factory for availability.

** The substrate may be allowed to float or be tied to V⁺ (J1 CMOS).

Pin Configurations



MAXIM

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Maxim Integrated Products 8-15

MAX378/379

High Voltage, Fault-Protected Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins	+44V
V ⁺ to Ground	+22V
V ⁻ to Ground	-22V
Digital Input Overvoltage:	
V _{EN} , V _A { V ⁺	+4V
{ V ⁻	-4V
Analog Input with Multiplexer Power On	±65V
{ Recommended	V ⁺ +15V
{ Power Supplies	V ⁻ -15V
Analog Input with Multiplexer Power Off	±80V

Continuous Current, IN or OUT	20mA
Peak Current, IN or OUT	
(Pulsed at 1ms, 10% duty cycle max)	40mA
Power Dissipation (Note 1) (CERDIP)	1.28W
Operating Temperature Range:	
MAX378/379M	-55°C to +125°C
MAX378/379C	0°C to +70°C
MAX378/379E	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

Note 1: Derate 12.8mW/°C above T_A = +75°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V⁺ = +15V, V⁻ = -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +70°C and -40°C to +85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
STATIC										
ON Resistance	r _{DS(ON)}	V _{OUT} = ±10V, I _{IN} = 100μA V _{AL} = 0.8V, V _{AH} = 2.4V	+25°C Full		2.0 3.0	3.0 4.0		2.0 3.0	3.5 4.0	kΩ
OFF Input Leakage Current	I _{IN(OFF)}	V _{IN} = ± 10V, V _{OUT} = ∓10V V _{EN} = 0.8V (Note 6)	+25°C Full	-0.5 -50	0.03 50	0.5 50	-1.0 -50	0.03 50	1.0 50	nA
OFF Output Leakage Current	I _{OUT(OFF)}	V _{OUT} = ±10V, V _{IN} = ∓10V V _{EN} = 0.8V MAX378 MAX379	+25°C Full Full	-1.0 -200 -100	0.1 200 100	1.0 200 100	-2.0 -200 -100	0.1 200 100	2.0 200 100	nA
ON Channel Leakage Current	I _{OUT(ON)}	V _{IN(ALL)} = V _{OUT} = ±10V (Note 5) V _{AH} = V _{EN} = 2.4V V _{AL} = 0.8V MAX378 MAX379	+25°C Full Full	-2.0 -200 -100	0.1 200 100	2.0 200 100	-5.0 -200 -100	0.1 200 100	5.0 200 100	nA
Analog Signal Range	V _{AN}	(Note 2)	Full	-15		+15	-15		+15	V
Differential, OFF Out-put Leakage Current	I _{DIFF}	MAX379 only (Note 6)	Full	-50		50	-50		50	nA
FAULT										
Output Leakage Current (with Input Overvoltage)	I _{OUT(OFF)}	V _{OUT} = 0V (Note 3) V _{IN} = ±60V	+25°C Full		20	10		20	20	nA μA
Input Leakage Current (with Overvoltage)	I _{IN(OFF)}	V _{IN} = ±60V, V _O = ±10V (Note 3)	+25°C			25			40	μA
Input Leakage Current (with Power Supplies Off)	I _{IN(OFF)}	V _{IN} = ±75V, V _{EN} = V _O = 0V A ₀ = A ₁ = A ₂ = 0V or 5V	+25°C			10			20	μA
CONTROL										
Input Low Threshold	V _{AL}	(Note 4)	Full			0.8			0.8	V
Input High Threshold	V _{AH}	(Note 4)	Full	2.4			2.4			V
Input Leakage Current (High or Low)	I _A	V _A = 5V or 0V (Note 5)	Full	-1.0		1.0	-1.0		1.0	μA

High Voltage, Fault-Protected Analog Multiplexers

MAX378/379

ELECTRICAL CHARACTERISTICS (Continued)

(V⁺ = +15V, V⁻ = -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	-55°C to +125°C			0°C to +70°C and -40°C to +85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC										
Access Time	t _A	(Figure 1)	+25°C		0.5	1.0		0.5	1.0	μs
Break-Before-Make Delay (Figure 2)	t _{ON-tOFF}	V _{EN} = +5V, V _{IN} = ±10V A ₀ , A ₁ , A ₂ Strobed	+25°C	25	200		25	200		ns
Enable Delay (ON)	t _{ON(EN)}	(Figure 3)	+25°C Full		400	750 1000		400	1000 1500	ns
Enable Delay (OFF)	t _{OFF(EN)}	(Figure 3)	+25°C Full		300	500 1000		300	1000	ns
Settling Time (0.1%) (0.01%)	t _{SETT}		+25°C		1.2 3.5			1.2 3.5		μs
"OFF Isolation"	OFF _(ISO)	V _{EN} = 0.8V, R _L = 1kΩ, C _L = 15pF, V = 7V _{RMS} , f = 100kHz	+25°C	50	68		50	68		dB
Channel Input Capacitance	C _{IN(OFF)}		+25°C		5			5		pF
Channel Output Capacitance	C _{OUT(OFF)}	MAX378 MAX379	+25°C		25 12			25 12		pF
Digital Input Capacitance	C _A		+25°C		5			5		pF
Input to Output Capacitance	C _{DS(OFF)}		+25°C		0.1			0.1		pF
SUPPLY										
Positive Supply Current	I ⁺	V _{EN} = 0.8V, or 2.4V All V _A = 0V or 5V	+25°C Full		0.1 0.3	0.6 0.7		0.2 0.5	1.0 1.0	mA
Negative Supply Current	I ⁻	V _{EN} = 0.8V or 2.4V All V _A = 0V or 5V	+25°C Full		0.01 0.02	0.1 0.2		0.01 0.02	0.1 0.1	mA
Power Supply Range for Continuous Operation	V _{OP}	(Note 7)	+25°C	±4.5		±18	±4.5		±18	V

Note 2: When the analog signal exceeds +13.5V or -12V the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow and the channel on resistance rises to infinity.

Note 3: The value shown is the steady state value. The transient leakage is typically 50μA. See detailed description.

Note 4: Guaranteed by other static parameters.

Note 5: Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at +25°C.

Note 6: Leakage currents not tested at T_A = cold temp.

Note 7: Electrical characteristics, such as ON Resistance, will change when power supplies other than ±15V are used.

High Voltage, Fault-Protected Analog Multiplexers

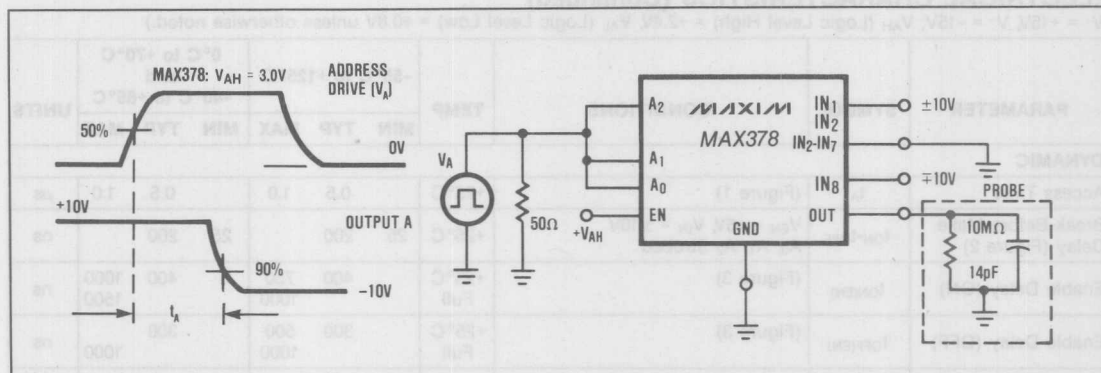


Figure 1. Access Time vs. Logic Level (High)

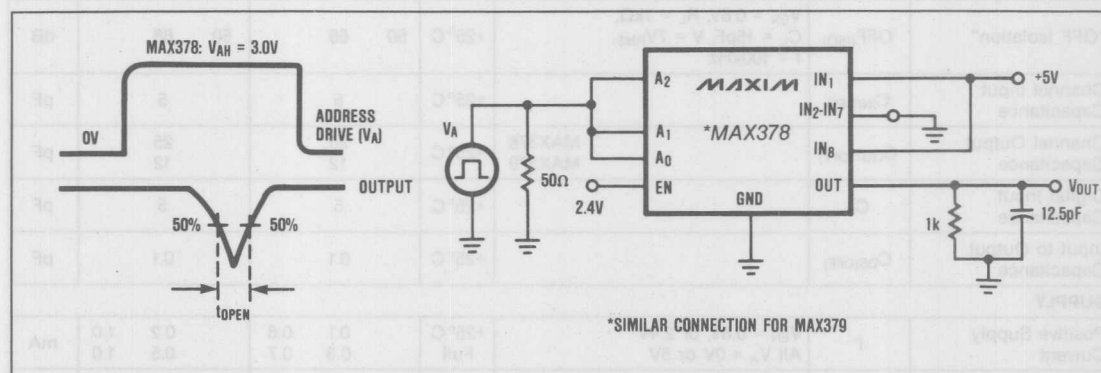


Figure 2. Break-Before-Make Delay (t_{OPEN})

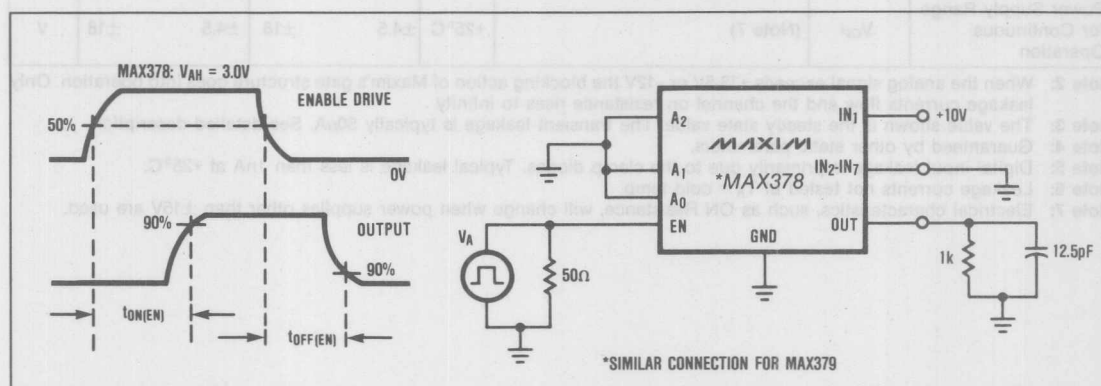


Figure 3. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)

High Voltage, Fault-Protected Analog Multiplexers

MAX378/379

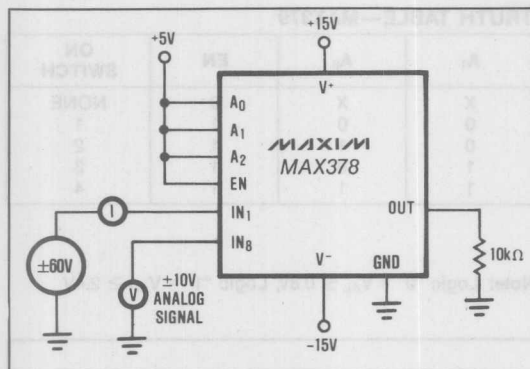


Figure 4. Input Leakage Current (Overvoltage)

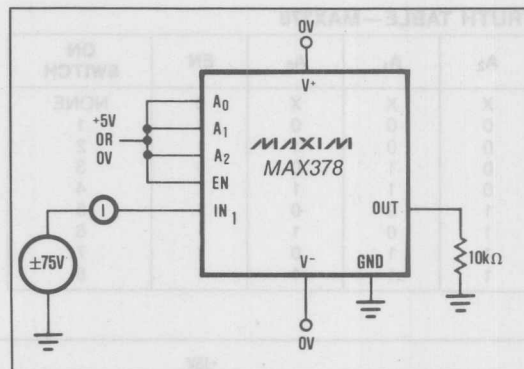
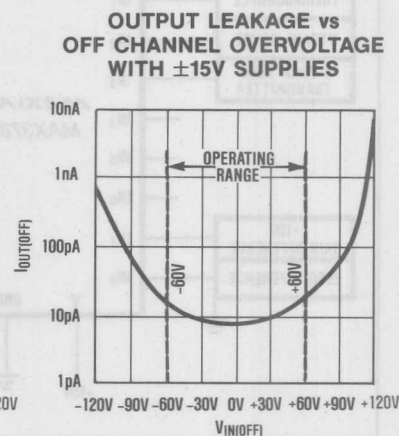
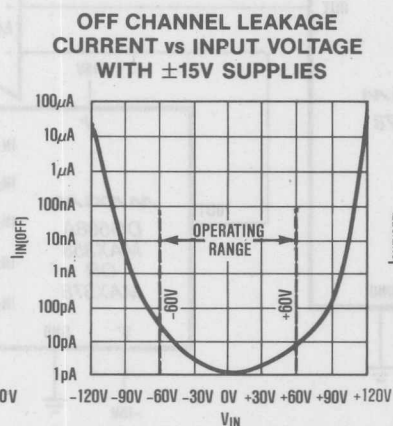
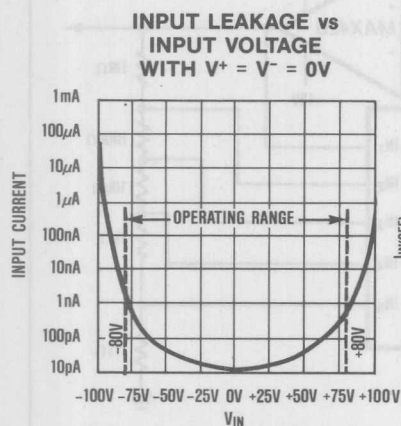
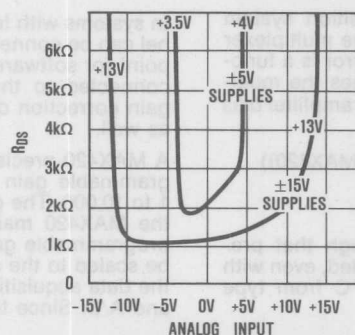


Figure 5. Input Leakage Current (with Power Supplies OFF)

Typical Operating Characteristics



$R_{DS(ON)}$ vs ANALOG INPUT VOLTAGE



NOTE: Typical $R_{DS(ON)}$ match @ +10V Analog in ($\pm 15V$ supplies) = 2% for lowest to highest $R_{DS(ON)}$ channel; @ -10V Analog in, match = 3%.

MAXIM

High Voltage, Fault Protected Analog Multiplexers

TRUTH TABLE—MAX378

A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE—MAX379

A ₁	A ₀	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Note: Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4V$

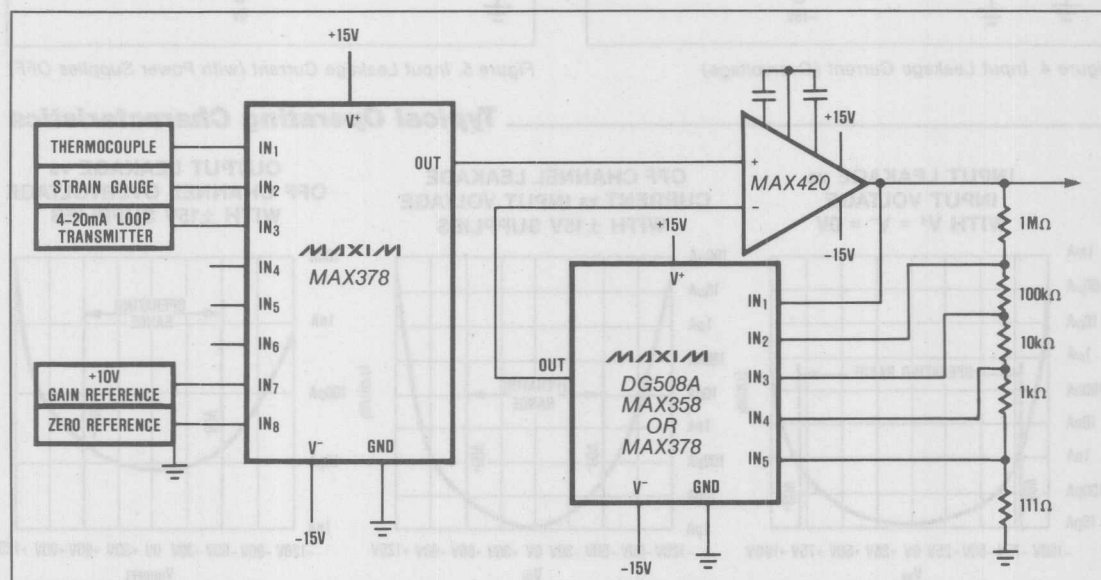


Figure 6. Typical Data Acquisition Front End

Typical Applications

Figure 6 shows a typical data acquisition system using the MAX378 multiplexer. Since the multiplexer is driving a high impedance input, its error is a function of its own resistance ($R_{DS(ON)}$) times the multiplexer leakage current ($I_{OUT(ON)}$) and the amplifier bias current (I_{BIAS}):

$$\begin{aligned} V_{ERR} &= R_{DS(ON)} \times (I_{OUT(ON)} + I_{BIAS} \text{ (MAX420)}) \\ &= 2.0k \times (2nA + 30pA) \\ &= 18.0\mu V \text{ maximum error} \end{aligned}$$

In most cases, this error is low enough that pre-amplification of input signals is not needed, even with very low level signals, such as $40\mu V/^\circ C$ from type J thermocouples.

In systems with fewer than 8 inputs, an unused channel can be connected to the system ground reference point for software zero correction. A second channel connected to the system voltage reference allows gain correction of the entire data acquisition system as well.

A MAX420 precision op amp is connected as a programmable gain amplifier, with gains ranging from 1 to 10,000. The guaranteed $5\mu V$ unadjusted offset of the MAX420 maintains high signal accuracy, while programmable gain allows the output signal level to be scaled to the optimum range for the remainder of the data acquisition system, normally a Sample/Hold and A/D. Since the gain-changing multiplexer is not

High Voltage, Fault-Protected Analog Multiplexers

MAX378/379

connected to the external sensors, it can be either a DG508A multiplexer or the fault protected MAX358 or MAX378.

Input switching, however, must be done with a fault-protected MAX378 multiplexer to provide the level of protection and isolation required with most data acquisition inputs. Since external signal sources may continue to supply voltage when the multiplexer and system power are turned off, non-fault protected multiplexers, or even first-generation fault protected devices, will allow many milliamps of fault current to flow from outside sources into the multiplexer. The result could be damage to either the sensors or the multiplexer. A non-fault protected multiplexer will also allow input overvoltages to appear at its output, perhaps damaging Sample/Holds or A/Ds. Such input overdrives may also cause input-to-input shorts, allowing the high current output of one sensor to possibly damage another.

The MAX378 eliminates all of the above problems since it not only limits its output voltage to safe levels, with or without power applied (V^+ and V^-), but also turns all channels off when power is removed, drawing only sub-microamp fault currents from the inputs, and maintaining isolation between inputs for continuous input levels up to $\pm 75V$ with power supplies off.

Detailed Description Fault Protection Circuitry

MAX378/379 are fully fault-protected for continuous input voltages up to $\pm 60V$, whether or not the V^+ and V^- power supplies are present. These devices use a "series FET" switching scheme which not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels.

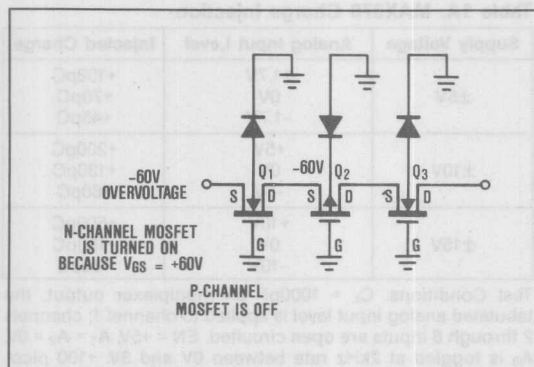


Figure 7. -60V Overvoltage with Multiplexer Power OFF

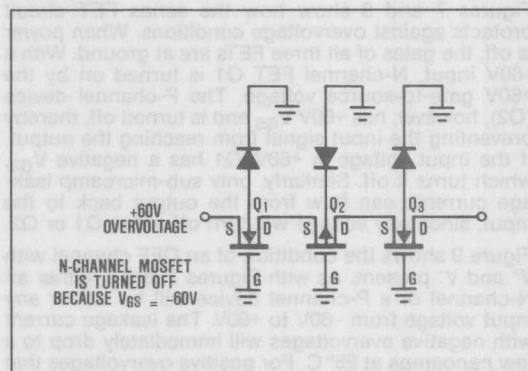


Figure 8. +60V Overvoltage with Multiplexer Power OFF

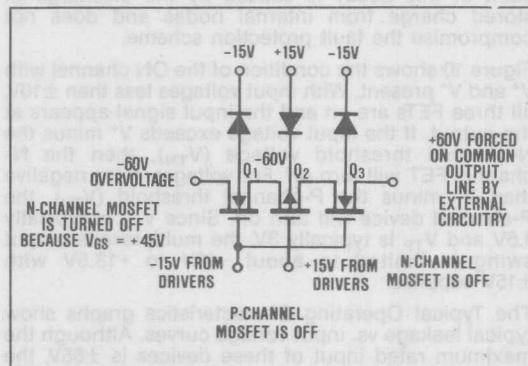


Figure 9. -60V Overvoltage on an OFF Channel with Multiplexer Power Supply ON

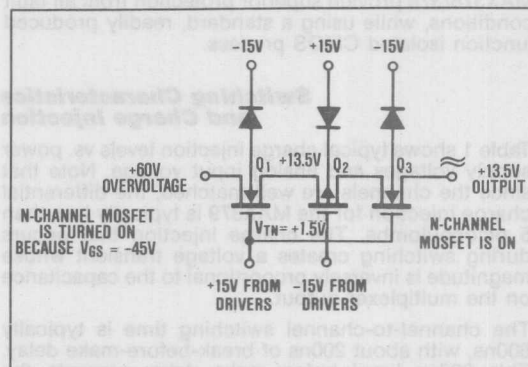


Figure 10. +60V Overvoltage Input to the ON Channel

High Voltage, Fault-Protected Analog Multiplexers

Figures 7 and 8 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all three FETs are at ground. With a -60V input, N-channel FET Q1 is turned on by the +60V gate-to-source voltage. The P-channel device (Q2), however, has +60V V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is +60V, Q1 has a negative V_{GS} , which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any voltage will turn off either Q1 or Q2.

Figure 9 shows the condition of an OFF channel with V^+ and V^- present. As with Figures 7 and 8, either an N-channel or a P-channel device will be off for any input voltage from -60V to +60V. The leakage current with negative overvoltages will immediately drop to a few nanoamps at 25°C. For positive overvoltages that fault current will initially be 40 or 50 μ A, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault protection scheme.

Figure 10 shows the condition of the ON channel with V^+ and V^- present. With input voltages less than $\pm 10V$, all three FETs are on and the input signal appears at the output. If the input voltage exceeds V^+ minus the N-channel threshold voltage (V_{TN}), then the N-channel FET will turn off. For voltages more negative than V^- minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically 1.5V and V_{TP} is typically 3V, the multiplexer's output swing is limited to about -12V to +13.5V with $\pm 15V$ supplies.

The Typical Operating Characteristics graphs show typical leakage vs. input voltage curves. Although the maximum rated input of these devices is $\pm 65V$, the MAX378/379 typically have excellent performance up to $\pm 75V$, providing additional margin for the unknown transients that exist in the real world. In summary, the MAX378/379 provide superior protection from all fault conditions, while using a standard, readily produced junction isolated CMOS process.

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels vs. power supply voltages and analog input voltage. Note that since the channels are well matched, the differential charge injection for the MAX379 is typically less than 5 picocoulombs. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

The channel-to-channel switching time is typically 600ns, with about 200ns of break-before-make delay. This 200ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system such as

Figure 6, the dominant delay is not the switching time of the MAX378 multiplexer, but is the settling time of the following amplifiers and S/H. Another limiting factor is the RC time constant of the multiplexer $R_{DS(ON)}$ plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output will approximately double the settling time to 0.01% accuracy.

Operation with Supply Voltage Other than $\pm 15V$

The main effect of supply voltages other than $\pm 15V$ is the reduction in output signal range. The MAX378 limits the output voltage to about 1.5V below V^+ and about 3V above V^- . In other words, the output swing is limited to +3.5V to -2V when operating from $\pm 5V$. The Typical Operating Characteristics graphs show typical $R_{DS(ON)}$ for $\pm 15V$, $\pm 10V$, and $\pm 5V$ power supplies. Maxim tests and guarantees the MAX378/379 for operation from $\pm 4.5V$ to $\pm 18V$ supplies. The switching delays are increased by about a factor of 2 at $\pm 5V$, but break-before-make action is preserved.

The MAX378/379 can be operated with a single +9V to +22V supply, as well as asymmetrical power supplies such as +15V and -5V. The digital threshold will remain approximately 1.6V above the Ground pin, and the analog characteristics such as $R_{DS(ON)}$ are determined by the total voltage difference between V^+ and V^- . Connect V^- to 0V when operating with a +9V to +22V single supply.

This means that the Maxim MAX378/379 will operate with standard TTL logic levels, even with $\pm 5V$ power supplies. In all cases, the threshold of the ENable pin is the same as the other logic inputs.

Table 1A. MAX378 Charge Injection

Supply Voltage	Analog Input Level	Injected Charge
$\pm 5V$	+1.7V	+100pC
	0V	+70pC
	-1.7V	+45pC
$\pm 10V$	+5V	+200pC
	0V	+130pC
	-5V	+60pC
$\pm 15V$	+10V	+500pC
	0V	+180pC
	-10V	+50pC

Test Conditions: $C_L = 1000pF$ on multiplexer output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. EN = +5V, $A_1 = A_2 = 0V$, A_0 is toggled at 2kHz rate between 0V and 3V. +100 picocoulombs of charge creates a +100mV step when injected into a 1000pF load capacitance.

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Table 1B. MAX379 Charge Injection

Supply Voltage	Analog Input Level	Injected Charge		
		Out A	Out B	Differential A-B
±5V	+1.7V	+105pC	+107pC	-2pC
	0V	+73pC	+74pC	-1pC
	-1.7V	+48pC	+50pC	-2pC
±10V	+5V	+215pC	+220pC	-5pC
	0V	+135pC	+139pC	-4pC
	-5V	+62pC	+63pC	-1pC
±15V	+10V	+525pC	+530pC	-5pC
	0V	+180pC	+185pC	-5pC
	-10V	+55pC	+55pC	0pC

Test Conditions: $C_L = 1000\text{pF}$ on Out A and Out B; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. EN = +5V, $A_1 = 0\text{V}$, A_0 is toggled from 0V to 3V at a 2kHz rate.

Digital Interface Levels

The typical digital threshold of both the address lines and the ENable pin is 1.6V, with a temperature coefficient of about $-3\text{mV}/^\circ\text{C}$. This ensures compatibility with 0.8V to 2.4V TTL logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from $\pm 15\text{V}$ to $\pm 5\text{V}$. In all cases, the digital threshold is referenced to the Ground pin.

The digital inputs can also be driven with CMOS logic levels swinging from either V^+ to V^- or from V^+ to Ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of $1\mu\text{A}$. The digital inputs are protected from ESD by a 30V zener diode between the input and V^+ , and can be driven $\pm 4\text{V}$ beyond the supplies without drawing excessive current.

Operation as a Demultiplexer

The MAX378/379 will function as a demultiplexer, where the input is applied to the Output pin, and the Input pins are used as outputs. The MAX378/379 provide both break-before-make action and full fault protection when operated as a demultiplexer, unlike earlier generations of fault protected multiplexers.

Channel-to-Channel Crosstalk, Off Isolation and Digital Feedthrough

At DC and low frequencies the channel-to-channel crosstalk is caused by variations in output leakage currents as the off channel input voltages are varied. The MAX378 output leakage varies only a few picoamps as all 7 off inputs are toggled from -10V to $+10\text{V}$. The output voltage change depends on the impedance level at the MAX378 output, which is $R_{DS(ON)}$ plus the input signal source resistance in most cases since the

load driven by the MAX378 is usually a high impedance. For a signal source impedance of $10\text{k}\Omega$ or lower, the DC crosstalk exceeds 120dB.

Table 2 shows typical AC crosstalk and off isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled. When the output is disabled, the digital feedthrough is virtually unmeasurable, since the digital pins are physically isolated from the analog section by the Ground and V^- pins. The groundplane formed by these lines is continued onto the MAX378/9 die to provide over 100dB isolation between the digital and analog sections.

Table 2A. Typical Off Isolation Rejection Ratio

Frequency	100kHz	500kHz	1MHz
One Channel Driven	74dB	72dB	66dB
All Channels Driven	64dB	48dB	44dB

Test Conditions: $V_{IN} = 20\text{V}_{PK-PK}$ at the tabulated frequency, $R_L = 1.5\text{k}$ between OUT and Ground, EN = 0V.

$$\text{OIRR} = 20 \log \frac{20\text{V}_{PK-PK}}{V_{OUT (PK-PK)}}$$

Table 2B. Typical Crosstalk Rejection Ratio

Frequency	100kHz	500kHz	1MHz
$F_L = 1.5\text{k}$	70dB	68dB	64dB
$R_L = 10\text{k}$	62dB	46dB	42dB

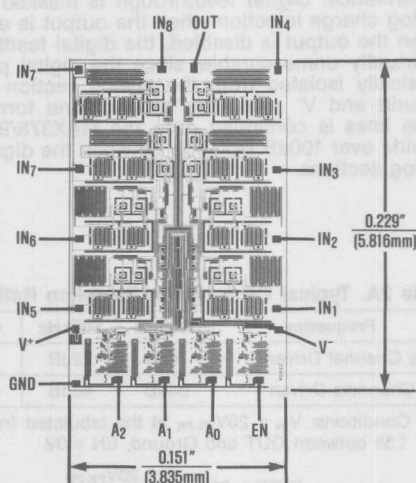
Test Conditions: Specified R_L connected from OUT to Ground, EN = +5V, $A_0 = A_1 = A_2 = +5\text{V}$ (Channel 1 selected). 20V_{PK-PK} at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

8

Analog Multiplexers

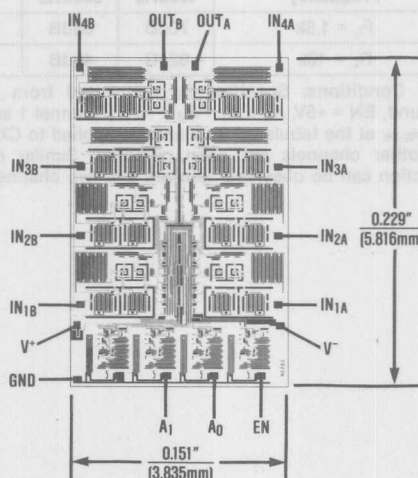
Chip Topographies

MAX378



NOTE: Connect substrate to V⁺ or leave it floating.

MAX379



NOTE: Connect substrate to V⁺ or leave it floating.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX379EPE	-40°C to +85°C	16 Lead Plastic DIP
MAX379EWE	-40°C to +85°C	16 Lead Wide SO
MAX379EJE	-40°C to +85°C	16 Lead CERPDP
MAX379MJE	-55°C to +125°C	16 Lead CERPDP
MAX379MLP*	-55°C to +125°C	20 Lead LCC
MAX379C/D**	0°C to +70°C	Dice

* Contact Factory for availability.

** The substrate may be allowed to float or be tied to V⁺ (JI CMOS).

parametric measurement capability has been specially designed by Maxim to make the precision measurement capability in analog circuits. We believe this quality control technology to be the best in the industry. capable of testing below 10A current levels and size than for capacitance. Maxim's proprietary software allows customer measurement of a wide range of parameters. Test source state delay and other parameters which are crucial to good long term stability and reliability.

Package Unit Process Flow	A-ii
Surface Mount Products	A-1
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Maxim U.S. Franchised Distributors	A-26
Maxim U.S. Chip Distributors	A-26
Maxim International Representatives	A-26

Product Conditioning and Qualification

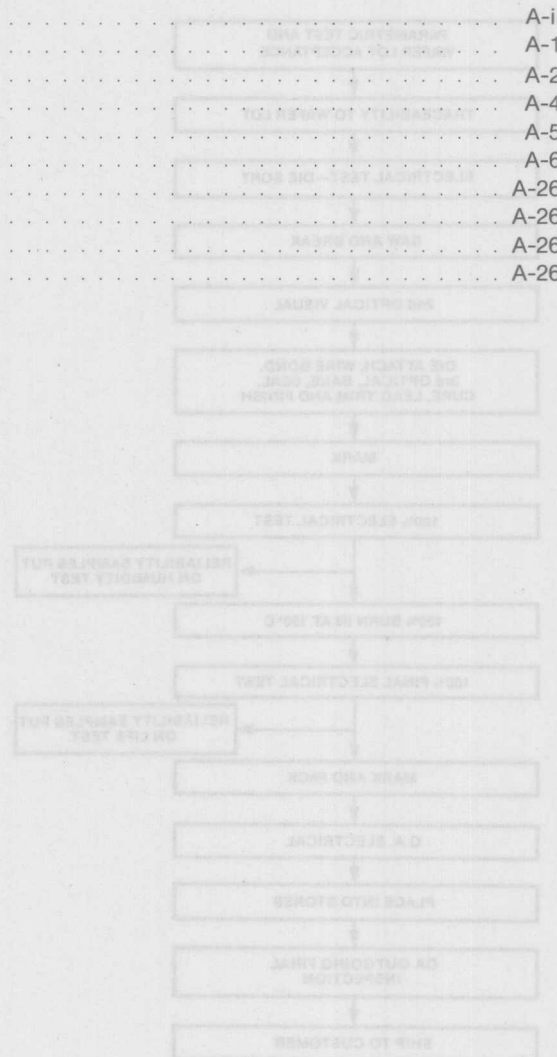
Reliability of Maxim's products is further assured by subjecting parts to qualification cycles that include accelerated life tests equivalent to 20 million operating hours, as well as pressure and humidity (85°C/85% humidity). In addition, every unit shipped has been tested in which the exception of reversed lead and surface Mount products—see below to further reduce the possibility of field failure.

Products processed to this level are normally available from other manufacturers at a price premium. By order, our special process flow, Maxim provides the testing and conditioning, including a 100% burn-in at no additional cost.

MAXIM

Appendix

Finished wafers are inspected optically to detect any physical defects. They are then parametrically tested to insure full conformity to Maxim's specifications. Our numerous in-process check-points for oxide thickness, critical dimensions, pin hole densities, and other parameters must comply with Maxim's design and physical specifications.



Package Unit Process Flow

Wafer Inspection

All wafers are fabricated using specifically developed processes with extremely tight control. Each must pass numerous in-process check-points for oxide thickness, critical dimensions, pin hole densities, and other requirements, and must comply with Maxim's demanding Electrical and Physical Specifications.

Finished wafers are inspected optically to detect any physical defects. Then they are parametrically tested to insure full conformity to Maxim's specifications. Our

parametric measurement capability has been specially designed by Maxim to make the precision measurements which are mandatory to insure reliability and reproducibility in analog circuits. We believe this quality control technology to be the best in the industry, capable of resolving below 1pA current levels, and less than 1pF capacitance. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface state density, and other parameters which are crucial to predicting long term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.

Testing

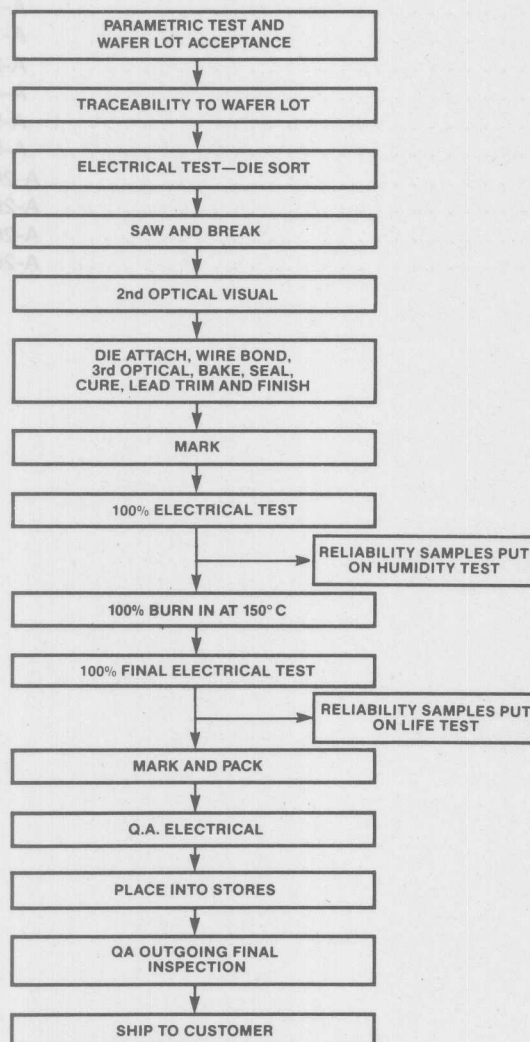
After wafer parametric inspection, each die is 100% tested prior to assembly. Once assembled, units are tested *over temperature*. This is not a common practice in the industry. By using the latest high speed automatic handling equipment, Maxim is able to offer "at temperature" testing for no additional cost.

Sophisticated testing is an integral part of delivering the highest quality data acquisition products. Maxim's analog test capability represents an order of magnitude improvement in accuracy, noise performance, and speed when compared to current industry standards. This provides the customer with total assurance that he will receive the part he paid for every time, without fail.

Product Conditioning and Qualification

Reliability of Maxim's products is further assured by subjecting parts to qualification cycles that include accelerated life tests equivalent to 20 million operating hours, as well as pressure and humidity ($85^{\circ}\text{C}/85\%$) cycles. In addition, *every unit shipped has been burned-in* (with the exception of reversed lead and Surface Mount Products—see below) to further reduce the possibility of field failure.

Products processed to this level are normally available from other manufacturers at a price premium, by ordering special process flows. *Maxim provides this testing and conditioning, including a 100% burn-in, at no additional cost.*



Surface Mount Products

Maxim is committed to providing high quality, high reliability 8 to 60 lead plastic surface mount products. With few exceptions, every monolithic product will be offered in a surface mount package. These products are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested

Pin Convention

0.150" JEDEC SOIC (S) parts have the same pinout as in the 0.300" DIP package equivalents.

0.300" JEDEC SOIC (W) parts also have the same pinout as in the 0.300" DIP package except for selected products in the 16 lead, 14 lead products that are too large for the 0.150" 14 lead (S) package are made available in the 0.300" 16 lead (W) package.

Flatpack Pin Convention

No fixed convention exists for 40-lead products assembled in either 44-lead or 60-lead flatpack. Consult product marketing for specific pin-outs.

to the same stringent electrical and visual AQL levels, with the exception of 100% burn-in and cold test. They receive the same product conditioning and lot qualification as the DIPs. Maxim still assures the reliability of every lot by subjecting a sample from each lot to a long term life test prior to shipment.

Quad Pack Pin Convention

- 1.) Devices in the 28 Lead Quad Pack are pin for pin number compatible with the DIP package. That is to say, pin 1 on the 28L Quad will be the same function as pin 1 on the DIP package.
- 2.) All 40 Lead devices planned for the 44 Lead Quad pack will have the following pin convention:

DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#
	1 N/C		12 N/C		23 N/C		34 N/C
1	2	11	13	21	24	31	35
2	3	12	14	22	25	32	36
3	4	13	15	23	26	33	37
4	5	14	16	24	27	34	38
5	6	15	17	25	28	35	39
6	7	16	18	26	29	36	40
7	8	17	19	27	30	37	41
8	9	18	20	28	31	38	42
9	10	19	21	29	32	39	43
10	11	20	22	30	33	40	44

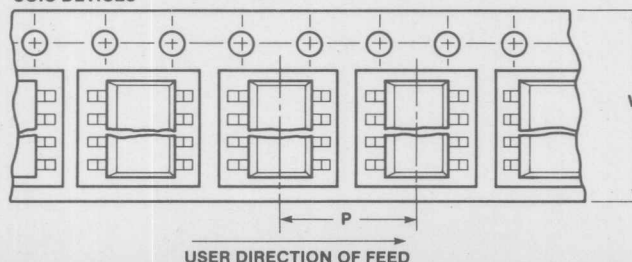
Surface Mount Packages In Reeled Tape

Maxim surface mount packages are normally shipped in antistatic plastic rails. They are also available mounted in pockets on embossed tape for customers using automatic placement systems. The tape is wound and shipped on reels.

The following table and diagrams indicate the tape sizes used for the various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT	TAPE SIZE mm (W)	PART PITCH mm (P)
SOIC	8L	12
	14L	16
	16L	16
SOIC	16L	16
	18L	24
	20L	24
	24L	24
	28L	24
PLCC	28L	24
	44L	32
PFP	44L	24
	60L	44

SOIC DEVICES



All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow" the standard to ensure lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet 25°C worst case parameters.

Generally, the parameters or parameter limits listed in the packaged unit data sheets are tested during electrical probe. However some parameters are impossible to test or test with absolute accuracy on unassembled product. Information regarding any of these parameters/parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	3"	4"	UNITS
Chip Thickness Backlapped wafers	13 ± 1	15 ± 1	mils
Die length/width tolerance	± 1		mils
Bonding pads dimensions (minimum)	4.0 x 4.0		mils
Bonding pad and interconnect material thickness	10K-15K		A
Storage temperature	-40 to +150		°C
Operating temperature	-20 to +70		°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010.2, Condition B with modifications reflecting CMOS requirements.

Each die surface is protected by a planar passivation layer and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by HF etching or by plasma etching. The bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.

Maxim guarantees die and wafer AQL levels as follows:

Visual	1.0%
Functional Electrical Testing	0.65%
Parametric DC Testing	2.5%
Untested Parameters	6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry ambient—preferably inert gas. Extreme care should be taken when handling die. Both electrical and visual damage can occur as a result of an unclean environment or harsh handling techniques.

Die Attach

To prevent oxidization the die attach operation should be done under a gaseous nitrogen ambient atmosphere. If an eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C.

Bonding

Thermosonic or thermocompression gold ball bonding may be used with 1.0 or 1.3 mil diameter 99.99% pure gold wire. Ultrasonic bonding may be used with 1.0 or 1.25 mil diameter 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Die and wafers are packaged as shown in Figures 1 and 2, respectively.

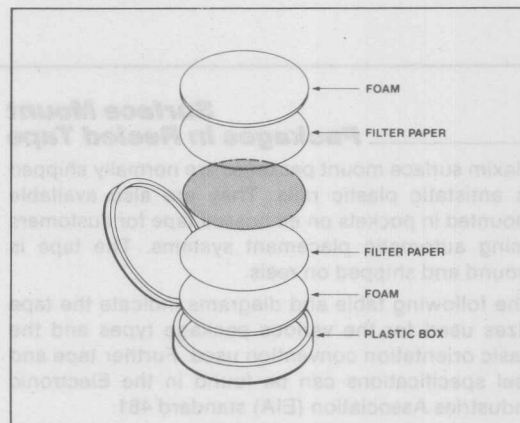


Figure 1. Wafer Carrier Package

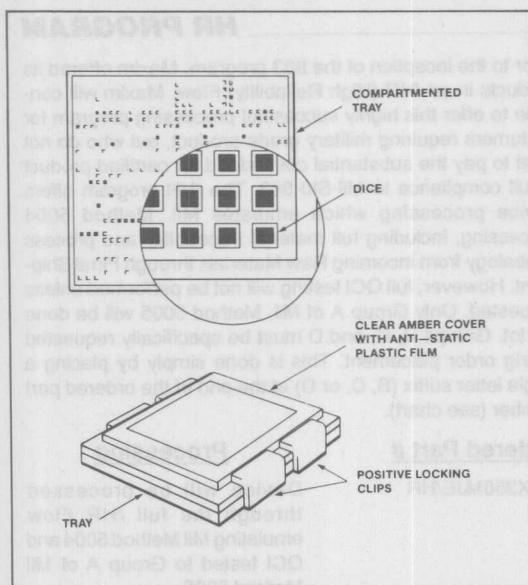


Figure 2. Die Carrier Package

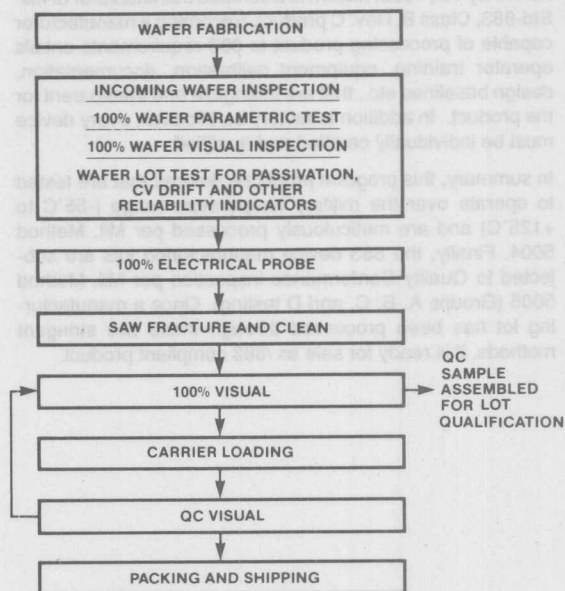
Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

User Responsibility

Written notification of any non-conformance by Maxim or Maxim's dice specifications must be made within 75 days of the shipment date of the die to the user. Maxim assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

Dice Process Flow



Ordering Information

Die orders are identified by a /D suffix.

Example: ICL7109C/D

When ordering die in wafer form replace "D" in the part numbers with a "W"

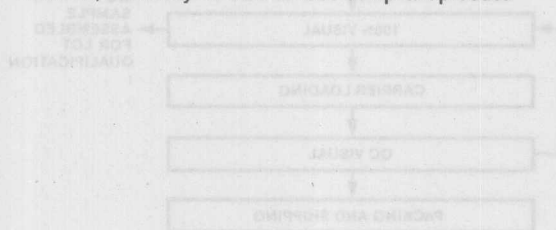
Example: MAX7231C/D Die = MAX7231C/W Wafer.

Maxim's /883 and /HR Program

883 PROGRAM

As of July 1st, 1988, Maxim is a certified manufacturer of Mil-Std-883, Class B, Rev. C product. Becoming a manufacturer capable of processing product to 883 requirements entails operator training, equipment calibration, documentation, design baselines etc., that are intangible and transparent for the product. In addition to factory certification, every device must be individually certified and qualified.

In summary, this program produces devices that are tested to operate over the military temperature range (-55°C to +125°C) and are meticulously processed per Mil. Method 5004. Finally, the 883 device manufacturing lots are subjected to Quality Conformance inspection per Mil. Method 5005 (Groups A, B, C, and D testing). Once a manufacturing lot has been processed through these two stringent methods, it is ready for sale as /883 compliant product.



Ordering Information
 The order is identified by a 4D suffix
 Example: ICL100CVD
 When ordering die in water form replace "D" in the part number with a "W"
 Example: MAX3231C D Die - MAX3231CW Water

HR PROGRAM

Prior to the inception of the 883 program, Maxim offered its products in an /HR (High Reliability) Flow. Maxim will continue to offer this highly successful processing program for customers requiring military grade product, but who do not want to pay the substantial cost added for certified product in full compliance to Mil-Std-883. The /HR program offers device processing which emulates Mil. Method 5004 processing, including full material traceability and process genealogy from Incoming Raw Materials through Final Shipment. However, full QCI testing will not be performed unless requested. Only Group A of Mil. Method 5005 will be done per lot. Groups B, C, and D must be specifically requested during order placement. This is done simply by placing a single letter suffix (B, C, or D) at the end of the ordered part number (see chart).

Ordered Part

MAX358MJE/HR

MAX358MJE/HRB

MAX358MJE/HRC

MAX358MJE/HRD

Processing

Device will be processed through the full /HR Flow emulating Mil Method 5004 and QCI tested to Group A of Mil Method 5005.

Same as above with the addition of Mil Method 5005 Group B testing. QCI contains both Group A and B.

Same as above except now QCI includes Group C. QCI now contains Groups A, B, and C.

Same as above except now QCI includes Group D. QCI now contains Groups A, B, C, and D.

To order /883 or /HR devices, contact the Maxim sales representative or distributor in your area.

Proprietary and Second Source Numbering System

Maxim's Proprietary Numbering System

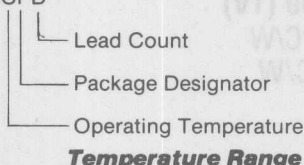
Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped by their functions into certain categories. Maxim presently uses a "MAX" as the prefix to the device's unique number. The categories are as follows:

MAX100-199	Analog-to-Digital Converters
MAX200-299	Interface
MAX300-399	Analog Switches and Multiplexers
MAX400-499	Op-Amps, Buffers and Video Amplifiers
MAX500-599	Digital-to-Analog Converters
MAX600-699	Power Supply Circuits and Voltage References
MAX700-799	μ P Peripherals and Display Drivers
MAX800-899	Open
MAX900-999	Open

Within each category, blocks of numbers are reserved for sub-groups.

3 Letter Suffixes

EXAMPLE: MAX358CPD



Temperature Range

"C"	0°C to +70°C
"I"	-20°C to +85°C
"E"	-40°C to +85°C
"M"	-55°C to +125°C

Package

"A"	TO-237
"C"	TO-220
"D"	Ceramic Sidebrase
"F"	Ceramic Flat-Pack
"H"	TO-66
"J"	CERDIP Dual-In-Line
"K"	TO-3
"L"	Leadless, Ceramic
"M"	Plastic Flat Pack
"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	Plastic Chip Carrier (Quad Pak)
"R"	Narrow CERDIP (24 pin, 0.3" wide)
"S"	Small Outline, Slim (8 or more leads), 150 mil
"S"	TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-78, TO-99, TO-100)
"U"	TO-72 Type (also TO-18, TO-71)
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"Z"	TO-92
"D"	Dice
"W"	Wafer
"-1"	On Package Information Indicates Hybrid Circuit

Number of Pins

"A"	8	"P"	20
"B"	10	"Q"	2
"C"	12	"R"	3
"D"	14	"S"	4
"E"	16	"T"	6
"F"	22	"U"	60
"G"	24	"V"	8 (0.200" pin circle, isolated case)
"H"	44	"W"	10 (0.230" pin circle, isolated case)
"I"	28	"Y"	8 (0.200" pin circle, case to pin 4)
"J"	32	"Z"	10 (0.230" pin circle, case to pin 5)
"L"	40		
"M"	48		
"N"	18		

4 Letter Suffixes

The first letter of the suffix is used to denote product grade, for example, MAX631ACPA means 5% output accuracy (A), the remaining 3 letters denote temperature range, package type and number of leads. Therefore, the MAX631ACPA operates over the 0°C to +70°C and is in a Plastic Dual-in-Line package and has 8 leads.

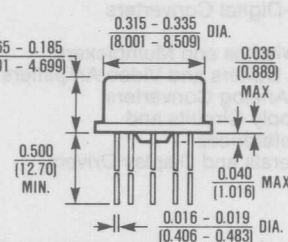
Second Source Products

In most cases, Maxim's part number for a multiple source product follows the numbering system that is most widely accepted in the industry for that particular part, rather than our own convention. This includes original designators for package type, temperature range, and performance grades as well as the most commonly recognized prefix.

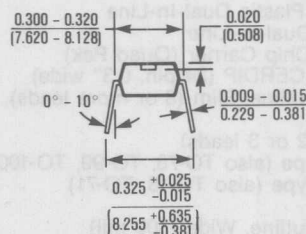
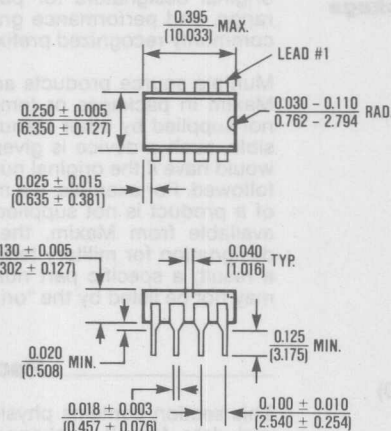
Multiple source products are frequently supplied by Maxim in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, such a device is given the part number that it would have if the original numbering convention were followed. For example, if a military temperature grade of a product is not supplied by other sources but is available from Maxim, the original manufacturer's designation for military temperature will be used. As a result, a specific part number supplied by Maxim may not be listed by the "original" manufacturer.

Package Information

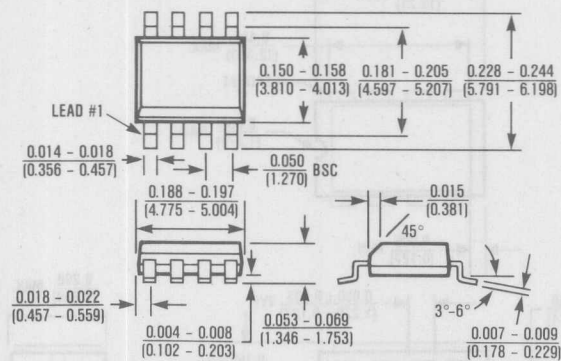
This section contains physical dimensions and thermal data for all packages currently supplied by Maxim. Each drawing is followed by a two letter code which indicates package type (Plastic DIP, Small Outline, etc.) and number of leads. This code is also used, along with indicators for temperature range and device grade (where appropriate) in the part number suffix for each of Maxim's proprietary devices.


$$\theta_{JA} = 150^{\circ}\text{C/W}$$
$$\theta_{JC} = 45^{\circ}\text{C/W}$$

— 30 — 15 5/11


$$\theta_{JA} = 120^{\circ}\text{C/W}$$
 $\theta_{JC} = 70^{\circ}\text{C/W}$

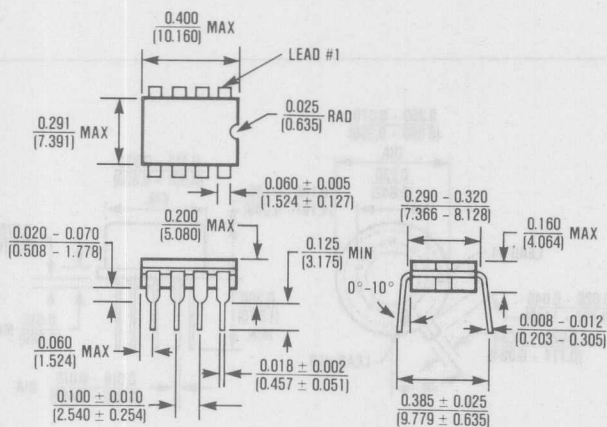
90



8 Lead Small Outline (SA)

$$\theta_{JA} = 170^{\circ}\text{C/W}$$

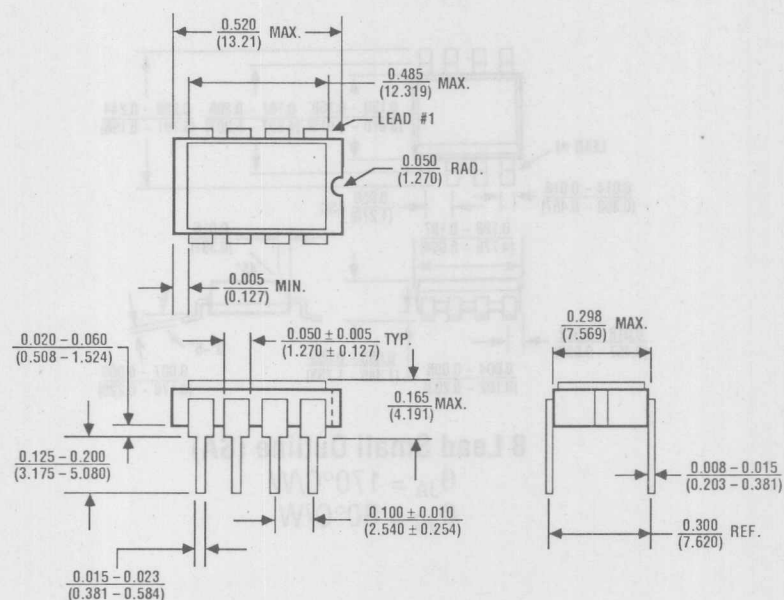
$$\theta_{JC} = 80^{\circ}\text{C/W}$$



8 Lead Cerdip (JA)

$$\theta_{JA} = 125^{\circ}\text{C/W}$$

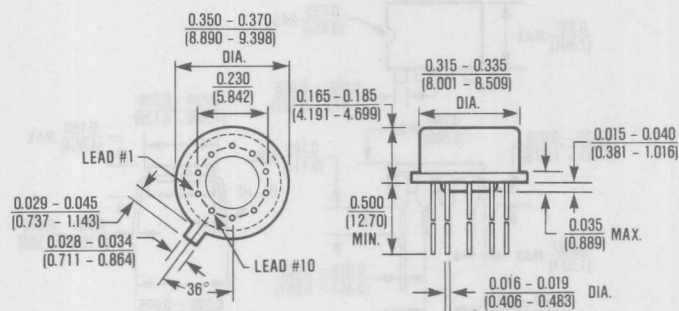
$$\theta_{JC} = 55^{\circ}\text{C/W}$$



8 Lead Ceramic Sidebrazed (DA)

$$\theta_{JA} = 120^{\circ}\text{C/W}$$

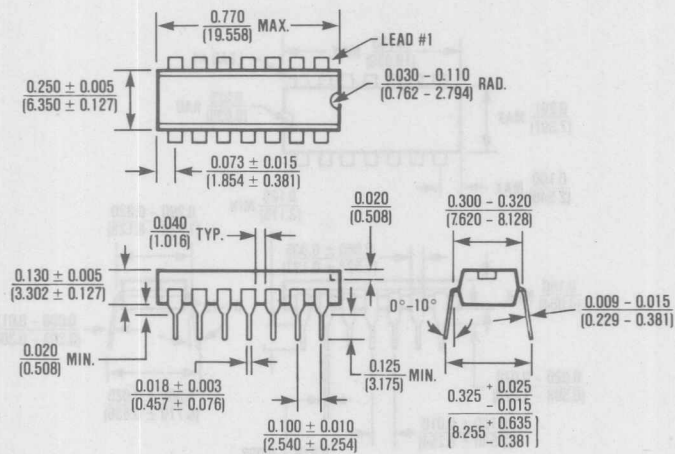
$$\theta_{JC} = 50^{\circ}\text{C/W}$$



10 Lead TO-100 Can (TW)

$$\theta_{JA} = 150^{\circ}\text{C/W}$$

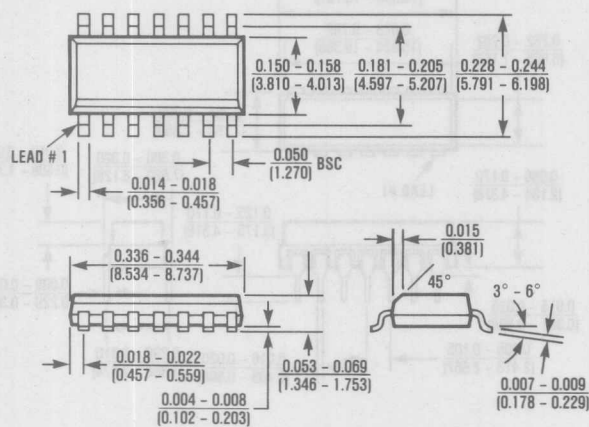
$$\theta_{JC} = 45^{\circ}\text{C/W}$$



14 Lead Plastic DIP (PD)

$$\theta_{JA} = 140^\circ\text{C/W}$$

$$\theta_{JC} = 70^\circ\text{C/W}$$

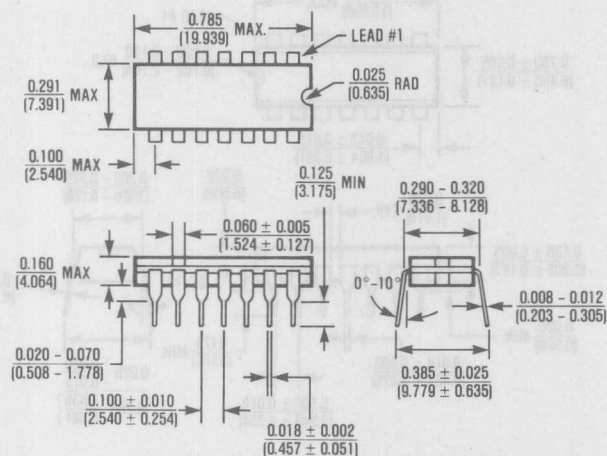


14 Lead Small Outline (SD)

$$\theta_{JA} = 115^\circ\text{C/W}$$

$$\theta_{JC} = 60^\circ\text{C/W}$$

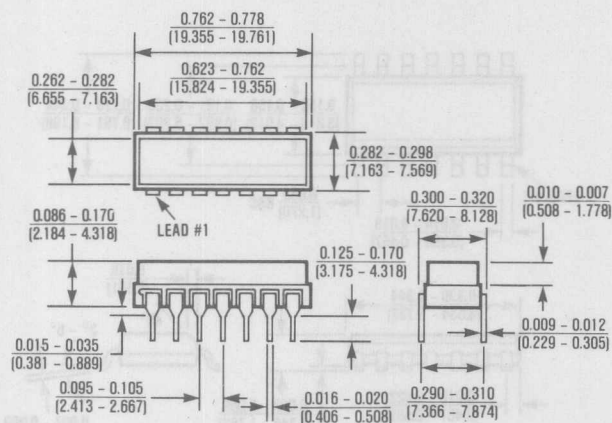
Package Information



14 Lead Cerdip (JD)

$$\theta_{JA} = 105^\circ\text{C/W}$$

$$\theta_{JC} = 50^\circ\text{C/W}$$

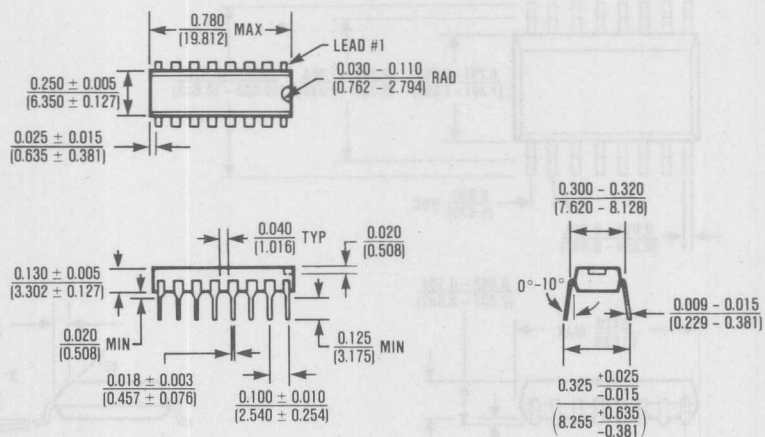


14 Lead Ceramic Sidebrazed (DD) -1

$$\theta_{JA} = 100^\circ\text{C/W}$$

$$\theta_{JC} = 45^\circ\text{C/W}$$

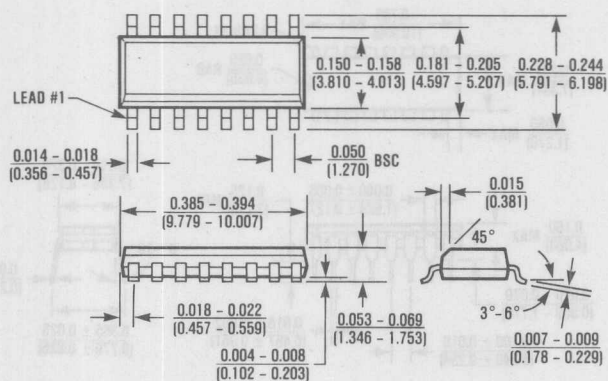
Package Information



16 Lead Plastic DIP (PE)

$$\theta_{JA} = 135^\circ\text{C/W}$$

$$\theta_{JC} = 65^\circ\text{C/W}$$

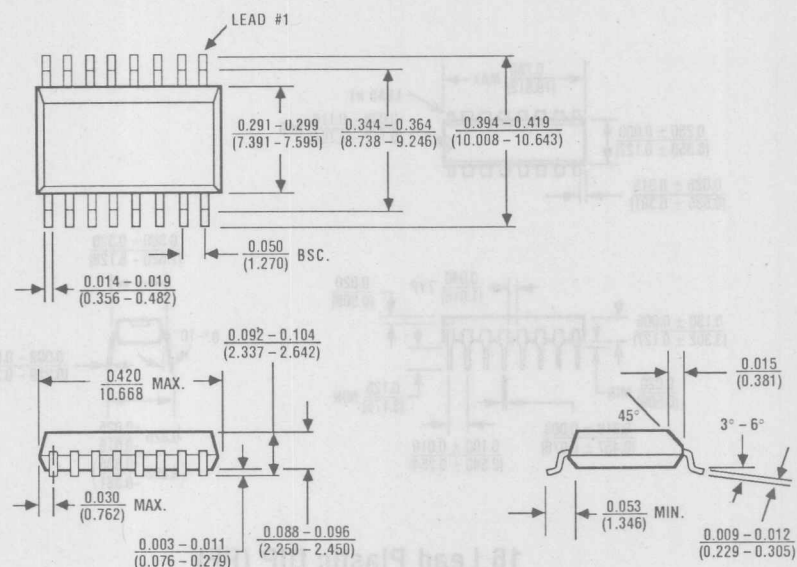


16 Lead Small Outline (SE)

$$\theta_{JA} = 110^\circ\text{C/W}$$

$$\theta_{JC} = 60^\circ\text{C/W}$$

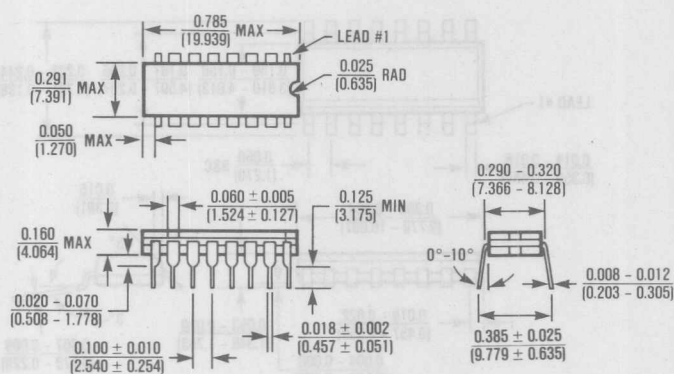
Package Information



16 Lead Small Outline, Wide (WE)

$$\theta_{JA} = 105^{\circ}\text{C/W}$$

$$\theta_{JC} = 60^{\circ}\text{C/W}$$

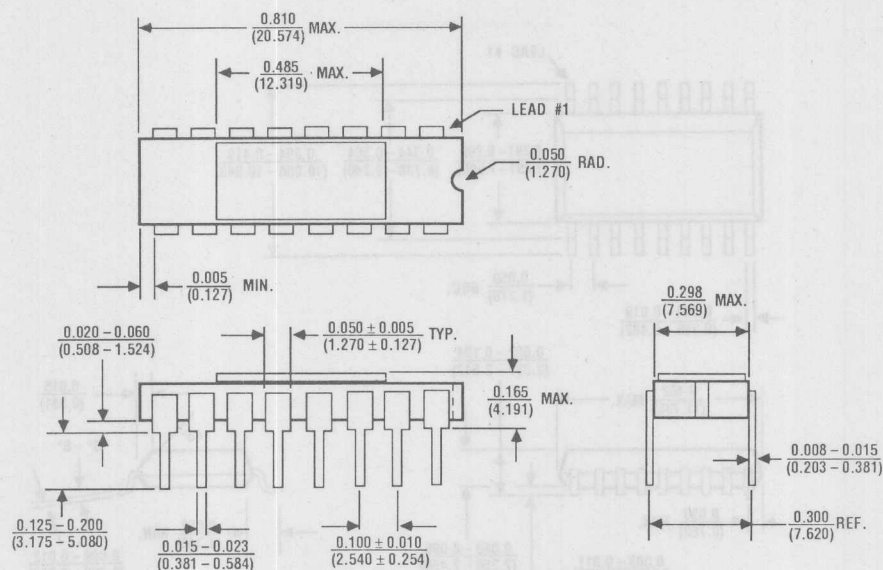


16 Lead Cerdip (JE)

$$\theta_{JA} = 100^{\circ}\text{C/W}$$

$$\theta_{JC} = 50^{\circ}\text{C/W}$$

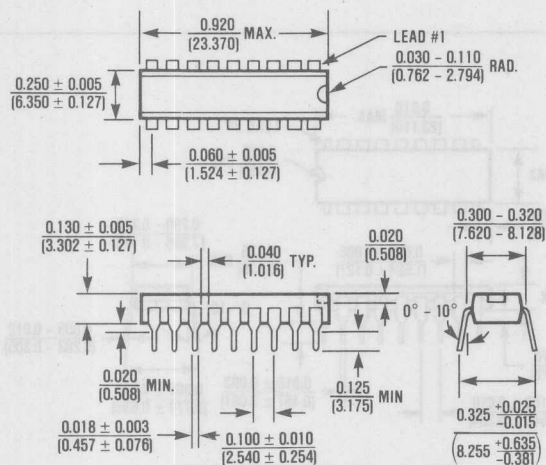
Package Information



16 Lead Ceramic Sidebrazed (DE)

$$\theta_{JA} = 95^{\circ}\text{C/W}$$

$$\theta_{JC} = 45^{\circ}\text{C/W}$$

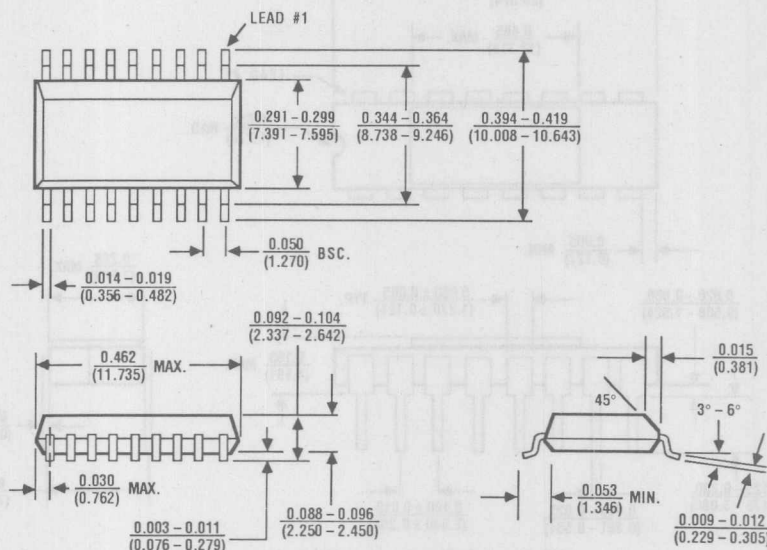


18 Lead Plastic DIP (PN)

$$\theta_{JA} = 130^{\circ}\text{C/W}$$

$$\theta_{JC} = 60^{\circ}\text{C/W}$$

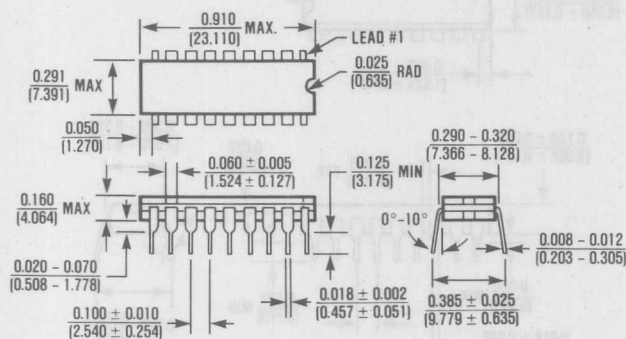
Package Information



18 Lead Small Outline, Wide (WN)

$$\theta_{JA} = 105^{\circ}\text{C/W}$$

$$\theta_{JC} = 60^{\circ}\text{C/W}$$

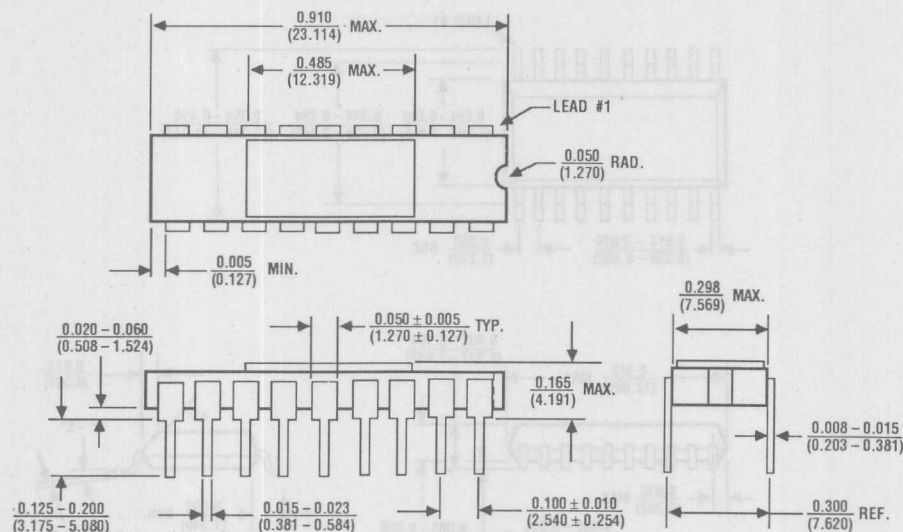


18 Lead Cerdip (JN)

$$\theta_{JA} = 90^{\circ}\text{C/W}$$

$$\theta_{JC} = 45^{\circ}\text{C/W}$$

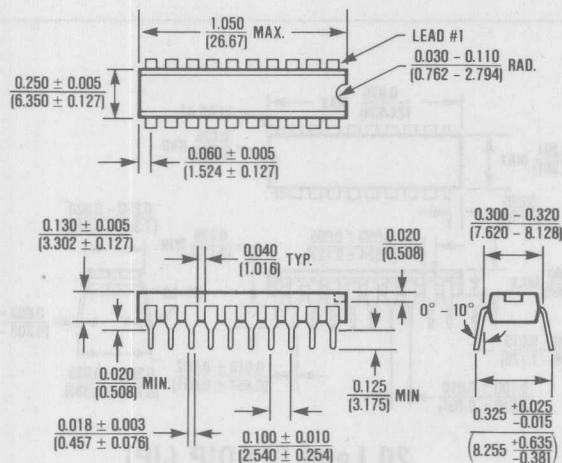
Package Information



18 Lead Ceramic Sidebrazed (DN)

$$\theta_{JA} = 90^{\circ}\text{C/W}$$

$$\theta_{JC} = 40^{\circ}\text{C/W}$$

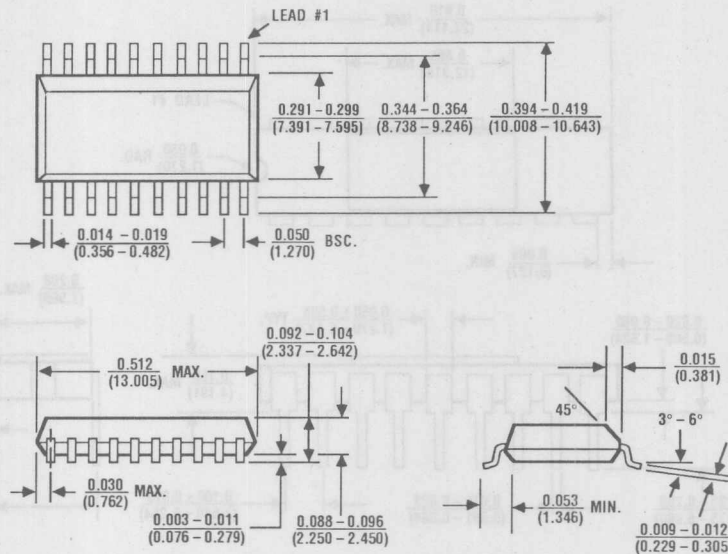


20 Lead Plastic DIP (PP)

$$\theta_{JA} = 125^{\circ}\text{C/W}$$

$$\theta_{JC} = 60^{\circ}\text{C/W}$$

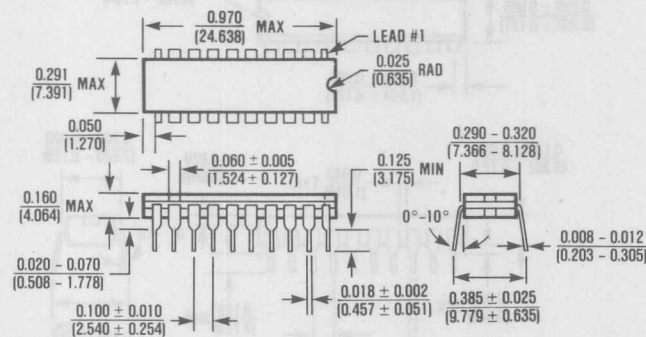
Package Information



20 Lead Small Outline, Wide (WP)

$$\theta_{JA} = 100^{\circ}\text{C/W}$$

$$\theta_{JC} = 50^{\circ}\text{C/W}$$

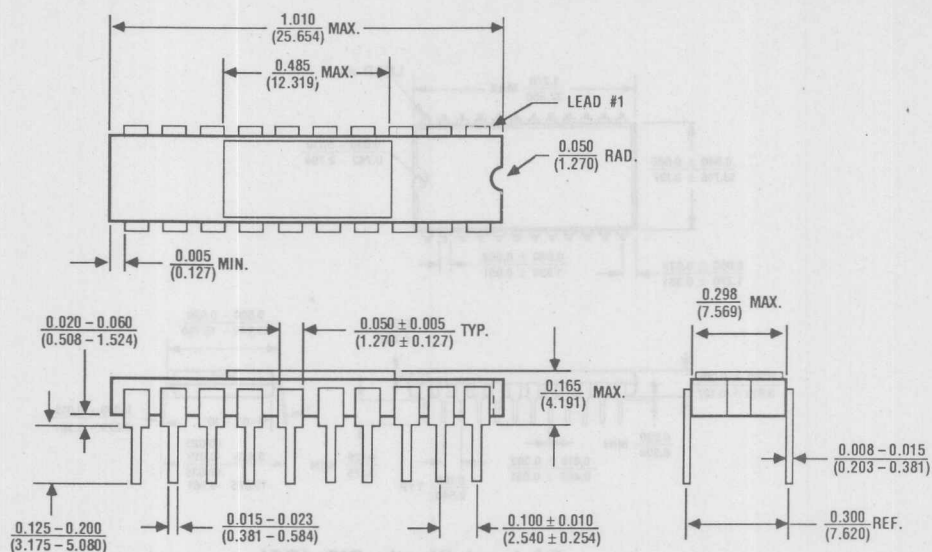


20 Lead Cerdip (JP)

$$\theta_{JA} = 90^{\circ}\text{C/W}$$

$$\theta_{JC} = 40^{\circ}\text{C/W}$$

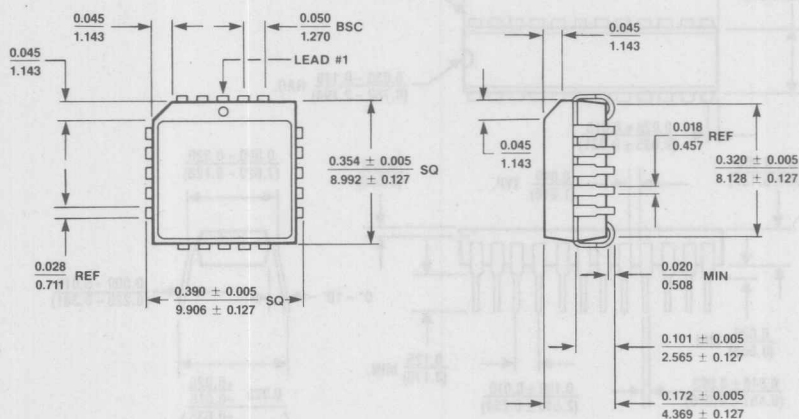
Package Information



20 Lead Ceramic Sidebrazed (DP)

$$\theta_{JA} = 85^{\circ}\text{C/W}$$

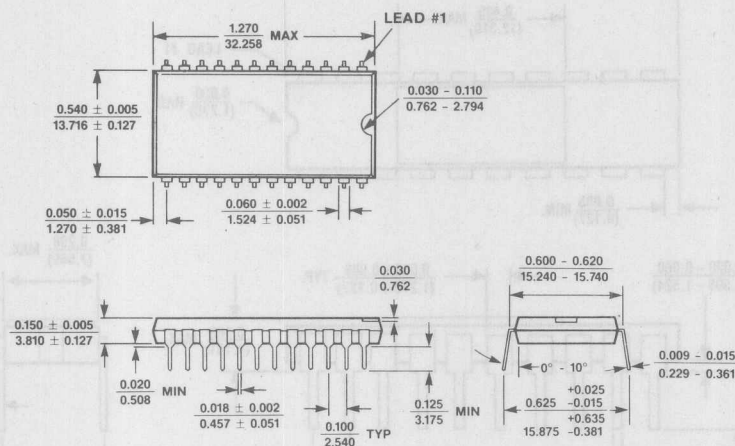
$$\theta_{JC} = 35^{\circ}\text{C/W}$$



20 Lead Plastic Chip Carrier (Quad Pak) (QP)

$$\theta_{JA} = 110^{\circ}\text{C/W}$$

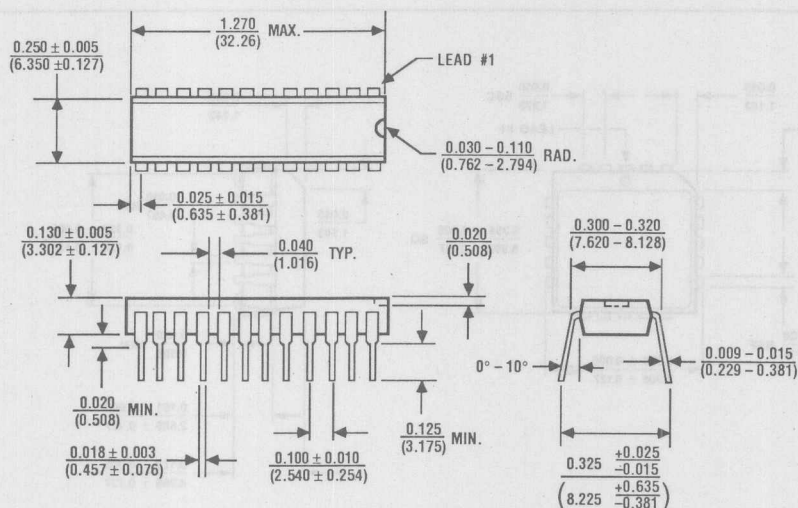
$$\theta_{JC} = 50^{\circ}\text{C/W}$$



24 Lead Plastic DIP (PG)

$$\theta_{JA} = 110^\circ\text{C/W}$$

$$\theta_{JC} = 50^\circ\text{C/W}$$

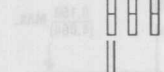


24 Lead Plastic Narrow DIP (NG)

$$\theta_{JA} = 120^\circ\text{C/W}$$

$$\theta_{JC} = 60^\circ\text{C/W}$$

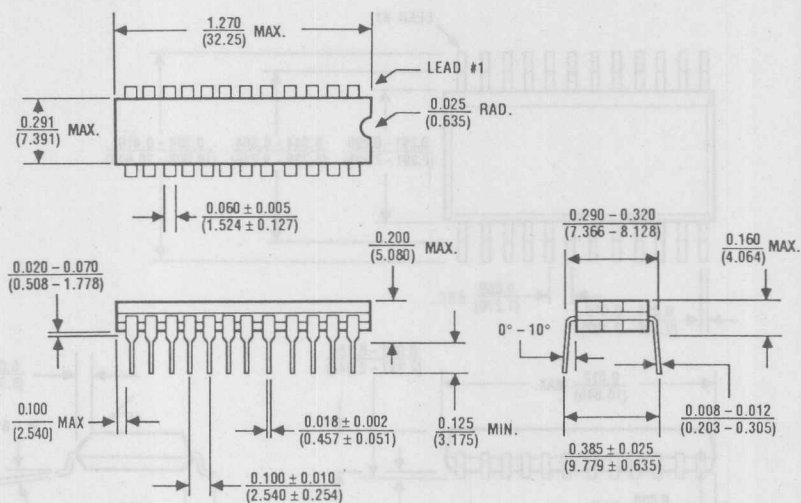
Background information


$$\theta_{JA} = 85^{\circ}\text{C/W}$$

$$\theta_{JC} = 45^{\circ}\text{C/W}$$
$$\theta_{JA} = 55^{\circ}\text{C/W}$$

$$\theta_{JC} = 20^{\circ}\text{C/W}$$

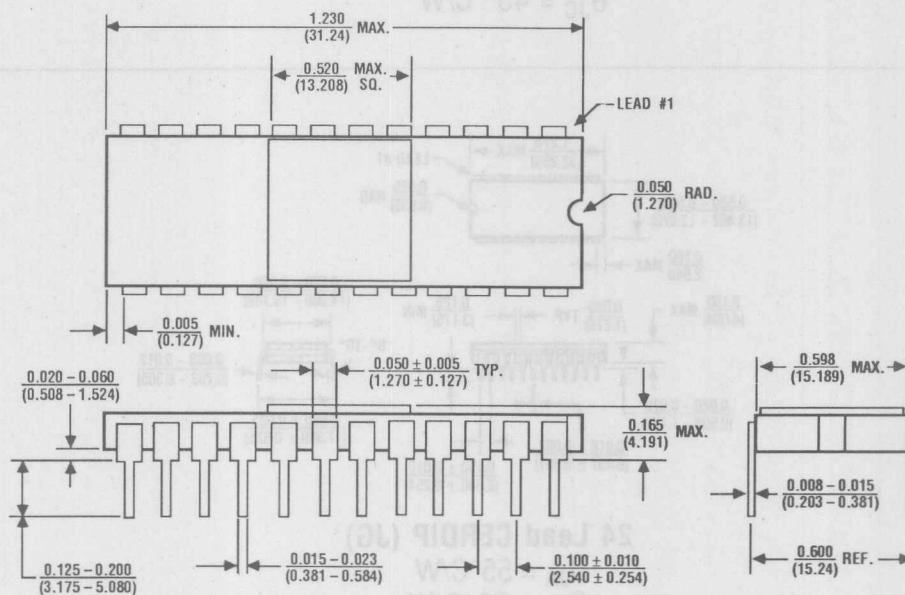
Package Information



24 Lead Narrow Cerdip (RG)

$$\theta_{JA} = 80^{\circ}\text{C/W}$$

$$\theta_{JC} = 40^{\circ}\text{C/W}$$

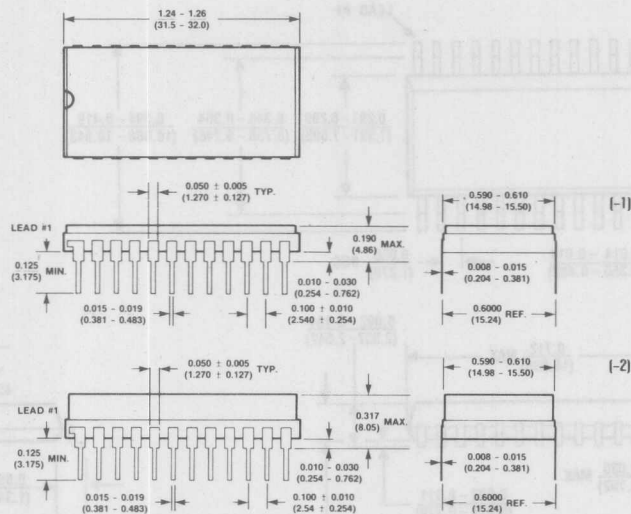


24 Lead Ceramic Sidebrazed (DG)

$$\theta_{JA} = 50^{\circ}\text{C/W}$$

$$\theta_{JC} = 15^{\circ}\text{C/W}$$

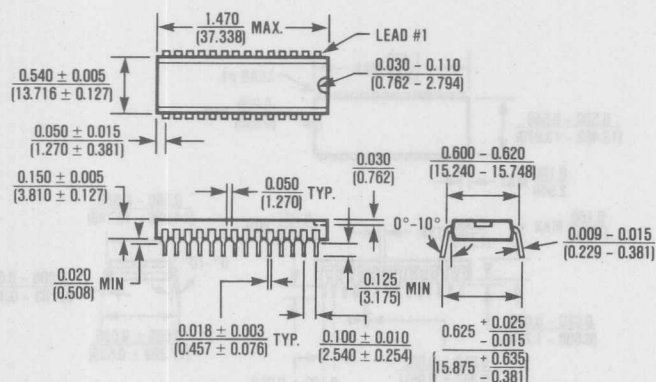
Package Information



24 Lead Ceramic Sidebrazed (DG) -1, -2

$$\theta_{JA} = 50^{\circ}\text{C/W}$$

$$\theta_{JA} = 15^{\circ}\text{C/W}$$

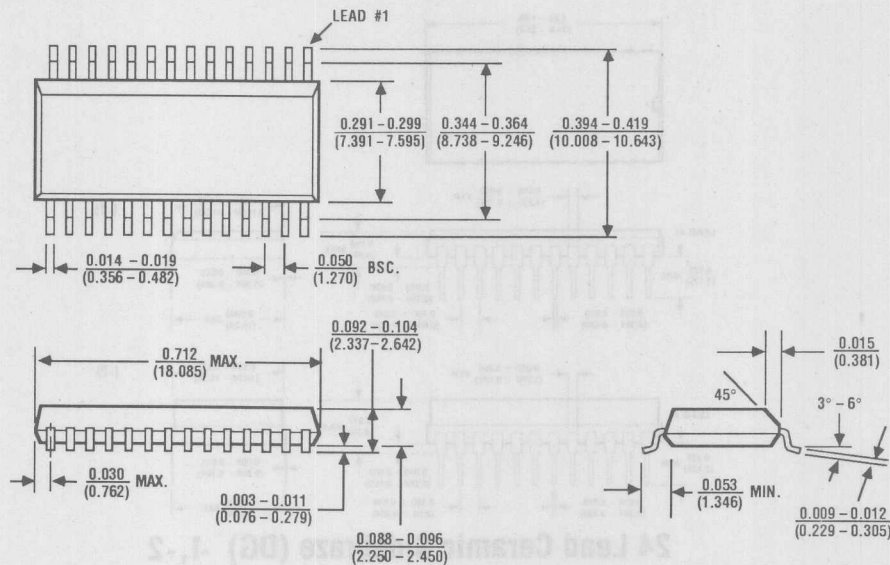


28 Lead Plastic DIP (PI)

$$\theta_{JA} = 110^{\circ}\text{C/W}$$

$$\theta_{JC} = 50^{\circ}\text{C/W}$$

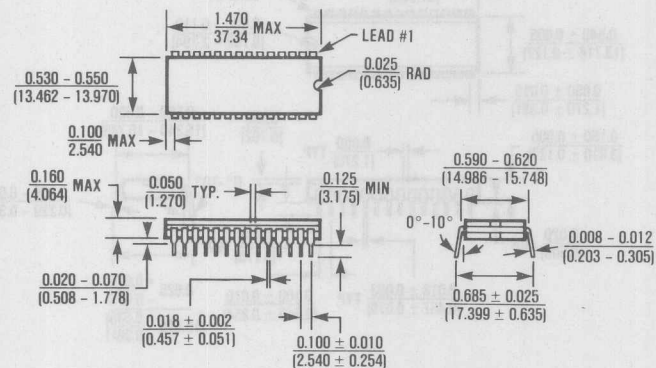
Package Information



28 Lead Small Outline, Wide (WI)

$$\theta_{JA} = 80^{\circ}\text{C/W}$$

$$\theta_{JC} = 45^{\circ}\text{C/W}$$

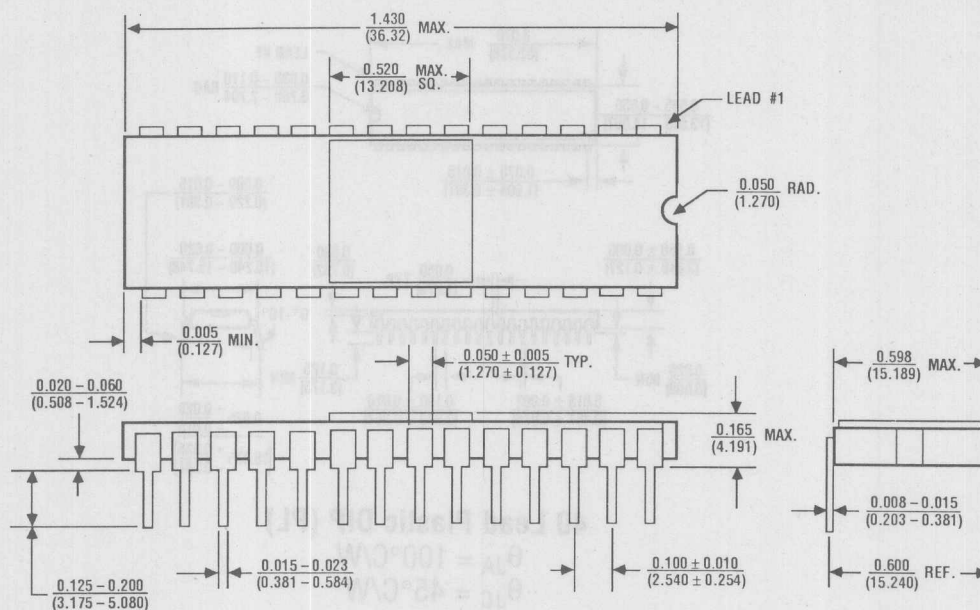


28 Lead CERDIP (JI)

$$\theta_{JA} = 55^{\circ}\text{C/W}$$

$$\theta_{JC} = 20^{\circ}\text{C/W}$$

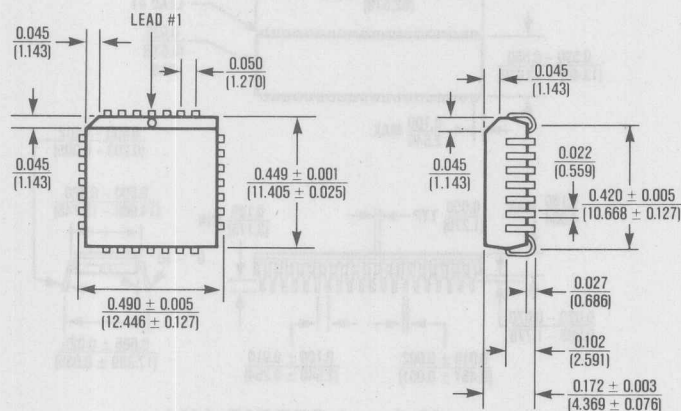
Package Information



28 Lead Ceramic Sidebrazed (DI)

$$\theta_{JA} = 50^{\circ}\text{C/W}$$

$$\theta_{JC} = 15^{\circ}\text{C/W}$$

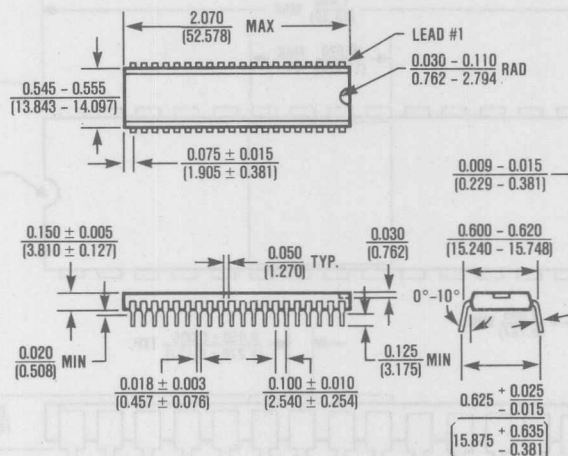


28 Lead Plastic Chip Carrier (Quad Pak) (QI)

$$\theta_{JA} = 100^{\circ}\text{C/W}$$

$$\theta_{JC} = 45^{\circ}\text{C/W}$$

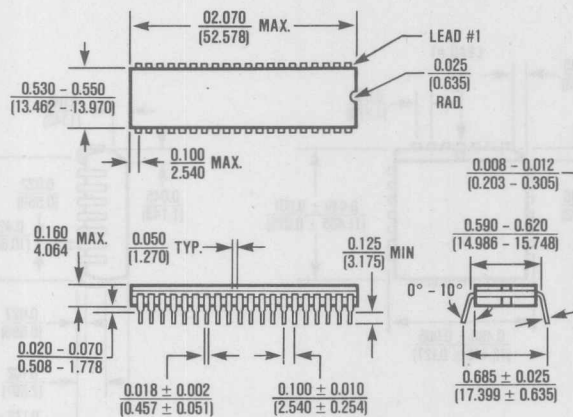
Package Information



40 Lead Plastic DIP (PL)

$$\theta_{JA} = 100^\circ\text{C/W}$$

$$\theta_{JC} = 45^\circ\text{C/W}$$

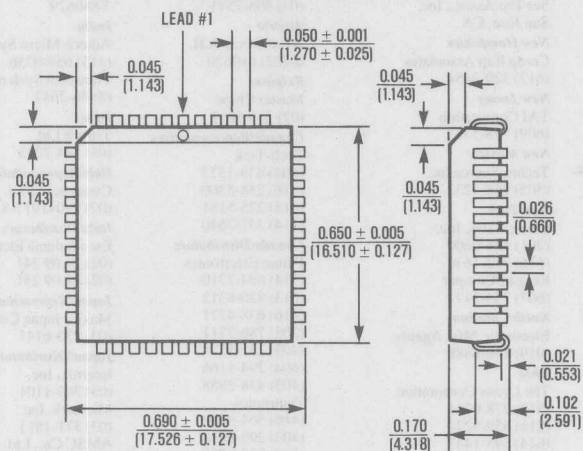


40 Lead Cerdip (JL)

$$\theta_{JA} = 45^\circ\text{C/W}$$

$$\theta_{JC} = 20^\circ\text{C/W}$$

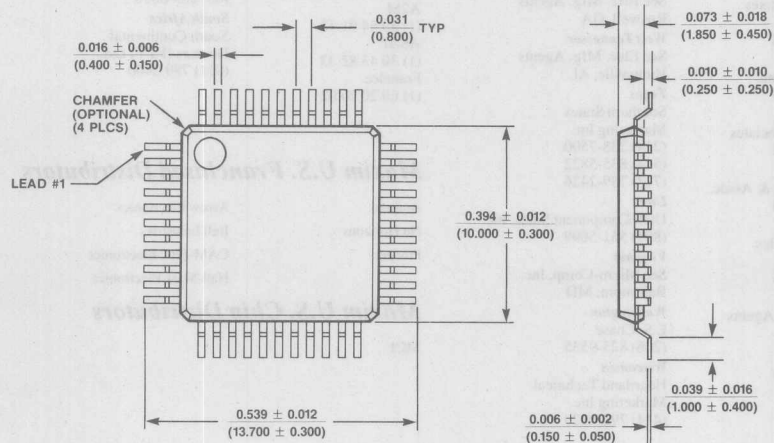
Package Information



44 Lead Plastic Chip Carrier (Quad Pak) (QH)

$$\theta_{JA} = 80^{\circ}\text{C/W}$$

$$\theta_{JC} = 40^{\circ}\text{C/W}$$



44 Lead Plastic Flat Pack (MH)

$$\theta_{JA} = 170^{\circ}\text{C/W}$$

$$\theta_{JC} = 70^{\circ}\text{C/W}$$

Maxim U.S. Sales Representatives

Alabama
Electronic Mfg. Agents
(205) 830-4030

Arizona
Techni Source Inc.
(602) 730-8093

California
Mesa
(619) 278-8021
Pro Assoc., Inc.
(408) 248-5300
Jones & McGeoy Sales, Inc.
(714) 547-6964
(818) 994-6500

Colorado
Thorson Rocky Mountain,
(303) 799-3435

Connecticut
NRG Limited
(203) 384-1112

Florida
Sales Engineer Concepts
(305) 426-4601
(407) 682-4800

Georgia
Electronic Mfg. Agents
(404) 992-7240

Idaho
Inter Mountain Tech
(208) 888-6071

Illinois
Heartland Technical
Marketing Inc.
(708) 358-6622

Indiana
EMCI
(317) 921-3450

Iowa
Contact Factory

Kansas
Contact Factory

Louisiana
See Southern States
Marketing Inc.
Richardson, TX

Maryland
Micro-Comp, Inc.
(301) 644-5700

Massachusetts
Comp Rep Associates
(617) 329-3454

Michigan
A. Blumenberg & Assoc.
(313) 968-3230

Minnesota
Professional Sales
Industries
(612) 944-8545

Mississippi
See Elec. Mfg. Agents
Huntsville, AL

Missouri
Contact Factory

Montana
See E.S. Chase
Portland, OR

Nebraska
Contact Factory

Nevada
(Reno, Tahoe, area only)
See Pro Assoc., Inc.
San Jose, CA

New Hampshire
Comp Rep Associates
(617) 329-3454

New Jersey
TAI Corporation
(609) 778-5353

New Mexico
Techni Source Inc.
(505) 268-4232

New York
Emtec Sales, Inc.
(201) 428-0600
(516) 752-1630
Reagan/Compar
(607) 754-2171

North Carolina
Electronic Mfg. Agents
(919) 846-6888

Ohio
The Lyons Corporation
(513) 278-0714
(216) 659-9224
(614) 895-1447

Oklahoma
See Southern States
Marketing, Inc.,
Richardson, TX

Oregon
E.S. Chase
(503) 292-8840

Pennsylvania
(Pittsburgh area)
See Lyons Corporation
Westerville, OH

South Carolina
Electronic Mfg. Agents
(704) 365-0547

East Tennessee
See Elec. Mfg. Agents
Roswell, GA

West Tennessee
See Elec. Mfg. Agents
Huntsville, AL

Texas
Southern States
Marketing Inc.
(214) 238-7500
(512) 835-5822
(713) 789-2426

Utah
Utah Component Sales, Inc.
(801) 561-5099

Virginia
See Micro-Comp, Inc.
Baltimore, MD

Washington
E.S. Chase
(206) 823-9535

Wisconsin
Heartland Technical
Marketing Inc.
(414) 792-0920

Maxim International Sales Representatives

Australia
Veltek Pty. Ltd.
(03) 808-7511

Austria
Axco Ges.m.b.H.
(0222) 610620

Belgium
Master Chips
(02) 219 5862

Canada/Representatives
Tech-Trek
(604) 439-1373
(416) 238-5300
(613) 225-5161
(514) 337-7540

Canada/Distributors
Future Electronics
(514) 694-7710
(613) 820-8313
(416) 638-4771
(204) 786-7711
(403) 235-5325
(604) 294-1166
(403) 438-2858
Zentronics
(416) 564-9600
(403) 295-8838
(514) 737-9700
(613) 226-8840
(204) 694-1957
(306) 955-2202
(604) 273-5575

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